

## LOW-POWER, SINGLE AND DUAL-CHANNEL DIGITAL ISOLATORS

### Features

- High-speed operation
  - DC to 150 Mbps
  - 15  $\mu$ s startup time
- Wide Operating Supply Voltage: 2.6–5.5 V
- Ultra low power (typical)
  - 5 V Operation:
    - < 2.6 mA/channel at 1 Mbps
    - < 6.8 mA/channel at 100 Mbps
  - 2.70 V Operation:
    - < 2.3 mA/channel at 1 Mbps
    - < 4.6 mA/channel at 100 Mbps
- 100-year life at rated working voltage
- High electromagnetic immunity
- Precise timing (typical)
  - 11 ns propagation delay max
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 5 ns minimum pulse width
  - DC correct
- Up to 5000  $V_{RMS}$  isolation
- Transient immunity: 30 kV/ $\mu$ s
- No start-up initialization required
- Wide temperature range:
  - –40 to 125 °C at 150 Mbps
- RoHS compliant packages
  - SOIC-16 wide body and SOIC-8

### Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters

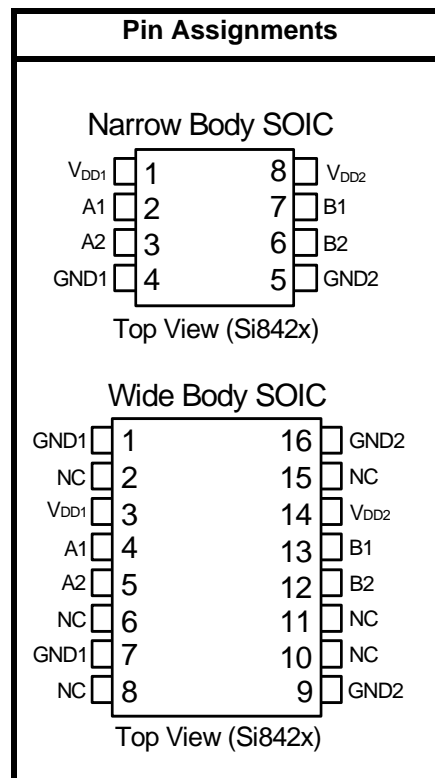
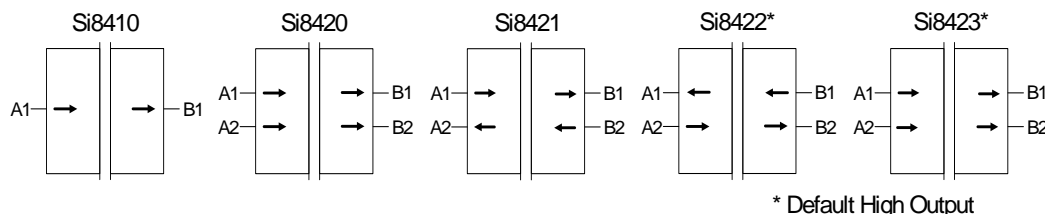
### Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 5000  $V_{RMS}$  for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010, 60601 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)
  - EN60950 (reinforced insulation)

### Description

This Silicon Laboratories family of ultra-low-power digital isolators is comprised of CMOS devices that employ RF couplers to transmit digital information across isolation barriers. Very high-speed operation at low power levels is achieved. These devices are available in 8-pin narrow-body SOIC and 16-pin wide body packages. Two speed grade options (1 and 150 Mbps) are available and achieve worst-case propagation delays of less than 10 ns.

### Block Diagram



Patents pending



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# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

### 1. Electrical Specifications

**Table 1. Electrical Characteristics**

( $V_{DD1} = 5\text{ V} \pm 10\%$ ,  $V_{DD2} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V <sub>DD1</sub> , V <sub>DD2</sub> rising	2.15	2.3	2.5	V
VDD Negative-going Lockout Hysteresis	VDD <sub>HYS</sub>		45	75	95	mV
Positive-going input threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-going input threshold	VT–	All inputs falling	1.1	—	1.4	V
Input hysteresis	V <sub>HYS</sub>		0.40	0.45	0.50	V
High Level Input Voltage	V <sub>IH</sub>		2.0	—	—	V
Low Level Input Voltage	V <sub>IL</sub>		—	—	0.8	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>oh</sub> = –4 mA	V <sub>DD1</sub> , V <sub>DD2</sub> – 0.4	4.8	—	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>ol</sub> = 4 mA	—	0.2	0.4	V
Input Leakage Current	I <sub>L</sub>		—	—	±10	µA
Output Impedance <sup>1</sup>	Z <sub>O</sub>		—	50	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
Si8410Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.0	1.5	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.0	1.5	
V <sub>DD1</sub>		All inputs 1 DC	—	3.0	4.5	
V <sub>DD2</sub>		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.3	2.0	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	5.8	8.7	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8421Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.7	2.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	3.7	5.6	
V <sub>DD2</sub>		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	3.7	5.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	3.7	5.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.7	2.6	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	5.4	8.1	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.3	2.0	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t <sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. Start-up time is the time period from the application of power to valid data at the output.						

# Si8410/20/21 (5 kV) Si8422/23 (2.5 & 5 kV)

**Table 1. Electrical Characteristics (Continued)**

( $V_{DD1} = 5\text{ V} \pm 10\%$ ,  $V_{DD2} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>1 Mbps Supply Current</b> (All inputs = 500 kHz square wave, $C_L = 15\text{ pF}$ on all outputs)						
<b>Si8410Ax, Bx</b>						
$V_{DD1}$			—	2.0	3.0	mA
$V_{DD2}$			—	1.1	1.7	
<b>Si8420Ax, Bx</b>						
$V_{DD1}$			—	3.5	5.3	mA
$V_{DD2}$			—	1.9	2.9	
<b>Si8421Ax, Bx</b>						
$V_{DD1}$			—	2.8	4.2	mA
$V_{DD2}$			—	2.8	4.2	
<b>Si8422Ax, Bx</b>						
$V_{DD1}$			—	2.8	4.2	mA
$V_{DD2}$			—	2.8	4.2	
<b>Si8423Ax, Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	1.9	2.9	
<b>10 Mbps Supply Current</b> (All inputs = 5 MHz square wave, $C_L = 15\text{ pF}$ on all outputs)						
<b>Si8410Bx</b>						
$V_{DD1}$			—	2.1	3.1	mA
$V_{DD2}$			—	1.5	2.1	
<b>Si8420Bx</b>						
$V_{DD1}$			—	3.6	5.4	mA
$V_{DD2}$			—	2.6	3.6	
<b>Si8421Bx</b>						
$V_{DD1}$			—	3.2	4.5	mA
$V_{DD2}$			—	3.2	4.5	
<b>Si8422Bx</b>						
$V_{DD1}$			—	3.2	4.5	mA
$V_{DD2}$			—	3.2	4.5	
<b>Si8423Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	2.5	3.5	
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>1. The nominal output impedance of an isolator driver channel is approximately <math>50\text{ }\Omega</math>, <math>\pm 40\%</math>, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>2. <math>t_{PSK(P-P)}</math> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>3. Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

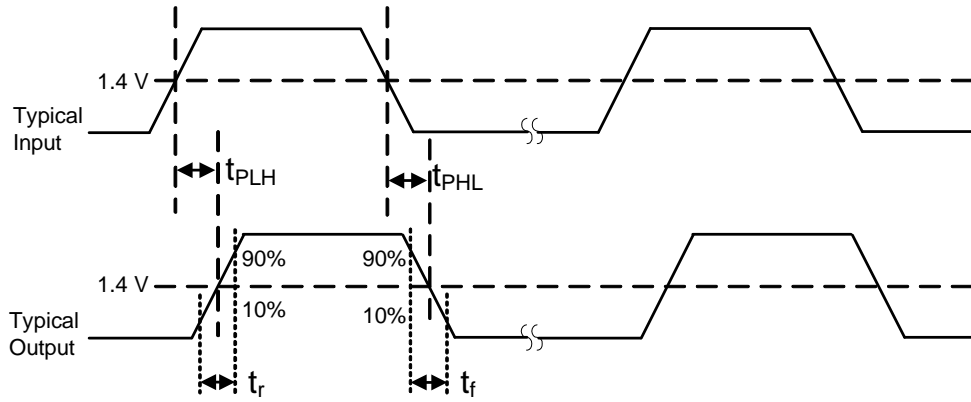
# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 1. Electrical Characteristics (Continued)**

( $V_{DD1} = 5\text{ V} \pm 10\%$ ,  $V_{DD2} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>100 Mbps Supply Current</b> (All inputs = 50 MHz square wave, $C_L = 15\text{ pF}$ on all outputs)						
<b>Si8410Bx</b>						
$V_{DD1}$			—	2.1	3.1	mA
$V_{DD2}$			—	5.0	6.3	
<b>Si8420Bx</b>						
$V_{DD1}$			—	3.7	5.4	mA
$V_{DD2}$			—	9.8	12.3	
<b>Si8421Bx</b>						
$V_{DD1}$			—	6.8	8.5	mA
$V_{DD2}$			—	6.8	8.5	
<b>Si8422Bx</b>						
$V_{DD1}$			—	6.8	8.5	mA
$V_{DD2}$			—	6.8	8.5	
<b>Si8423Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	9.2	11.5	
<b>Timing Characteristics</b>						
<b>Si8422Ax, Si8423Ax</b>						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 1	—	—	35	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew <sup>2</sup>	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	$t_{PSK}$		—	—	35	ns
<b>Si8422Bx, Si8423Bx</b>						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 1	4.0	8.0	11	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 1	—	1.5	3.0	ns
Propagation Delay Skew <sup>2</sup>	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	$t_{PSK}$		—	0.5	1.5	ns
<b>All Models</b>						
Output Rise Time	$t_r$	$C_L = 15\text{ pF}$	—	2.0	4.0	ns
Output Fall Time	$t_f$	$C_L = 15\text{ pF}$	—	2.0	4.0	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or $0\text{ V}$	—	30	—	kV/ $\mu\text{s}$
Start-up Time <sup>3</sup>	$t_{SU}$		—	15	40	$\mu\text{s}$
<b>Notes:</b>						
1. The nominal output impedance of an isolator driver channel is approximately $50\text{ }\Omega$ , $\pm 40\%$ , which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. Start-up time is the time period from the application of power to valid data at the output.						



**Figure 1. Propagation Delay Timing**

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 2. Electrical Characteristics**

( $V_{DD1} = 3.3 \text{ V} \pm 10\%$ ,  $V_{DD2} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V <sub>DD1</sub> , V <sub>DD2</sub> rising	2.15	2.3	2.5	V
VDD Negative-going Lockout Hysteresis	VDD <sub>HYS</sub>		45	75	95	mV
Positive-going input threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-going input threshold	VT–	All inputs falling	1.1	—	1.4	V
Input hysteresis	V <sub>HYS</sub>		0.40	0.45	0.50	V
High Level Input Voltage	V <sub>IH</sub>		2.0	—	—	V
Low Level Input Voltage	V <sub>IL</sub>		—	—	0.8	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>oh</sub> = –4 mA	V <sub>DD1</sub> , V <sub>DD2</sub> – 0.4	3.1	—	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>ol</sub> = 4 mA	—	0.2	0.4	V
Input Leakage Current	I <sub>L</sub>		—	—	±10	µA
Output Impedance (Si8410/20) <sup>1</sup>	Z <sub>O</sub>		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.0	1.5	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.0	1.5	
V <sub>DD1</sub>		All inputs 1 DC	—	3.0	4.5	
V <sub>DD2</sub>		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.3	2.0	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	5.8	8.7	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8421Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.7	2.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	3.7	5.6	
V <sub>DD2</sub>		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	3.7	5.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	3.7	5.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.7	2.6	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	5.4	8.1	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.3	2.0	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Notes:						
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.						
2. t <sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.						
3. Start-up time is the time period from the application of power to valid data at the output.						



**Table 2. Electrical Characteristics (Continued)**

( $V_{DD1} = 3.3 \text{ V} \pm 10\%$ ,  $V_{DD2} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>1 Mbps Supply Current</b> (All inputs = 500 kHz square wave, $C_L = 15 \text{ pF}$ on all outputs)						
<b>Si8410Ax, Bx</b>						
$V_{DD1}$			—	2.0	3.0	mA
$V_{DD2}$			—	1.1	1.7	
<b>Si8420Ax, Bx</b>						
$V_{DD1}$			—	3.5	5.3	mA
$V_{DD2}$			—	1.9	2.9	
<b>Si8421Ax, Bx</b>						
$V_{DD1}$			—	2.8	4.2	mA
$V_{DD2}$			—	2.8	4.2	
<b>Si8422Ax, Bx</b>						
$V_{DD1}$			—	2.8	4.2	mA
$V_{DD2}$			—	2.8	4.2	
<b>Si8423Ax, Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	1.9	2.9	
<b>10 Mbps Supply Current</b> (All inputs = 5 MHz square wave, $C_L = 15 \text{ pF}$ on all outputs)						
<b>Si8410Bx</b>						
$V_{DD1}$			—	2.0	3.0	mA
$V_{DD2}$			—	1.3	1.8	
<b>Si8420Bx</b>						
$V_{DD1}$			—	3.5	5.3	mA
$V_{DD2}$			—	2.3	3.2	
<b>Si8421Bx</b>						
$V_{DD1}$			—	3.0	4.4	mA
$V_{DD2}$			—	3.0	4.4	
<b>Si8422Bx</b>						
$V_{DD1}$			—	3.0	4.4	mA
$V_{DD2}$			—	3.0	4.4	
<b>Si8423Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	2.2	3.1	
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>The nominal output impedance of an isolator driver channel is approximately <math>50 \Omega</math>, <math>\pm 40\%</math>, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li><math>t_{PSK(P-P)}</math> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 2. Electrical Characteristics (Continued)**

( $V_{DD1} = 3.3 \text{ V} \pm 10\%$ ,  $V_{DD2} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>100 Mbps Supply Current</b> (All inputs = 50 MHz square wave, $C_L = 15 \text{ pF}$ on all outputs)						
<b>Si8410Bx</b>						
$V_{DD1}$			—	2.0	3.0	mA
$V_{DD2}$			—	3.6	4.5	
<b>Si8420Bx</b>						
$V_{DD1}$			—	4.5	5.3	mA
$V_{DD2}$			—	7.0	8.8	
<b>Si8421Bx</b>						
$V_{DD1}$			—	5.3	6.6	mA
$V_{DD2}$			—	5.3	6.6	
<b>Si8422Bx</b>						
$V_{DD1}$			—	5.3	6.6	mA
$V_{DD2}$			—	5.3	6.6	
<b>Si8423Bx</b>						
$V_{DD1}$			—	3.4	5.1	mA
$V_{DD2}$			—	6.6	8.3	
<b>Timing Characteristics</b>						
<b>Si8422Ax, Si8423Ax</b>						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 1	—	—	35	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew <sup>2</sup>	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	$t_{PSK}$		—	—	35	ns
<b>Si8422Bx, Si8423Bx</b>						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 1	4.0	8.0	11	ns
Pulse Width Distortion $ t_{PLH} - t_{PHL} $	PWD	See Figure 1	—	1.5	3.0	ns
Propagation Delay Skew <sup>2</sup>	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	$t_{PSK}$		—	0.5	1.5	ns
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>1. The nominal output impedance of an isolator driver channel is approximately <math>50 \Omega</math>, <math>\pm 40\%</math>, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>2. <math>t_{PSK(P-P)}</math> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>3. Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

**Table 2. Electrical Characteristics (Continued)**

( $V_{DD1} = 3.3 \text{ V} \pm 10\%$ ,  $V_{DD2} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>All Models</b>						
Output Rise Time	$t_r$	$C_L = 15 \text{ pF}$	—	2.0	4.0	ns
Output Fall Time	$t_f$	$C_L = 15 \text{ pF}$	—	2.0	4.0	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	30	—	kV/ $\mu\text{s}$
Start-up Time <sup>3</sup>	$t_{SU}$		—	15	40	$\mu\text{s}$
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>1. The nominal output impedance of an isolator driver channel is approximately <math>50 \text{ } \Omega</math>, <math>\pm 40\%</math>, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>2. <math>t_{PSK(P-P)}</math> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>3. Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 3. Electrical Characteristics<sup>1</sup>**

(V<sub>DD1</sub> = 2.70 V, V<sub>DD2</sub> = 2.70 V, T<sub>A</sub> = -40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V <sub>DD1</sub> , V <sub>DD2</sub> rising	2.15	2.3	2.5	V
VDD Negative-going Lockout Hysteresis	VDD <sub>HYS</sub>		45	75	95	mV
Positive-going input threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-going input threshold	VT−	All inputs falling	1.1	—	1.4	V
Input hysteresis	V <sub>HYS</sub>		0.40	0.45	0.50	V
High Level Input Voltage	V <sub>IH</sub>		2.0	—	—	V
Low Level Input Voltage	V <sub>IL</sub>		—	—	0.8	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>oh</sub> = −4 mA	V <sub>DD1</sub> , V <sub>DD2</sub> − 0.4	2.3	—	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>ol</sub> = 4 mA	—	0.2	0.4	V
Input Leakage Current	I <sub>L</sub>		—	—	±10	μA
Output Impedance <sup>2</sup>	Z <sub>O</sub>		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.0	1.5	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.0	1.5	
V <sub>DD1</sub>		All inputs 1 DC	—	3.0	4.5	
V <sub>DD2</sub>		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.3	2.0	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	5.8	8.7	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8421Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	1.7	2.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	3.7	5.6	
V <sub>DD2</sub>		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	3.7	5.6	mA
V <sub>DD2</sub>		All inputs 0 DC	—	3.7	5.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.7	2.6	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V <sub>DD1</sub>		All inputs 0 DC	—	5.4	8.1	mA
V <sub>DD2</sub>		All inputs 0 DC	—	1.7	2.6	
V <sub>DD1</sub>		All inputs 1 DC	—	1.3	2.0	
V <sub>DD2</sub>		All inputs 1 DC	—	1.7	2.6	

**Notes:**

- Specifications in this table are also valid at V<sub>DD1</sub> = 2.6 V and V<sub>DD2</sub> = 2.6 V when the operating temperature range is constrained to T<sub>A</sub> = 0 to 85 °C.
- The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
- t<sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
- Start-up time is the time period from the application of power to valid data at the output.

**Table 3. Electrical Characteristics<sup>1</sup> (Continued)**

(V<sub>DD1</sub> = 2.70 V, V<sub>DD2</sub> = 2.70 V, T<sub>A</sub> = -40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>1 Mbps Supply Current</b> (All inputs = 500 kHz square wave, C <sub>L</sub> = 15 pF on all outputs)						
<b>Si8410Ax, Bx</b>						
V <sub>DD1</sub>			—	2.0	3.0	mA
V <sub>DD2</sub>			—	1.1	1.7	
<b>Si8420Ax, Bx</b>						
V <sub>DD1</sub>			—	3.5	5.3	mA
V <sub>DD2</sub>			—	1.9	2.9	
<b>Si8421Ax, Bx</b>						
V <sub>DD1</sub>			—	2.8	4.2	mA
V <sub>DD2</sub>			—	2.8	4.2	
<b>Si8422Ax, Bx</b>						
V <sub>DD1</sub>			—	2.8	4.2	mA
V <sub>DD2</sub>			—	2.8	4.2	
<b>Si8423Ax, Bx</b>						
V <sub>DD1</sub>			—	3.3	5.0	mA
V <sub>DD2</sub>			—	1.8	2.8	
<b>10 Mbps Supply Current</b> (All inputs = 5 MHz square wave, C <sub>L</sub> = 15 pF on all outputs)						
<b>Si8410Bx</b>						
V <sub>DD1</sub>			—	2.0	3.0	mA
V <sub>DD2</sub>			—	1.1	1.7	
<b>Si8420Bx</b>						
V <sub>DD1</sub>			—	3.5	5.3	mA
V <sub>DD2</sub>			—	2.1	3.0	
<b>Si8421Bx</b>						
V <sub>DD1</sub>			—	2.9	4.3	mA
V <sub>DD2</sub>			—	2.9	4.3	
<b>Si8422Bx</b>						
V <sub>DD1</sub>			—	2.9	4.3	mA
V <sub>DD2</sub>			—	2.9	4.3	
<b>Si8423Bx</b>						
V <sub>DD1</sub>			—	3.4	5.1	mA
V <sub>DD2</sub>			—	2.0	2.9	
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>Specifications in this table are also valid at V<sub>DD1</sub> = 2.6 V and V<sub>DD2</sub> = 2.6 V when the operating temperature range is constrained to T<sub>A</sub> = 0 to 85 °C.</li> <li>The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>t<sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 3. Electrical Characteristics<sup>1</sup> (Continued)**

(V<sub>DD1</sub> = 2.70 V, V<sub>DD2</sub> = 2.70 V, T<sub>A</sub> = -40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>100 Mbps Supply Current</b> (All inputs = 50 MHz square wave, CL = 15 pF on all outputs)						
<b>Si8410Bx</b>						
V <sub>DD1</sub>			—	2.0	3.0	mA
V <sub>DD2</sub>			—	2.0	3.0	
<b>Si8420Bx</b>						
V <sub>DD1</sub>			—	3.5	5.3	mA
V <sub>DD2</sub>			—	5.5	6.9	
<b>Si8421Bx</b>						
V <sub>DD1</sub>			—	4.6	5.8	mA
V <sub>DD2</sub>			—	4.6	5.8	
<b>Si8422Bx</b>						
V <sub>DD1</sub>			—	4.6	5.8	mA
V <sub>DD2</sub>			—	4.6	5.8	
<b>Si8423Bx</b>						
V <sub>DD1</sub>			—	3.4	5.1	mA
V <sub>DD2</sub>			—	5.2	6.5	
<b>Timing Characteristics</b>						
<b>Si8422Ax, Si8423Ax</b>						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>	See Figure 1	—	—	35	ns
Pulse Width Distortion  t <sub>PLH</sub> - t <sub>PHL</sub>	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew <sup>3</sup>	t <sub>PSK(P-P)</sub>		—	—	40	ns
Channel-Channel Skew	t <sub>PSK</sub>		—	—	35	ns
<b>Si8422Bx, Si8423Bx</b>						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>	See Figure 1	4.0	8.0	11	ns
Pulse Width Distortion  t <sub>PLH</sub> - t <sub>PHL</sub>	PWD	See Figure 1	—	1.5	3.0	ns
Propagation Delay Skew <sup>3</sup>	t <sub>PSK(P-P)</sub>		—	2.0	3.0	ns
Channel-Channel Skew	t <sub>PSK</sub>		—	0.5	1.5	ns
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>Specifications in this table are also valid at V<sub>DD1</sub> = 2.6 V and V<sub>DD2</sub> = 2.6 V when the operating temperature range is constrained to T<sub>A</sub> = 0 to 85 °C.</li> <li>The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>t<sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

**Table 3. Electrical Characteristics<sup>1</sup> (Continued)**

(V<sub>DD1</sub> = 2.70 V, V<sub>DD2</sub> = 2.70 V, T<sub>A</sub> = -40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>All Models</b>						
Output Rise Time	t <sub>r</sub>	C <sub>L</sub> = 15 pF	—	2.0	4.0	ns
Output Fall Time	t <sub>f</sub>	C <sub>L</sub> = 15 pF	—	2.0	4.0	ns
Common Mode Transient Immunity	CMTI	V <sub>I</sub> = V <sub>DD</sub> or 0 V	—	30	—	kV/μs
Start-up Time <sup>4</sup>	t <sub>SU</sub>		—	15	40	μs
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T<sub>A</sub> = 0 to 85 °C.</li> <li>The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>t<sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> <li>Start-up time is the time period from the application of power to valid data at the output.</li> </ol>						

**Table 4. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature <sup>2</sup>	T <sub>STG</sub>	-65	—	150	°C
Operating Temperature	T <sub>A</sub>	-40	—	125	°C
Supply Voltage	V <sub>DD1</sub> , V <sub>DD2</sub>	-0.5	—	6.0	V
Input Voltage	V <sub>I</sub>	-0.5	—	V <sub>DD</sub> + 0.5	V
Output Voltage	V <sub>O</sub>	-0.5	—	V <sub>DD</sub> + 0.5	V
Output Current Drive Channel	I <sub>O</sub>	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s) NB SOIC-8		—	—	4500	V <sub>RMS</sub>
Maximum Isolation Voltage (1 s) WB SOIC-16		—	—	6500	V <sub>RMS</sub>
<b>Notes:</b>					
<ol style="list-style-type: none"> <li>Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.</li> <li>VDE certifies storage temperature from -40 to 150 °C.</li> </ol>					

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 5. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	$T_A$	150 Mbps, 15 pF, 5 V	-40	25	125	C°
Supply Voltage	$V_{DD1}$		2.70	—	5.5	V
	$V_{DD2}$		2.70	—	5.5	V
*Note: The maximum ambient temperature is dependent upon data frequency, output loading, the number of operating channels, and supply voltage.						

**Table 6. Regulatory Information<sup>1,2</sup>**

<b>CSA</b>
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 600 V <sub>RMS</sub> basic insulation working voltage.
60950: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 1000 V <sub>RMS</sub> basic insulation working voltage.
60601: Up to 125 V <sub>RMS</sub> reinforced insulation working voltage; up to 380 V <sub>RMS</sub> basic insulation working voltage.
<b>VDE</b>
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 891 V <sub>peak</sub> for basic insulation working voltage.
60950: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 1000 V <sub>RMS</sub> basic insulation working voltage.
<b>UL</b>
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V <sub>RMS</sub> isolation voltage for basic insulation.
<b>Notes:</b>
1. Pending.
2. Regulatory Certifications apply to 2.5 kV <sub>RMS</sub> rated devices which are production tested to 3.0 kV <sub>RMS</sub> for 1 sec. Regulatory Certifications apply to 5.0 kV <sub>RMS</sub> rated devices which are production tested to 6.0 kV <sub>RMS</sub> for 1 sec. For more information, see "6. Ordering Guide" on page 29.



**Table 7. Insulation and Safety-Related Specifications**

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-8	
Nominal Air Gap (Clearance) <sup>1</sup>	L(IO1)		8.0 min	4.9 min	mm
Nominal External Tracking (Creepage) <sup>1</sup>	L(IO2)		8.0 min	4.01 min	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V <sub>RMS</sub>
Erosion Depth	ED		0.019	0.040	mm
Resistance (Input-Output) <sup>2</sup>	R <sub>IO</sub>		10 <sup>12</sup>	10 <sup>12</sup>	Ω
Capacitance (Input-Output) <sup>2</sup>	C <sub>IO</sub>	f = 1 MHz	2.0	1.0	pF
Input Capacitance <sup>3</sup>	C <sub>I</sub>		4.0	4.0	pF
<b>Notes:</b> <ol style="list-style-type: none"> <li>The values in this table correspond to the nominal creepage and clearance values as detailed in “7. Package Outline: 16-Pin Wide Body SOIC”, “9. Package Outline: 8-Pin Narrow Body SOIC”. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16 package and 4.7 mm minimum for the NB SOIC-8 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.</li> <li>To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 (1–4, NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (5–8, NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.</li> <li>Measured from input pin to ground.</li> </ol>					

**Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings**

Parameter	Test Conditions	Specification	
		NB SOIC8	WB SOIC 16
Basic isolation group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V <sub>RMS</sub>	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V <sub>RMS</sub>	I-III	I-IV
	Rated Mains Voltages ≤ 600 V <sub>RMS</sub>	I-II	I-III

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxx\***

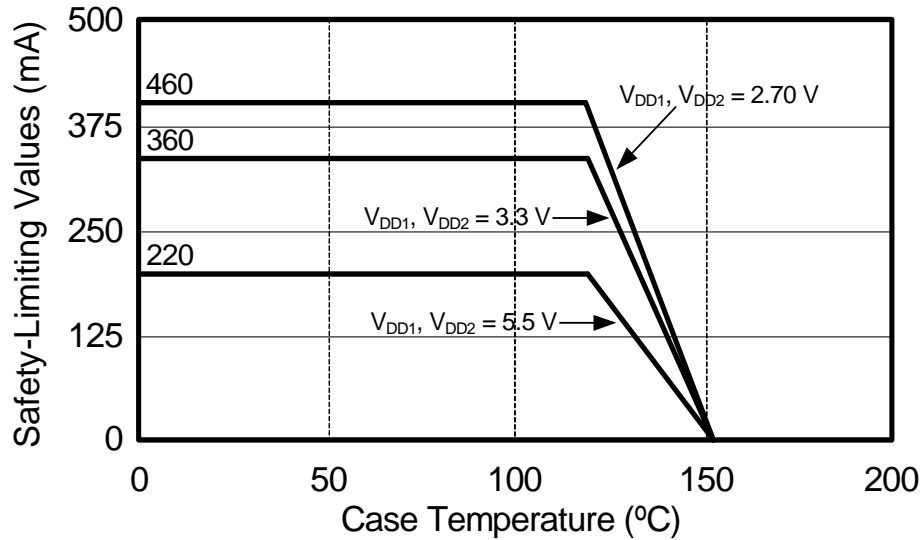
Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-8	
Maximum Working Insulation Voltage	$V_{IORM}$		891	560	Vpeak
Input to Output Test Voltage		Method b1 ( $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC)	1375	1050	
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 60$ sec)	$V_{TR}$		6000	4000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$		$>10^9$	$>10^9$	$\Omega$
<b>*Note:</b> This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.					

**Table 10. IEC Safety Limiting Values<sup>1</sup>**

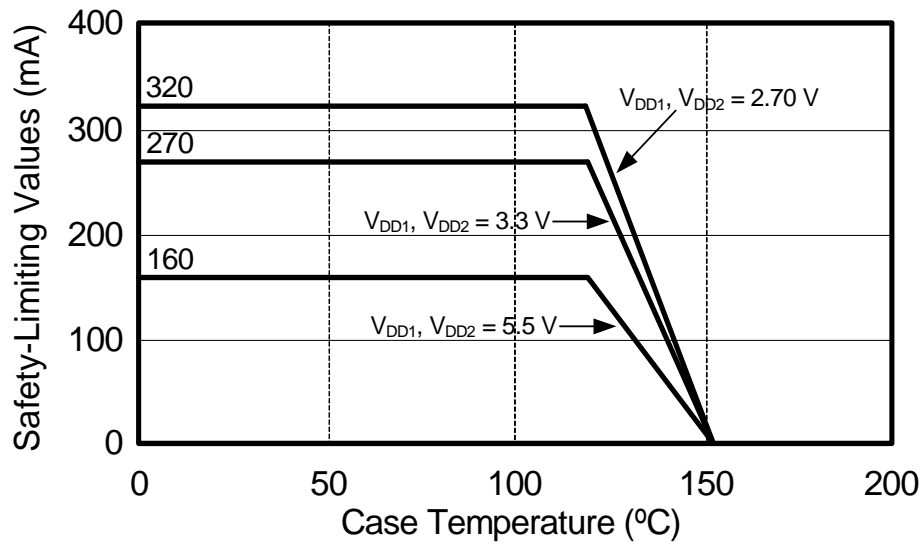
Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-8	
Case Temperature	$T_S$		—	—	150	150	°C
Safety input, output, or supply current	$I_S$	$\theta_{JA} = 140$ °C/W (NB SOIC-8), 100 °C (WB SOIC-16), $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C	—	—	220	160	mA
Device Power Dissipation <sup>2</sup>	$P_D$		—	—	150	150	mW
<b>Notes:</b> 1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3 and 4. 2. The Si84xx is tested with $VDD1 = VDD2 = 5.5$ V, $T_J = 150$ °C, $C_L = 15$ pF, input a 150 Mbps 50% duty cycle square wave.							

**Table 11. Thermal Characteristics**

Parameter	Symbol	WB SOIC-16	NB SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$	100	140	$^{\circ}\text{C}/\text{W}$



**Figure 2. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**



**Figure 3. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 12. Si84xx Logic Operation Table**

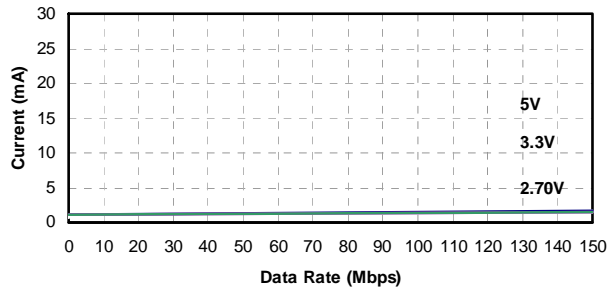
$V_I$ Input <sup>1,4</sup>	VDDI State <sup>1,2,3</sup>	VDDO State <sup>1,2,3</sup>	$V_O$ Output <sup>1,4</sup>	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	H (Si8422/23) L (Si8410/20/21)	Upon transition of VDDI from unpowered to powered, $V_O$ returns to the same state as $V_I$ in less than 1 $\mu$ s.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, $V_O$ returns to the same state as $V_I$ within 1 $\mu$ s.

**Notes:**

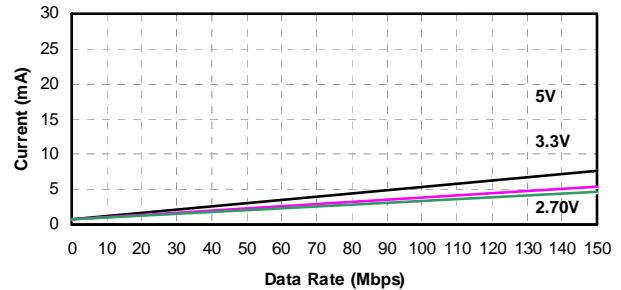
1. VDDI and VDDO are the input and output power supplies.  $V_I$  and  $V_O$  are the respective input and output terminals.
2. Powered (P) state is defined as  $2.70\text{ V} < \text{VDD} < 5.5\text{ V}$ .
3. Unpowered (UP) state is defined as  $\text{VDD} = 0\text{ V}$ .
4. X = not applicable; H = Logic High; L = Logic Low.

## 2. Typical Performance Characteristics

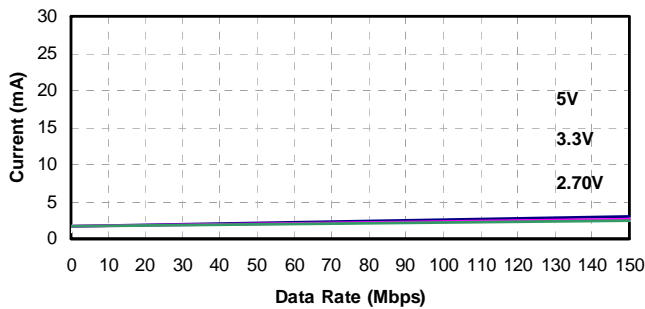
The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 1, 2, and 3 for actual specification limits.



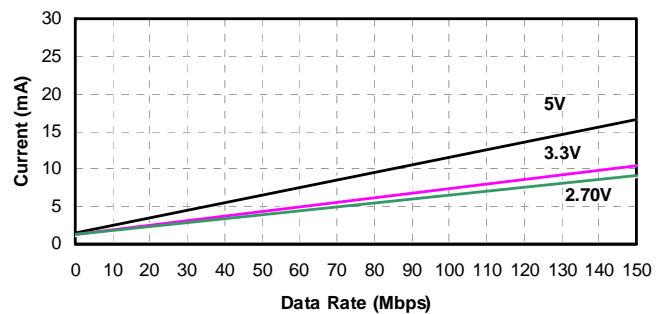
**Figure 4. Si8410 Typical  $V_{DD1}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation**



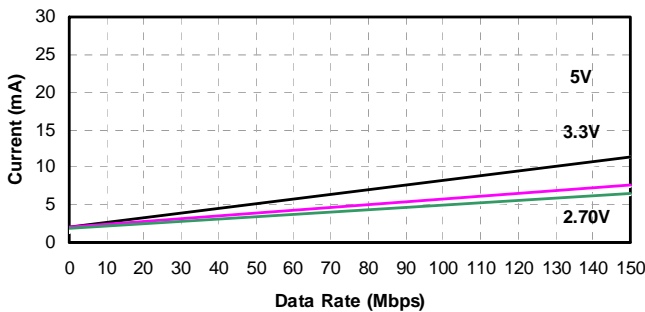
**Figure 7. Si8410 Typical  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)**



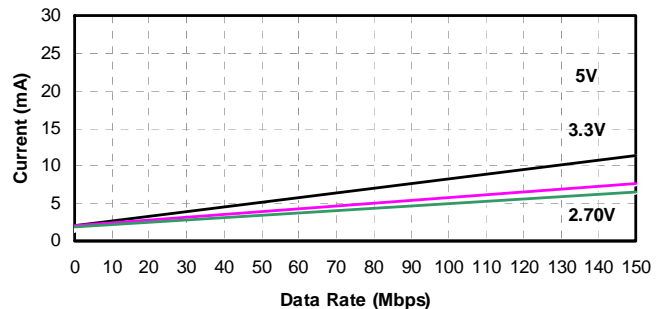
**Figure 5. Si8420 Typical  $V_{DD1}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation**



**Figure 8. Si8420 Typical  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)**



**Figure 6. Si8421 Typical  $V_{DD1}$  or  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)**



**Figure 9. Si8422 Typical  $V_{DD1}$  or  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)**

# Si8410/20/21 (5 kV) Si8422/23 (2.5 & 5 kV)

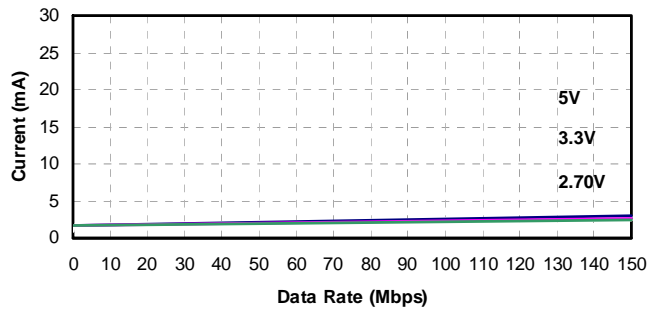


Figure 10. Si8423 Typical  $V_{DD1}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

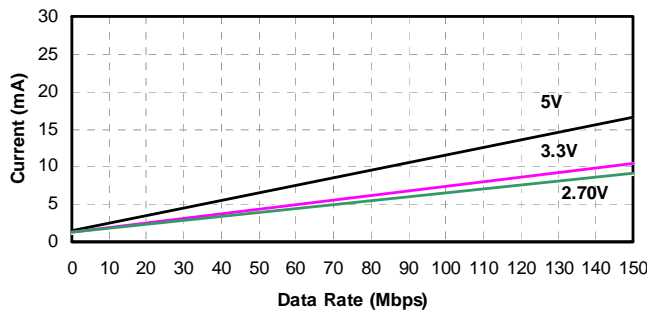


Figure 11. Si8423 Typical  $V_{DD2}$  Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

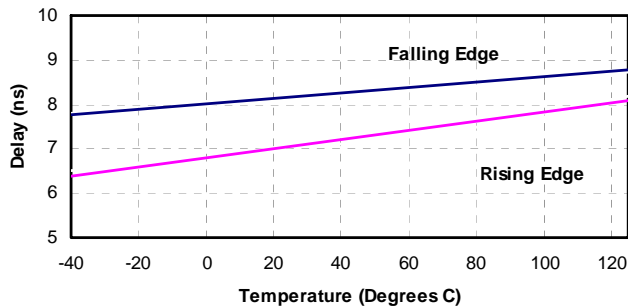


Figure 12. Propagation Delay vs. Temperature

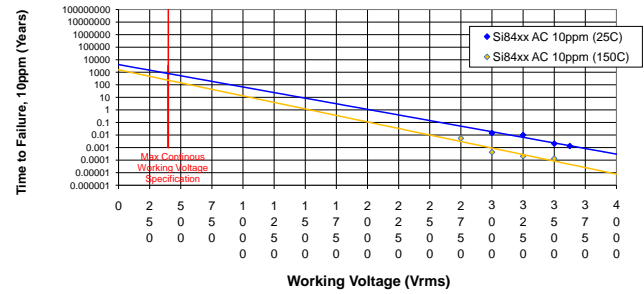


Figure 13. Time-Dependent Breakdown Dielectric Breakdown

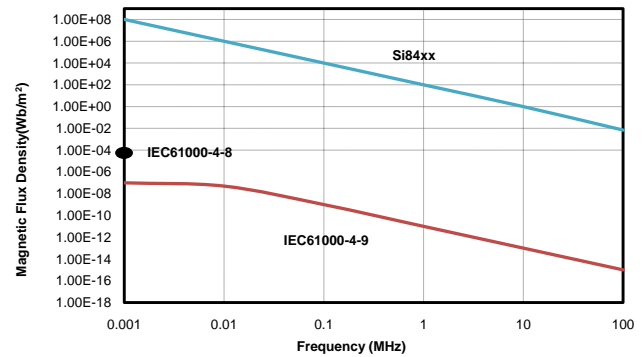
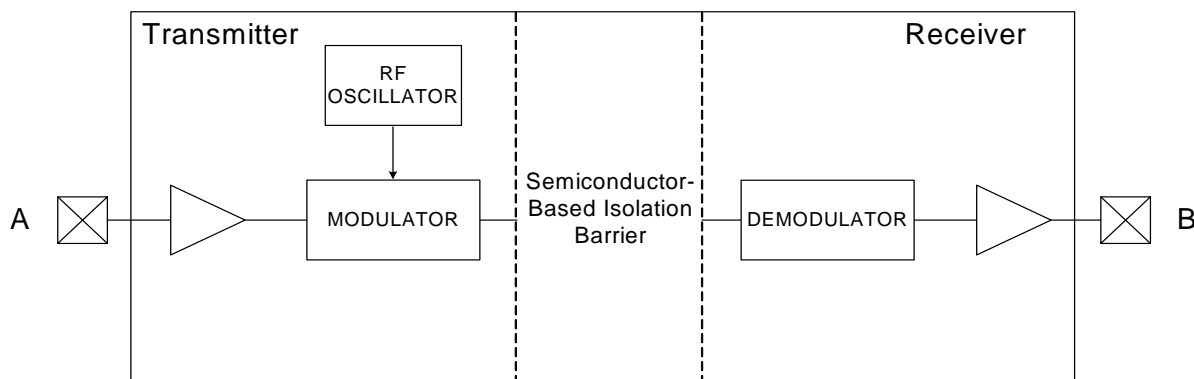


Figure 14. Electromagnetic Immunity

### 3. Application Information

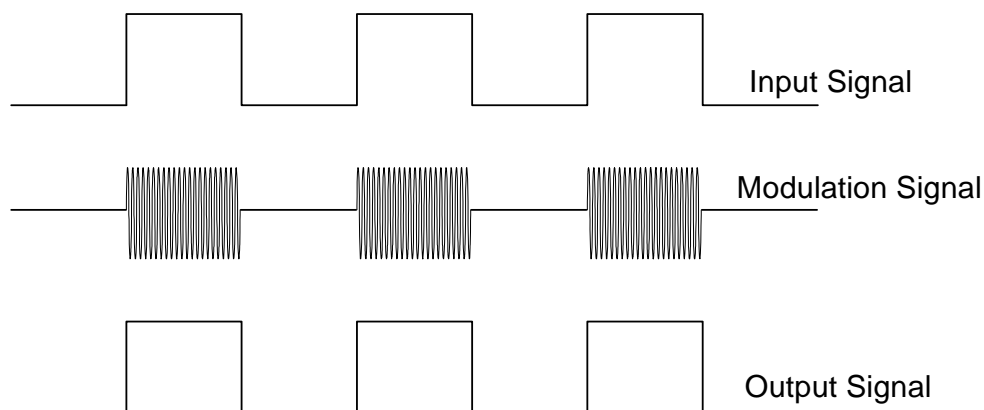
#### 3.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si84xx channel is shown in Figure 15.



**Figure 15. Simplified Channel Diagram**

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 16 for more details.



**Figure 16. Modulation Scheme**

## 3.2. Eye Diagram

Figure 17 illustrates an eye-diagram taken on an Si8422. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8422 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

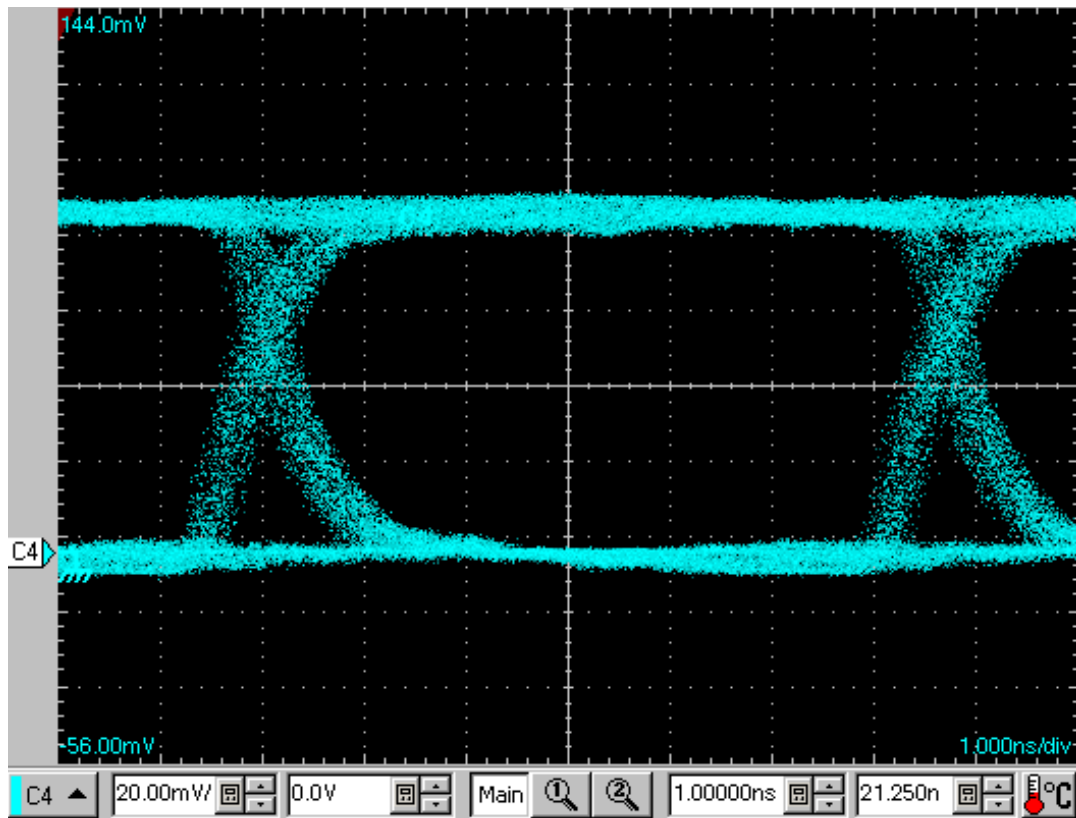


Figure 17. Eye Diagram



### **3.3. Layout Recommendations**

To ensure safety in the end user application, high voltage circuits (i.e., circuits with  $>30 V_{AC}$ ) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with  $<30 V_{AC}$ ) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 16 and Table 7 on page 17 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010, 60950, 60601, etc.) requirements before starting any design that uses a digital isolator.

#### **3.3.1. Supply Bypass**

The Si842x family requires a 1  $\mu F$  bypass capacitor between  $V_{DD1}$  and GND1 and  $V_{DD2}$  and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, it is further recommended that the user include 100  $\Omega$  resistors in series with the inputs and outputs if the supply or system is excessively noisy.

#### **3.3.2. Output Pin Termination**

The nominal output impedance of an isolator driver channel is approximately 50  $\Omega$ ,  $\pm 40\%$ , which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

### 3.3.3. RF Radiated Emissions

The Si84xx family uses an RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si84xx evaluation board passes FCC Class B (Part 15) requirements. Table 13 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions where all inputs are tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

**Table 13. Radiated Emissions**

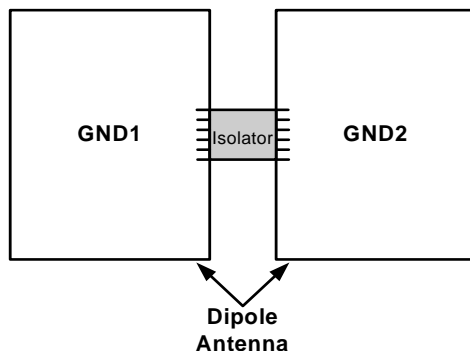
Frequency (MHz)	Measured (dB $\mu$ V/m)	FCC Spec (dB $\mu$ V/m)	Compared to Spec (dB)
712	29	37	-8
1424	39	54	-15
2136	42	54	-12
2848	43	54	-11
4272	44	54	-10
4984	44	54	-10
5696	44	54	-10

### 3.3.4. RF, Magnetic, and Common Mode Transient Immunity

The Si84xx families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 30 kV/ $\mu$ s (typical). During a high surge event, the output may glitch low for up to 20 to 30 ns, but the output corrects immediately after the surge event.

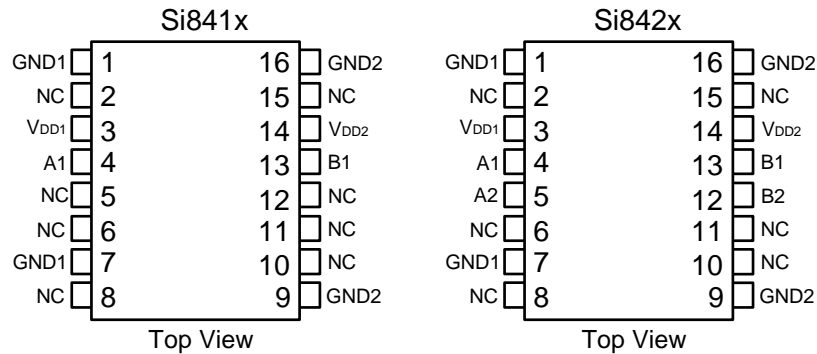
The Si84xx families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 18, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si84xx digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si84xx devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.



**Figure 18. Dipole Antenna**

#### 4. Pin Descriptions (Wide-Body SOIC)



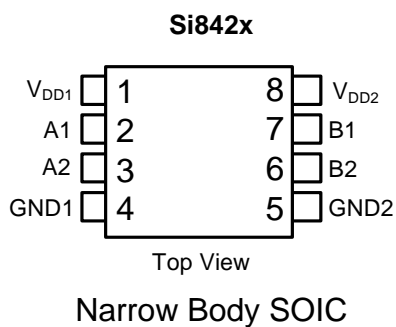
Name	SOIC-16 Pin# Si8410	SOIC-16 Pin# Si842x	Type	Description
GND1	1	1	Ground	Side 1 ground.
NC*	2, 5, 6, 8, 10, 11, 12, 15	2, 6, 8, 10, 11, 15	No Connect	NC
V <sub>DD1</sub>	3	3	Supply	Side 1 power supply.
A1	4	4	Digital I/O	Side 1 digital input or output.
A2	NC	5	Digital I/O	Side 1 digital input or output.
GND1	7	7	Ground	Side 1 ground.
GND2	9	9	Ground	Side 2 ground.
B2	NC	12	Digital I/O	Side 2 digital input or output.
B1	13	13	Digital I/O	Side 2 digital input or output.
V <sub>DD2</sub>	14	14	Supply	Side 2 power supply.
GND2	16	16	Ground	Side 2 ground.
<b>*Note:</b> No Connect. These pins are not internally connected. They can be left floating, tied to V <sub>DD</sub> or tied to GND.				

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

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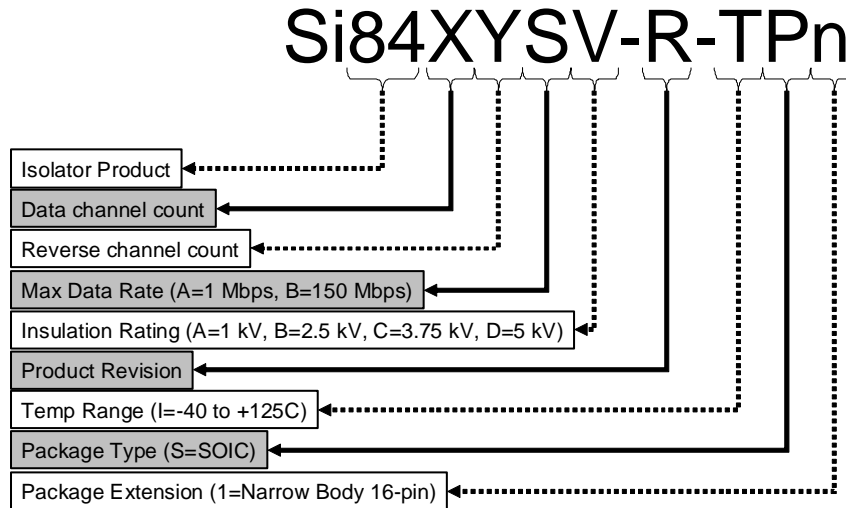
### 5. Pin Descriptions (Narrow-Body SOIC)



Name	SOIC-8 Pin# Si842x	Type	Description
V <sub>DD1</sub>	1	Supply	Side 1 power supply.
GND1	4	Ground	Side 1 ground.
A1	2	Digital I/O	Side 1 digital input or output.
A2	3	Digital I/O	Side 1 digital input or output.
B1	7	Digital I/O	Side 2 digital input or output.
B2	6	Digital I/O	Side 2 digital input or output.
V <sub>DD2</sub>	8	Supply	Side 2 power supply.
GND2	5	Ground	Side 2 ground.

## 6. Ordering Guide

Not all possible device configuration options and their corresponding ordering part numbers (OPN) are included in the Ordering Guide table. However, if there is a specific device configuration of interest that is currently not listed in the Ordering Guide table, please contact your local Silicon Labs sales representative, or go to the Silicon Labs Technical Support web page at <https://www.silabs.com/support/pages/contacttechnicalsupport.aspx> and register to submit a request for your specific device configuration and OPN.



**Figure 19. Ordering Part Number (OPN) Convention**

# Si8410/20/21 (5 kV)

## Si8422/23 (2.5 & 5 kV)

**Table 14. Ordering Guide<sup>1</sup>**

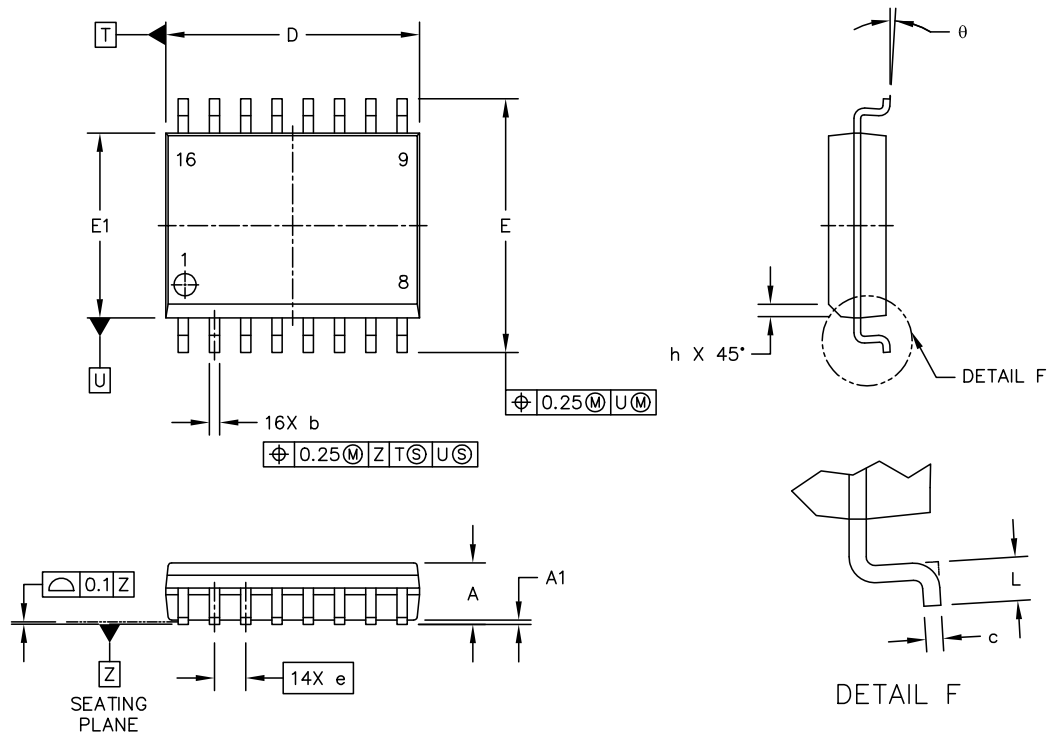
Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
Si8422AB-B-IS	1	1	1	2.5 kVrms	–40 to 125 °C	NB SOIC-8
Si8422BB-B-IS	1	1	150			
Si8423AB-B-IS	2	0	1			
Si8423BB-B-IS	2	0	150			
Si8410AD-A-IS <sup>2</sup>	1	0	1	5.0 kVrms	–40 to 125 °C	WB SOIC-16
Si8410BD-A-IS <sup>2</sup>	1	0	150			
Si8420AD-A-IS <sup>2</sup>	2	0	1			
Si8420BD-A-IS <sup>2</sup>	2	0	150			
Si8421AD-B-IS <sup>2</sup>	1	1	1			
Si8421BD-B-IS <sup>2</sup>	1	1	150			
Si8422AD-B-IS	1	1	1			
Si8422BD-B-IS	1	1	150			
Si8423AD-B-IS	2	0	1			
Si8423BD-B-IS	2	0	150			

**Notes:**

- All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.  
Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages.  
Moisture sensitivity level is MSL2A for narrow-body SOIC-8 packages.
- Refer to Si8410/20/21 data sheet for information regarding 2.5 kV rated versions of these products.

## 7. Package Outline: 16-Pin Wide Body SOIC

Figure 20 illustrates the package details for the Si84xx Digital Isolator. Table 15 lists the values for the dimensions shown in the illustration.



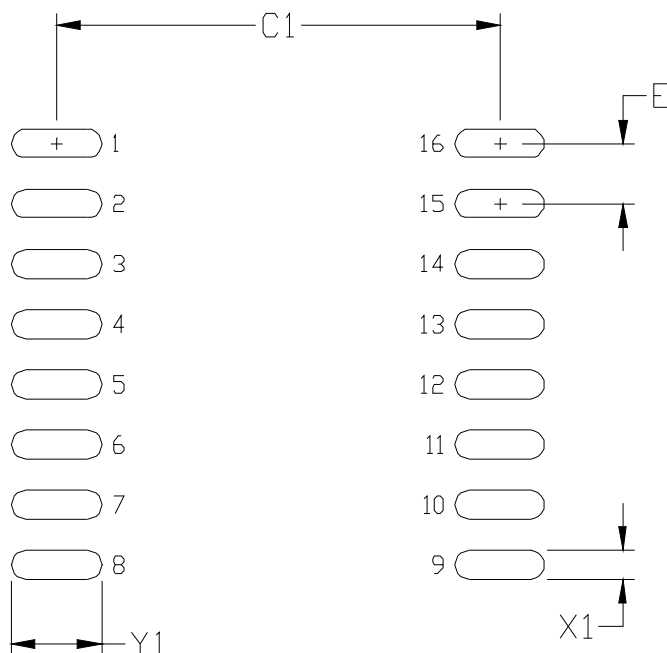
**Figure 20. 16-Pin Wide Body SOIC**

**Table 15. Package Diagram Dimensions**

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

## 8. Landing Pattern: 16-Pin Wide-Body SOIC

Figure 21 illustrates the recommended landing pattern details for the Si84xx in a 16-pin wide-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.



**Figure 21. 16-Pin SOIC Land Pattern**

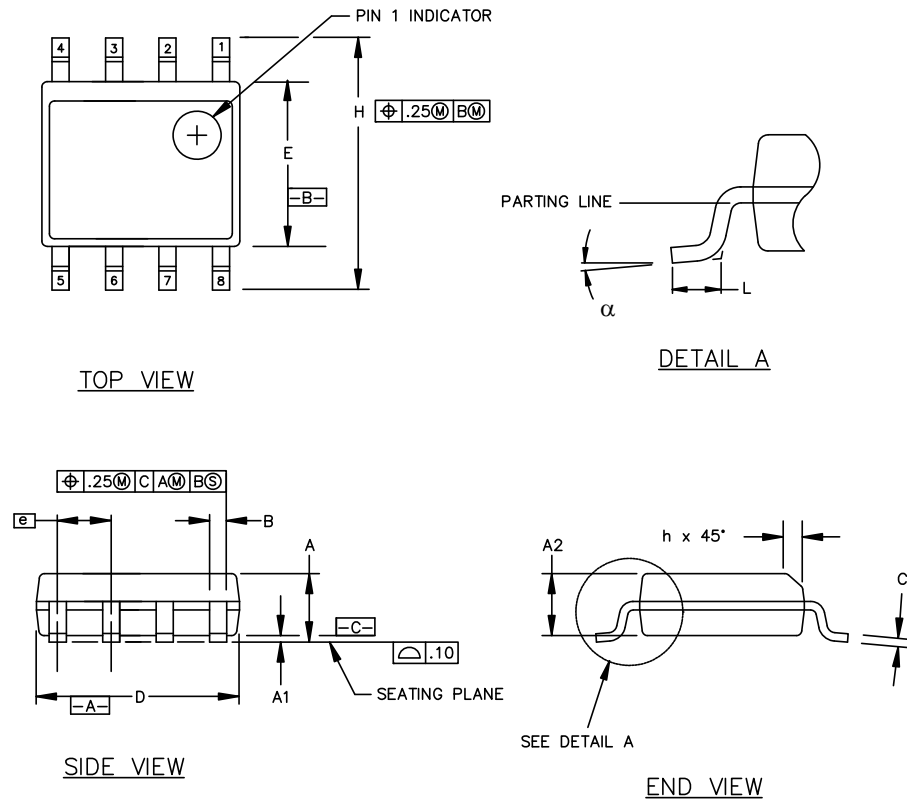
**Table 16. 16-Pin Wide Body SOIC Landing Pattern Dimensions**

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).</li> <li>2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.</li> </ol>		



## 9. Package Outline: 8-Pin Narrow Body SOIC

Figure 22 illustrates the package details for the Si84xx. Table 17 lists the values for the dimensions shown in the illustration.



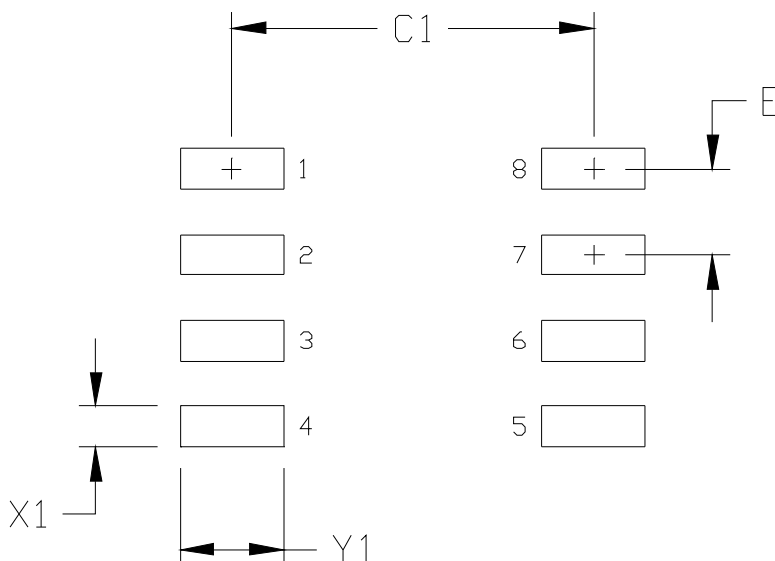
**Figure 22. 8-pin Small Outline Integrated Circuit (SOIC) Package**

**Table 17. Package Diagram Dimensions**

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

## 10. Landing Pattern: 8-Pin Narrow Body SOIC

Figure 23 illustrates the recommended landing pattern details for the Si84xx in an 8-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

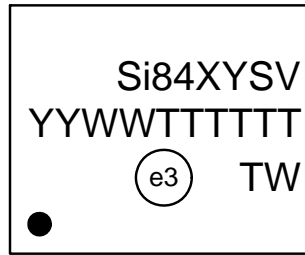


**Figure 23. PCB Landing Pattern: 8-Pin Narrow Body SOIC**

**Table 18. PCM Landing Pattern Dimensions (8-Pin Narrow Body SOIC)**

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).</li> <li>2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.</li> </ol>		

## 11. Top Marking: 16-Pin Wide Body SOIC

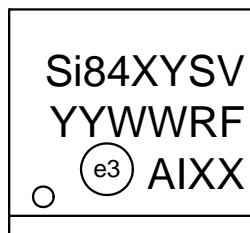


**Figure 24. Isolator Top Marking**

**Table 19. Top Marking Explanation**

<b>Line 1 Marking:</b>	Base Part Number Ordering Options  (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5 kV
<b>Line 2 Marking:</b>	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing code from assembly house.
<b>Line 3 Marking:</b>	Circle = 1.5 mm Diameter (Center-Justified)	"e3" Pb-Free Symbol.
	Country of Origin ISO Code Abbreviation	TW = Taiwan.

## 12. Top Marking: 8-Pin Narrow-Body SOIC



**Figure 25. Isolator Top Marking**

**Table 20. Top Marking Explanations**

Line 1 Marking:	Base Part Number Ordering Options  (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	R = Product (OPN) Revision F = Wafer Fab	
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	"e3" Pb-Free Symbol. First two characters of the manufacturing code.
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code.

**NOTES:**

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