Ferroelectric Memories

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In the past year it has become possible to fabricate ferroelectric thin-film memories onto standard silicon integrated circuits that combine very high speed (30-nanosecond read/erase/rewrite operation), 5-volt standard silicon logic levels, very high density (2 by 2 micrometer cell size), complete nonvolatility (no standby power required), and extreme radiation hardness. These ferroelectric random-access memories are expected to replace magnetic core memory, magnetic bubble memory systems, and electrically erasable read-only memory for many applications. The switching kinetics of these films, 100 to 300 nanometers thick, are now well understood, with switching times that fit an activation field dependence that scales applied field and temperature. Earlier problems of fatigue and retention failure are also now understood and have been improved to acceptable levels.

WITHIN A DECADE OF THE DISCOVERY OF FERROELECTRIC barium titanate ($BaTiO_3$) in several countries during World War II, it was widely recognized that the existence of robust, chemically stable, and relatively inert ferroelectric crystals offered an electrically switchable, two-state device. With such a device one could encode the 1 and 0 states required for the Boolean algebra of binary computer memories, and most of the large electronics research laboratories in the United States and Western Europe undertook the development of such devices. Some of the early work on ferroelectric memories in the 1950s was carried out by D. Young, M. Drougard, and R. Landauer at IBM, by R. C. Miller and A. Chynoweth at Bell Telephone Laboratories, by W. Merz at Bell and later at RCA, and by H. Stadler at Ford Laboratories. We review here the reasons effort was shelved in the mid-1970s as well as the reasons for its more recent resurgence (*1*).

Let us begin by summarizing the overall situation with regard to digital memories in the United States at present. There are now 14 generically different kinds of digital memories in use; Fig. 1 shows a log-log plot of access time versus cost per bit. The memories in use at present range from the slow, inexpensive devices (tape or disk) used for archival storage to the fast but expensive static random-access memories (SRAM) and the slightly slower dynamic RAMs (DRAM), whose availability in high-density chips (up to 1 Mbit) has permitted them to become dominant in the $8 billion per year computer memory market. The more expensive devices shown in Fig. 1A [plated wire, complementary metal-oxide semiconductor (CMOS) with battery backup, magnetic bubble memory, electrically erasable read-only memories (EEPROMs), and core] generally have some combination of attributes required for specific applications, particularly including nonvolatility (retention of memory when power is interrupted) and radiation hardness. The projected U.S. memory market will be greatly simplified in a few years, however, if ferroelectric RAMs become commercially available in high-density (for example, 256-kbit) devices with satisfactory operating characteristics and lifetimes (Fig. 1B). The intrinsic nonvolatility and radiation hardness of ferroelectric RAMs may greatly simplify the existing collections of computer memories, which will still include tape and disk systems for archival storage, as well as inexpensive high-density DRAMs and ultrafast SRAMs; however, most of the other memory devices now in use may be rendered obsolete by ferroelectric RAMs.

The radiation hardness of ferroelectric memories depends on this ability to function and retain information when the memories are subjected to intense x-rays, particle fluxes of charged ions, and neutrons, for both total integrated dosage and dose rates. A typical ferroelectric will withstand more than 5 Mrad of high-energy x-rays per square centimeter and an intensity of 10^{11} rad cm^{-2} s^{-1}, or 10^{14} 1-MeV neutrons per square centimeter, and will exhibit no single event upset and very little degradation in performance, as shown recently by Scott *et al.* (*2*). These properties may permit wide use of ferroelectrics in military aircraft as higher speed replacement for EEPROMs, magnetic bubble memory, and disk (Fig. 2). But one should not mistakenly assume that radiation hardness is of interest only to the military. Many civilian applications in space require radiation hardness; for example, a 1992 launch of a National Aeronautics and Space Administration satellite that must pass repeatedly through the Van Allen belt over several years of operation is at present likely to have core memory in its on-board computers. Replacement of core with ferroelectric RAMs could permit a significant improvement in weight, space, and power supply requirements while at the same time improving speed.

Basic Operation

A ferroelectric crystal of the tetragonal perovskite structure has two polarization states (Fig. 3). In lead titanate ($PbTiO_3$), for example, the Ti^{4+} ions occupy the centers of each cube; the Pb^{2+} ions are located at the corners; and O^{2-} ions are centered on each face of the undistorted lattice. In the distorted ferroelectric phase that is stable at room temperature, there is a net dipole (spontaneous polarization, P_S) of a few tens of microcoulombs per square centimeter produced primarily by the displacement up or down of the Ti^{4+} ions with respect to the other ions. In a crystal of $PbTiO_3$ that has not been specially prepared, we might expect to find regions in which the polarization is up and regions in which it is down, called "ferroelectric domains." However, if we apply a large electric field to the specimen (E_a of order a few kilovolts per centimeter), all the domains can be lined up in the same direction. More important for memory applications, we can switch the polarization of the

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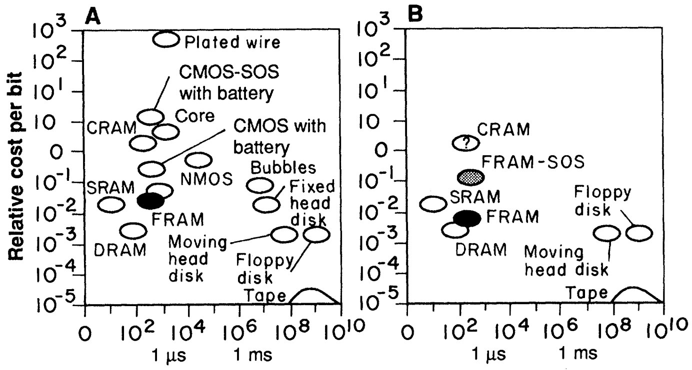

Fig. 1. Cost per bit versus access time for 14 generic types of digital memories (log-log plot): (**A**) 1988, FRAM (ferroelectric RAM) introduction; (**B**) projections for 1998; SOS, silicon on sapphire; NMOS, nitride metal-oxide semiconductor; CRAM, crosstie permalloy RAM. [Figure reproduced by permission of Leonard Schwee, U.S. Naval Surface Warfare Center, White Oak, MD] Vertical scale units are approximately 1 cent per bit.

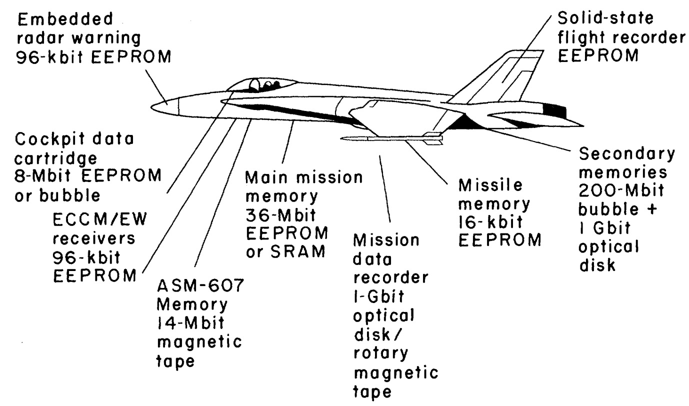

Fig. 2. Digital memories in use in a typical U.S. military aircraft; ECCM, electronic counter-command; ASM, antisubmarine system. [Figure reproduced by permission of Fedorak, Naval Air Defense Command]

entire crystal from up (+1) to down (0) by reversing the applied field. In a large single crystal this would require voltages of several kilovolts, which would be impractical for a commercial device; but for a thin film of order 100 nm thick, it requires only a few volts. Thus the development of practical ferroelectric memories is closely linked with progress in thin-film physics and engineering.

A basic characteristic of all ferroelectric materials is the hysteretic behavior relating polarization P and applied field E_a (Fig. 4). There is a nominal threshold (or coercive field E_c), above which the polarization changes sign. The two zero-field values $\pm P_r$ are equally stable. Thus, no applied field or voltage is required to maintain the memory, which is why the device is termed "nonvolatile." This bistable operation may be contrasted with the operation of memories such as nematic, liquid-crystal display devices, which relax back to a single favored state if the applied voltage is interrupted, or with Si DRAMs, which require a "refresh" voltage many times per second to maintain their stored information.

All of the early work on ferroelectric memories involved a simple design scheme (Fig. 5A). In this prototypical row-and-column array architecture, there is a ferroelectric cell at the intersection of each metallized row and column [or, in the parlance of computer engineers, at the intersection of each "word-line" (WL) and "bit-line" (BL)].

To write information in such a memory, short voltage pulses are applied along the rows and columns. Each voltage pulse is of value

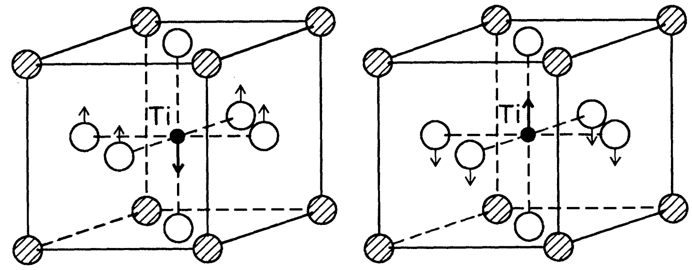

Fig. 3. Polarization states in a ferroelectric ABO_3 perovskite structure.

0.5 V_s, where V_s is the nominal switching voltage, given by $V_s = E_c d$, where d is the film thickness. Unfortunately, such a simple row-and-column address scheme is impractical for ferroelectric memories. The reason is that real ferroelectrics do not exhibit well-defined coercive fields or switching voltages; instead, E_c and V_s depend on the duration of the applied field (leaving the field on longer increases the probability of switching, even if E_a is much less than the nominal E_c), and on the history of the cell (E_c changes with time and with the number of times the cell has already been switched). In a typical ferroelectric the chances that a cell adjacent to the one being addressed (Fig. 5) will unintentionally also switch is 10^{-3} to 10^{-6}. In a large memory this would produce an unacceptably large error rate in writing information into the memory. In the jargon of computer memory designers, this problem was referred to as a "half-select disturb pulse threshold," which means that half the V_s could unintentionally disturb, or switch, stored data in a cell. In the 1950s and 1960s researchers attempted to solve this problem by finding the "perfect" ferroelectric, in which E_c is extremely sharp and well defined. Unfortunately, the best E_c behavior was found in KNO_3, whose hydroscopic nature makes it poorly suited for device processing. Much of the KNO_3 development was made at the General Motors Laboratories by Schubring *et al.* (*3*).

A better way to deal with the disturb problem is simply to circumvent it by designing around the problem; a more modern scheme is one in which each ferroelectric memory cell is electrically isolated from its neighbors by a pass-gate transistor (Fig. 5B). All modern ferroelectric RAMs use a variant of this transistorized array, typically either a six-transistor SRAM design or a more dense two-transistor DRAM layout.

A second problem associated with early research and development of ferroelectric memories is that they were fabricated from single crystals or ceramics. That resulted in thick cells and consequently unacceptably large operating voltages for practical commercial devices. It certainly precluded their integration into standard Si CMOS integrated circuits (ICs), for which the standard logic levels are 5.0 (± 10%) V. A particularly good example of a ferroelectric memory that might be regarded as state of the art in 1976 is that described by Wu *et al.* (*4*); this device was developed at the Westinghouse Research Laboratories. Wu *et al.* fabricated a 1-kbit RAM from bismuth titanate that could be optically read (nondestructive readout, which eliminates the fatigue associated with destructive electrical readout). In some ways it was a decade ahead of its time. However, it had a number of drawbacks. It was grown epitaxially on a crystalline substrate, which made it expensive. In order that it be read optically, it had to be thick (about 100 μm), which in turn necessitated a very large erase/rewrite voltage (around 100 V). And, despite this high voltage, it was rather slow to erase and rewrite (microseconds). The large operating voltage and consequent incompatibility with Si ICs was the primary reason why Westinghouse suspended development of this device from 1976 to 1988.

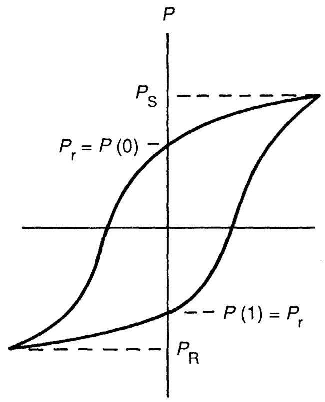

Fig. 4. Polarization P versus applied field E_a hysteresis curve in a typical ferroelectric; when a voltage is applied that changes sign with time (for example, 60 Hz). The polarization follows the solid curve.

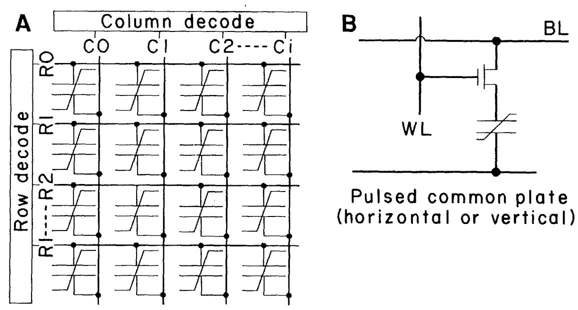

Fig. 5. (**A**) Raw array (row and column address scheme) ferroelectric memory. Half the nominal switching voltage is pulsed along a row and half down a column; the cell switches where the pulses intersect. (**B**) Pass-gate transistorized ferroelectric memory array.

Present Generation of Ferroelectric Memories

At present, the ferroelectric prototype memories being produced in the United States involve either sputtered films or sol-gel deposition. Other techniques can be used in some special cases (for instance, thermal evaporation for KNO_3), but expensive techniques such as molecular beam epitaxy (MBE) are not required. Moreover, the device can be fabricated with deposition of the ferroelectric film as a postproduction step on an Si IC that has been fabricated up to the first metal layer (bottom electrode) in a standard CMOS production facility. The ferroelectric film, top electrode, passivation layers, and so on can be put down in a rather small production facility without the need to rerun the IC through the Si line; this eliminates any possible contamination of an Si IC wafer line by the metal ions in the ferroelectric and greatly decreases the capital investment in such a ferroelectric RAM production facility.

Historically, the present generation of ferroelectric RAMs traces its origin to a few key development steps. In 1967 Schubring *et al.* (*3*) at General Motors investigated the properties of KNO_3 switching films that were thermally deposited in a simple manner. In 1973 Rohrer (*4*) found that KNO_3 films could be made sufficiently thin to permit 5-V operation (CMOS-compatible); that their operating temperatures were greatly enhanced above the bulk values (the Curie temperature of the film T_C = 196°C at thickness d = 70 nm, versus T_C = 127°C in bulk); and that they exhibited excellent fatigue and retention characteristics. Rohrer fabricated raw arrays of order 1 kbit. Somewhat later Nakagawa *et al.* (*5*) pointed out the need to develop sputtering techniques for lead zirconate-titanate (PZT) thin-film RAMs. Sputtered PZT is the basis for the ferroelectric 4-kbit RAM produced this year by Ramtron and TRW (*6*). Equally good PZT memories have been prepared by sol-gel deposition; this wet chemistry technique was pioneered by Payne at the University of Illinois (*7*) and Dey *et al.* at Arizona State University (*8*) and is utilized by Krysalis in its ferroelectric RAMs (*9*). Other wet chemistry alternatives to standard sol-gel deposition have also been investigated for PZT, particularly processes involving soap-like precursors and xylene solvents developed by Vest and Xu at Purdue University (*10*). In addition to PZT, switching in sputtered lead germanate thin films has been reported by Volz *et al.* (*11*), and barium bismuth titanate is known to be (*11*) extraordinarily fast, with 1-ns switching speeds extrapolated. The materials requirements for the ferroelectric film chosen are relatively modest; in particular, because most ferroelectrics have a polarization that corresponds to about 100 times the switched charge of an Si DRAM of the same area, it is not necessary to choose a ferroelectric material with a large spontaneous polarization: 0.1 to 1.0 $\mu C/cm^2$ is sufficient. This permits many non-oxide crystals to be considered as cell materials, in addition to the ABO_3 perovskites favored at present. The integration of ferroelectric thin-film arrays with CMOS Si integrated circuitry was first made by McMillan and his co-workers (*12*), an extremely important step in the development of commercially viable ferroelectric RAMs.

Optimum Thickness

In real ferroelectrics E_c depends strongly on the sample thickness, as first detailed by Callaby (*13*). For thick specimens E_c varies as d^{-n}, where n is a number between 1/3 and 1/2; this weak-field theory was developed by Kay and Dunn (*14*) and has been found to be valid for several materials, as shown by Scott *et al.* (*15, 16*). However, for thinner samples or higher voltages, a rather different dependence sets in, with n = 4/3. This was first reported by Hadni and Thomas (*17*) and is not completely understood. However, an analogous behavior is observed in magnetic thin films, where the dependence of critical magnetic field H_c jumps to $d^{-4/3}$ at a thickness where the domain wall structure changes for Bloch walls to Neel walls; the $d^{-4/3}$ behavior is termed Neel's law (*18*).

This change in the thickness dependence of E_c in ferroelectrics occurs near a thickness of 200 nm and has a profound practical effect on device construction. When we multiple E_c by d to obtain V_s, we find that the $E_c(d)$ dependence discussed above has two effects. It produces an optimum thickness near 250 nm, at which V_s is an absolute minimum (around 1.0 V, less than the GaAs device maximum of 3.0 V); and it defines a processing window of film thicknesses (from about 100 to 800 nm), within which V_s will be less than the 5.0-V CMOS logic levels for Si ICs. Within this processing window, the devices will be faster near the thin limit of 100 nm; in fact, as shown by Stadler (*19*), for a fixed 5.0-V driving voltage, the switching speed will vary as $d^{-3/2}$, so that a 100-nm film will be approximately eight times faster than a 400-nm film. Figure 6 shows the dependence of V_s on d. The $V^{-3/2}$ dependence of switching time t_s has been shown elsewhere (*15*). (The theoretical dependence of $t_s = A\,E^{-3/2}$, where A is a constant, predicts a $V^{-3/2}$ voltage dependence at constant thickness and a $d^{3/2}$ thickness dependence at constant voltage for these memory devices.)

Current Transient Shapes

In most ferroelectric memories one reads the memory cell electrically and destructively by sensing the current transient that is delivered to a small (10-ohm) load resistor when an external voltage is applied to the cell. Application of a positive switching voltage $+V_s$ to a cell initially stored in the negative ($-P_r$) state will result in a switching of charge given by $Q = A_o \epsilon E_a + A_o\, dP/dt$, where A_o is the area of the ferroelectric cell, ϵ is its dielectric constant (of order 1300 for PZT), and P is the polarization of the ferroelectric (of order 30 $\mu C/cm^2$ for PZT). This current transient thus consists of a linear dielectric response plus a displacement current; because the ferroelectric materials used are highly insulating (resistivity $\rho = 10^{11}$ ohm-cm is typical), the ohmic current is negligible. The sense amplifiers and associated circuitry used in the ferroelectric RAM must be capable of discriminating between the "switching" current described above and a "nonswitching" current transient. A nonswitching current transient is the response to a positive applied voltage $+V_s$ by a cell already stored in a positive $+P_r$ state. In this case $Q = A_o \epsilon E_a$. For the first 10 to 20 ns the current transients are indistinguishable; but by 30 ns a discrimination of 200 mV can be sensed between switching and nonswitching pulses, which makes reading the difference between 1 and 0 in the memory a relatively easy matter for the sense amplifiers and associated circuitry.

In most ferroelectrics the actual switching kinetics consist of three steps: (i) inhomogeneous nucleation at the electrode surfaces; (ii) needle-like growth of domains parallel or antiparallel to the applied field, normal to the film surface (the so-called "forward growth regime"); and (iii) sideways spreading out of the new domains within the plane of the film. Typically the last step is the rate-limiting step in the process, and it is this step that yields the $t_s = A E^{-3/2}$ dependence of switching times. Of course, in general, these three steps may proceed simultaneously.

Ishibashi and his co-workers have produced a theoretical model of such ferroelectric switching (*20*) in which three fitting parameters are a characteristic t_s, the dimensionality of domain growth D, and P_S. With this model very good fits of experimental current switching transients have been made by Dimmler *et al.* (*21*) and by Scott *et al.* (*22*). Notable in these results is the fact that the t_s so derived fits a simple activation-field dependence: $t_s = t_o \exp(\alpha/E_a)$ with an activation field α that is proportional to reduced temperature $(T_C - T)/T_C$. The fact that t_s scales in this way with voltage and temperature permits all the data at different voltages and temperatures to be plotted on a single universal curve, which greatly simplifies device modeling for the RAM design engineer (a lookup table can be used for SPICE modeling or related models).

Fatigue

A principal drawback to early ferroelectric memories was the fact that the amount of switched charge decreased with use. Typically Q degraded to 50% of its initial value after 10^6 read/erase/rewrite cycles. This is a profound problem for ferroelectric memories because they are normally designed with destructive electrical readout. Thus, a limit of 10^6 erase/rewrite operations is also a limit of 10^6 read operations. This is not sufficient to provide a competitive memory device; for example, a EEPROM may typically permit only 10^3 erase/rewrite operations (which are slow and inconvenient), but it permits 10^{15} read operations. If ferroelectric memories are to become competitive with EEPROMs, either they must be improved to withstand at least 10^{12} erase/rewrite operations or they must have qualitatively different nondestructive read operations.

Fatigue in ferroelectric devices has been studied for many years. Several mechanisms are well known at this point. Plessner (*23*) has described the role of 90° domains, which are a special problem in pseudo-cubic materials such as PZT; this kind of analysis has been continued by Ikegami and Ueda (*24*) and by Dederichs and Arlt (*25*). A different mechanism in PZT was first observed by Plumlee (*26*) at Sandia Laboratories; he found that switched charge decayed logarithmically with the number N of read/erase/rewrite cycles and that, coincident with this degradation, dark dendritic filaments could be observed by optical microscopy to be extending out from the electric interfaces into the ferroelectric film. We believe that these dark regions arise from O-deficient conducting regions of the PZT. A voltage of 5 V over a 100-nm film corresponds to 500 kV/cm, at which impact ionization of the Ti^{4+} ions can occur initiated by electrons from the electrode. This converts the Ti^{4+} to Ti^{3+} and generally replaces a nearby O^{2-} ion with a trapped electron. Modeling of this process by Scott *et al.* (*27*) and by Duiker and Beale (*28*) permits an accurate fit of the shape of the $Q(N)$ fatigue curves. It also explains a curious effect observed in partially fatigued ferroelectric memories. After many (10^8 to 10^9) read/write cycles, most ferroelectric memories become faster. This effect has a simple explanation. The switching occurs not between external electrodes spaced d apart but between the conducting filaments of O-deficient PZT material. Thus, the 5.0-V driving voltage is delivered across a gap that grows smaller with time; the resulting field is therefore higher ($E_a' = V_s/d'$), and hence the switching time is faster. (The amount of switched charge is also smaller.)

Mobile ions, both O^{2-} vacancies and other substitutional impurities, contribute to fatigue by collecting at grain boundaries and other defect sites and pinning domains. It is possible in both KNO_3 and PZT to "depin" such trapped domain walls by applying a voltage higher than the usual V_s of 5 V but less than the breakdown voltage. Scott and Pouligny (*29*) found that in KNO_3 10 V would restore the hysteresis loop squareness to nearly its original virgin state. This depinning procedure works well in sol-gel PZT but not in sputtered PZT; the reason is not well understood but presumably is due to greater homogeneity and smaller grain sizes in the sol-gel material. The fact that PZT memories can be restored to near virgin characteristics with a single 10-V pulse after 10^6 destructive read cycles suggests that one can significantly delay fatigue in such memories by programming such restore pulses into the memory design to occur periodically in normal operation.

The charge conversion from Ti^{4+} to Ti^{3+} discussed above can be ameliorated by doping. This led to a great deal of complex materials science, particularly at the IBM San Jose laboratory in the 1970s. In work begun by Chapman (*30*) and Atkin (*31*), very detailed studies of fatigue and retention improvement in PZT materials were made. Some of these involved intentional doping with various metal ions, for example, Fe, Mn, and W. These techniques do result in improved fatigue performance. At present both Ramtron and Krysalis claim 10^{12} read/write destructive cycles for their PZT memories without significant degradation (*6*). These cycles are not simple alternating voltage sequences (+, −, +, −), which are known to give overly optimistic endurance estimates, but a more complex sequence (*2*).

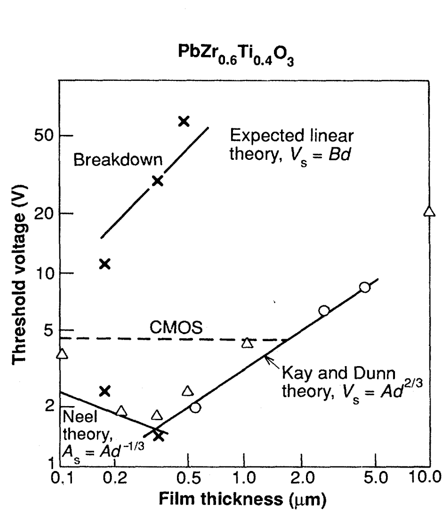

Fig. 6. Switching voltage $V_s(d)$ versus film thickness d for KNO_3 (circles and crosses) and PZT (triangles). The curve for the Kay and Dunn theory is based on (*14*). The curve for the Neel theory is based on (*18*).

Retention

In contrast to fatigue, which is defined as a loss of switched charge owing to repetitive destructive reads, retention is simply a matter of shelf life. Retention failure means that the stored charge has decreased to a level where the + or − state of polarization cannot be reliably sensed. In general, charge does not leak off ferroelectric cells, which are simply very small capacitors. The internal decay of stored charge is extremely small (typically it would take 30,000 years for the stored charge to flow ohmically through the film to a point where 50% was lost). However, under some circumstances the stored charge in a ferroelectric film can disappear, apparently very quickly. This is especially true when radiation is present. Scott *et al.* have recently shown (*2*) that this is caused by space charge effects well understood in electrets. If a ferroelectric film or a nonferroelectric electret is charged up with electrodes that are partially blocking or that trap charge at the interface, the effect can be that the stored charge Q actually reverses sign after a few hours or days, as first discovered by Eguchi (*32*). In a ferroelectric memory this can occur when the cell receives its write pulse and can give rise to an apparent rapid loss of retention. This effect can be acute when the cell is subjected to intense radiation (*2*), but the problem is minimized if the cell architecture is such that cells are not stored in short-circuited states. Under optimal conditions, retention in ferroelectric memories exceeds 10 years.

Direct-Current Breakdown

It is possible to design ferroelectric RAMs that have nondestructive electrical readout. The primary drawback of such designs is that they require that individual cells be subjected to a constant voltage (as great as 5 V) rather than open-circuit conditions. Such a constant voltage often produces what has been termed "time-dependent dc breakdown." That is, although the nominal breakdown voltage for a ferroelectric memory cell may be 45 V for a single 30-μs voltage pulse, application of 5.0 V, or even 2.5 V, for a very long period can produce breakdown (electrical shorting). This phenomenon is poorly understood but is viewed as arising from slow diffusion of mobile ions. If it could be completely eliminated, it would be possible in the immediate future to fabricate ferroelectric RAMs with 10^{15} read/write cycles, with the use of a nondestructive readout with cells maintained continuously at 5.0 V. In order to make ultrapure ferroelectric memories with virtually no mobile ions, it would be extremely useful to fabricate ferroelectric memories by MBE techniques; at least one group has begun to do so (*33*).

Application to GaAs Technology

Although the primary development of ferroelectric memory devices has been for Si metal-oxide-semiconductor field-effect transistor (MOSFET) structures, this technology is also applicable to JFET (junction FET) structures, including GaAs devices. Zuleeg and Geideman (*34*) have investigated the integration of ferroelectrics onto GaAs, as has McMillan (*35*). It is natural to combine GaAs, which has both superior speed and radiation hardness, compared with Si, and ferroelectric memory cells that offer superb speed and radiation hardness. In addition, because of the oxidation characteristics of Ga and As, it appears unlikely that a GaAs EEPROM will ever be developed; hence a GaAs-ferroelectric RAM may fill the EEPROM niche in GaAs technology. The 3.0-V operating level of GaAs ICs is not a problem for ferroelectric films.

Other Problems

Relatively little attention has been paid to the optimization of electrodes and electrode interfaces. Typically, Pt or Pt alloys are used. Flash-evaporated Au is known to produce problems. Electroding (the deposition of material by current film) affects retention, as shown by detailed studies at the IBM San Jose laboratory (*31*). No detailed studies of electroding or of the electrode-ferroelectric interface have been published.

Finite Size Effects

It is clear that the phase diagrams published for bulk ferroelectrics can be significantly in error when applied to thin films. In KNO_3, as discussed above, T_C is 69 K higher for d = 70-nm films than in bulk. Similar size effects are well known experimentally (*36*) and theoretically (*37*) in other materials, both for thin films (*38*) and small particles (*39*). For ferroelectrics a detailed model has been given by Duiker and Beale (*28*); this model is based on earlier work by Tilley and Zeks (*40*), Lubensky and Rubin (*41*), and Mills (*42*). One prediction, that T_C varies nearly linearly with $1/d$, seems to be verified experimentally. A second prediction, that bulk first-order transitions at T_C can become continuous for sufficiently small thicknesses d, is also in accord with data on KNO_3 (*27*). Because E_c increases more slowly (*14*) than linearly with reciprocal thickness for ferroelectric films, some ferroelectrics that will not switch in bulk actually made good thin-film switches.

State of the Art and Prognosis

Table 1 gives a set of device parameters for ferroelectric memories as of 1 June 1989. These parameters are already sufficiently good to permit incursions into the EEPROM and magnetic bubble market. In March 1989 the Strategic Defense Command requested proposals for approximately $20 million in research and development for prototypes of both low-density (4-kbit minimum) and high-density (64-kbit minimum) ferroelectric RAMs. It would appear that prototypes will be marketed by more than one company by the end of 1989.

The short-term prognosis is for limited replacement of EEPROMs by ferroelectric RAMs, primarily in military applications that require nonvolatile radiation-hard devices. Several long-term predictions in trade journals (*43*) predict nearly $1 billion in sales of ferroelectric RAMs by 1992.

From a scientific point of view, these new devices should permit quantitative testing of finite size effect theories, of models of

Table 1. Optimum device parameters for ferroelectric memories.

Parameter	Value
Minimum cell size	2 by 2 μm^2
Read time	10 ns
Erase/rewrite time	10 ns
Operating temperatures	−100° to +300°C
Minimum access voltage	1.0 V
Activation field	120 kV cm^{-1}
Breakdown voltage	40 V
Fatigue to 50% Q	10^{12} cycles
Retention	5 years (real time)
Radiation hardness	5 Mrad cm^{-2} (x-rays)
	10^{11} rad cm^{-2} s^{-1} (x-rays)
	10^{14} cm^{-2} (neutrons)

switching at extremely high speeds (about 1 ns), and of the role of mobile ions in fatigue, retention, and dc breakdown. Particularly interesting in this regard is the application of well-developed theories, such as those of Fridkin (*44*), for inhomogeneous fields in ferroelectric films that are slightly conducting.

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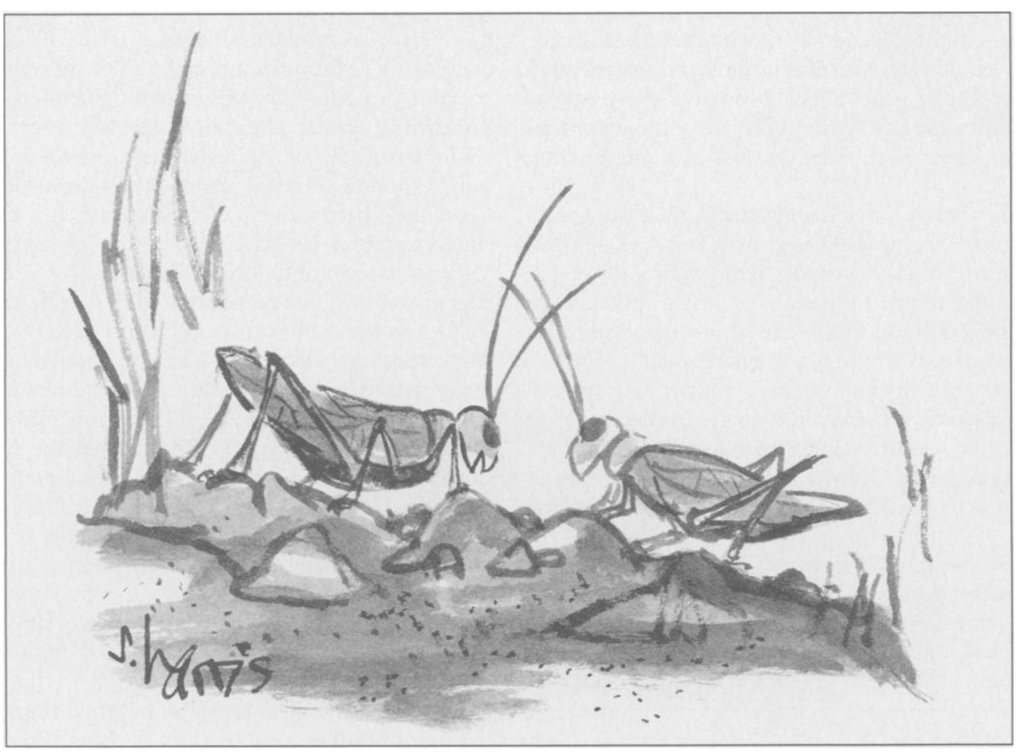

"Believe me, they're not expecting us. We're 387-year locusts."