New Ways to Make Microcircuits Smaller

Making integrated circuits has always been more art than science, but as miniaturization proceeds unabated more science is needed

"Round about the cauldron go;
In the poison'd entrails throw.
Toad, that under cold stone
Days and nights has thirty-one
Swelt'red venom sleeping got,
Boil thou first i' th' charmed pot."

Shakespeare said it first, but the thought of trying a little magic has probably crept into the head of more than one manager of a microcircuit production line. Despite the fact that the semiconductor silicon is likely the most intensively studied and well understood solid material on earth, when it comes to making integrated circuits in large quantities, the pure white gowns and caps of production line workers might as well be covered with moons and stars of the type that bedeck the robes of a conjuror. As microelectronics now enters the very large scale integrated circuit (VLSI) era in which a whole new round of miniaturization gets under way, the technical challenges faced by microcircuit manufacturers are getting even stiffer. Not only are new microfabrication instruments and techniques required, but a more scientific understanding of the materials and processes used in making integrated circuits with components having features approaching 1 micrometer in size is also needed.

This is the third of a series of Research News articles on microelectronics.

Given the intricacy and ultraminiature scale of integrated circuits, it would be surprising if their manufacture was a completely scientific undertaking. An analogy from Patrick Haggerty, the former chairman of Texas Instruments who helped guide the company from a small geophysical exploration firm to a giant in the microelectronics world, illustrates the magnitude of the problem. A pocket calculator chip made by Texas Instruments has about 6000 transistors on it, somewhat more than the number of city blocks in Manhattan. Said Haggerty, "Each of these devices must be interconnected by a thin path of aluminum deposited on its surface. . . . The entire electronic device will be useless if there is a fracture in the metal at any one point. This would be like shutting down Manhattan completely if there is a crack wider than one foot across any street."

It is mainly when large quantities of microcircuits must be produced that art overtakes science. The secret of success in semiconductors is to be able to make literally millions of devices without a high proportion of the circuits being defective. But the causes of defects are not always understood nor are they easy to control when they are understood. Airborne dust particles, for example, are a major cause of defects because they randomly settle on delicate circuit patterns during the photolithographic process that imprints features onto the silicon surface. The only means of controlling such particles is by filtering the production room air so that it contains no more than 100 particles 0.5 micrometer or larger in diameter per cubic foot, by requiring workers to wear caps, masks, gowns, and booties, and by protecting work surfaces with laminar flow air systems.

Contamination of the silicon by impurities is a significant problem because microcircuits are heated, sometimes to well over 1000°C, several times during the fabrication process. At such temperatures, impurities on the silicon surface picked up during processing easily diffuse into the material, thereby altering its electrical properties. Controlling contamination is especially difficult if the identity of the impurity or its effects are not known.

Murray Bullis and Robert Scace of the National Bureau of Standards recall that in the early 1950's when solid state electronics was just getting started and transistors were made from germanium rather than silicon, there was an impurity called deathnium "because it killed all the devices it got into." Deathnium was eventually identified as copper, a rapidly diffusing impurity that is present, among other sources, in tap water in more than sufficient quantities to be a problem. Now, with the more stringent requirements on silicon quality imposed by VLSI microcircuits, carbon, which is always present in newly grown crystalline silicon at concentrations of at least 1 part per million, is becoming the whipping boy. "Today," says Bullis, "we really don't know much more about the influence of carbon on silicon than we did 25 years ago about copper on germanium."

At present, fabrication of an integrated circuit involves a sequence of processes that may be repeated a dozen or more times before a circuit is completed. The manufacture of a microcircuit begins with a thin wafer that is either 7.5 or 10 centimeters in diameter and is made from very high purity silicon.

To make a functioning circuit, however, requires modifying the silicon. Perfectly pure silicon is almost an insulator, but certain impurities called dopants added in amounts of from 10 to 100 parts per million make silicon conduct electricity. There are two kinds of dopants, those that add free electrons and produce so-called n-type silicon, and those that soak up bonding electrons in the silicon and leave behind electron vacancies or "holes" that act like positively charged carriers of electrical current in so-called p-type silicon. A transistor consists of several alternating n- and p-type regions of silicon and separate electrical contacts to these regions by strips of metal or other conducting material. An integrated circuit consists of thousands of transistors (and also diodes, resistors, and capacitors) made of doped silicon, all connected by the appropriate pattern of conductors to create the computer logic, memory, or other type of circuit of interest. Hundreds of microcircuits can be made on one wafer.

The first processing step is to form a thin layer of silicon dioxide over the entire wafer. More than any other factor, the ease of forming the protective oxide coat is what makes silicon the premier material for microcircuitry. After oxidation, photolithography is the second process in the microfabrication sequence. A solution containing an organic polymer is spun onto the oxidized wafer. After heating, a tightly adhering polymer coat is left. Some polymers are normally in-

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soluble in a developer solution but become soluble after exposure to light; others behave in the reverse manner. Ultraviolet light shining through a mask containing a circuit pattern determines where the polymer will be exposed. The polymer (called a photoresist) that is left after developing and drying is impervious to acid etching solutions.

Etching is the third process in the sequence. The purpose of etching is to eat away the oxide coating in places where the wafer is not covered by photoresist. This process exposes the silicon surface in those areas where it is to be doped with impurities.

The fourth process is the introduction of the doping impurities that convert silicon into n- or p-type semiconducting material. Doping is most often carried out by heating a wafer in a furnace in which the atmosphere is saturated with the appropriate impurity element and in which the temperature can reach 1100° to 1200°C. In recent years, ion implantation, in which a small acclerator propels a beam of impurity ions directly into the silicon, has become a widely used alternative doping technique.

One measure of the complexity of the processing is the number of masks needed. In a talk last December at the International Electron Devices Meeting in Washington, D.C., Dean Toombs, a Texas Instruments vice president, noted that the most popular integrated circuits used six to nine masks, although more exotic technologies require up to 15. The trend, moreover, is for all types of VLSI microcircuits to use more masks than previous generations did.

The accuracy that must be maintained in the locations of components of a microcircuit is of a very high order. Alignment of a mask in the photolithography process with features imprinted by previous masking steps must be done to better than 1 part in 10^5, which is comparable to a navigator keeping a ship within 500 feet of its course over the length of a 10,000-mile voyage.

While it all sounds crisp and clear-cut, the complexity and precision notwithstanding, numerous factors can intervene to inject a strong "art" flavor to an otherwise scientific enterprise. Some of these were reviewed by Robert Keyes of IBM's Yorktown Heights laboratory at a National Science Foundation workshop on microstructures technology:*

- The thicknesses of the oxide and photoresist layers, which are each about 1 micrometer or less, must be uniform over the 10-centimeter-diameter wafer. If, for example, the oxide is not the same thickness everywhere, some parts may not be etched completely through, while other parts may be overetched so that features are larger than planned.
- Because of diffraction effects, the edges of features in the mask are not sharply exposed in the photoresist. During development of the photoresist, material is removed around the edges of features because of partial exposure. This has two effects: the size of the feature depends on the development time, and a sloping wall in the resist is produced. The thin resist at the bottom of the feature may not protect the underlying oxide during etching, further adding to uncertainty in feature size.
- The resist may not adhere perfectly to the oxide. During development of the photoresist, part of the material may be lost around feature edges as the developer invades the interface between the imperfectly adhering layers, thus exposing an undetermined amount of the oxide layer to the etchant.
- The time and temperature of the diffusion step is critical because dopants diffuse laterally in the silicon under the oxide as fast as they go vertically down into it. Moreover, an imperfect silicon-oxide interface can cause enhanced diffusion laterally at the silicon surface, and defects in the silicon itself can cause the dopants to diffuse nonuniformly.
- The most common material for contacts and interconnections is aluminum. If the walls of the protective oxide are too sharply vertical, the evaporated aluminum layer will be quite thin over the walls. The electrical current density in such thin regions can become so large that it physically moves aluminum atoms (a phenomenon called electromigration). If enough atoms are moved, a discontinuity in the aluminum layer results and electrical contact is lost.

Keyes summed it up by saying, "Seemingly identical apparatuses and starting materials often yield different results. Recipes must be carefully followed, with little understanding of which aspects of a process are critical or what contaminants are important, and why." Small wonder that a cry for a little "eye of newt and toe of frog" to be added to the pot might occasionally be heard. Finding out why one company's production line is successful with high yields (a high yield for new products can be 10 percent defect-free chips) while another's is low can be a perplexing business, especially when customers are wondering why a new widely advertised part is not yet available. The latest example of yield problems is the super-dense computer memory chip called a 64 K RAM (a random access memory that can store 65,536 bits of information). Two years ago, Japan's largest computer company, Fujitsu, was the first to announce that it was producing a 64 K RAM. Today, several American companies have made similar announcements, but only IBM is producing the part in quantity (for its own internal use).

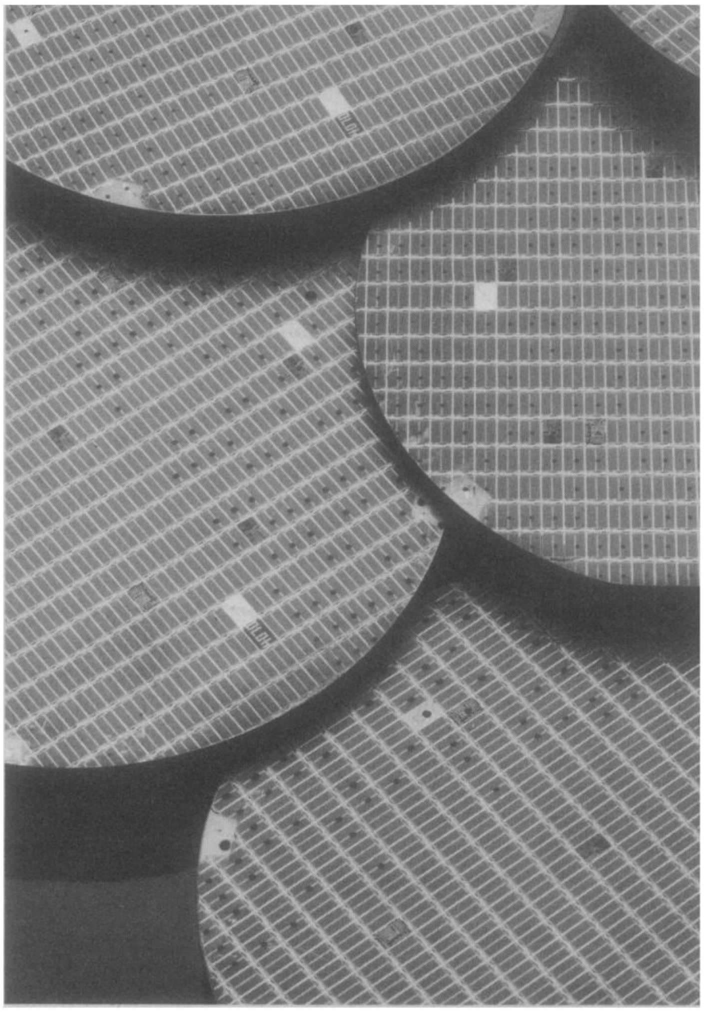
Today's most densely packed microcircuits are called large scale integrated circuits (LSI). Computer memory chips and microcomputers are typical LSI products. The smallest features in LSI circuits are usually the width of the metal interconnections, now at 3 micrometers and heading toward 2. The microfabrication processes discussed so far are probably not adequate for microcircuits with linewidths of 2 micrometers or less, according to George Heilmeier, a vice president at Texas Instruments. When the company was designing its version of the 64 K RAM, development proceeded in parallel of an entirely new fabrication facility with automated wafer handling in a dust-free environment and with advanced optical lithographic and etching equipment. To make integrated circuits with true VLSI dimensions (linewidth of 1 micrometer or less) may require even more radical departures from current practice. When individual components may eventually be 10 to 20 times smaller than they now are, margins for error will be comparably reduced. The leading cause of defective LSI circuits, for example, is pinholes in the oxide layer. Near certain electrodes the oxide can be as thin as 600 angstroms. In the same device scaled to VLSI dimensions, the oxide would be 150 angstroms thick. Thus, there will be less room for reliance on recipes that have worked in the past and more need for a firmer scientifically based fabrication process. Some of the new fabrication technologies are already or shortly will be widespread. Others will come along in the 1980's as they are shown to be cost effective.

Among the most widely discussed new processing technologies designed to get the microcircuit industry into VLSI are methods of lithography. Murray Lepselter of Bell Laboratories and Alec Broers of IBM reviewed the options at the NSF microstructures workshop. For photolithography, the fundamental limit in resolution is twice the wavelength of the ultraviolet light. Researchers are experimenting with 2600- to 2000-angstrom deep ultraviolet radiation in place of the 4000-angstrom near ultraviolet of com-

*NSF Workshop on Opportunities for Microstructures Science, Engineering, and Technology, Airlie House, Airlie, Virginia, 19-22 November 1978.

mercial instruments. The problem is that the resolution is only one of the areas of concern. Others include depth of field and field width. If the depth of field is shallow and the resist layer is thick or the wafer is not flat, the mask pattern will not be in focus over the entire wafer. The size of the pattern that can be kept in focus (field width) tends to be inversely related to the resolution, so that a pattern smaller than the wafer must be used, which is then reexposed several times to cover the entire wafer.

Optical components also present difficulties because glass is not transparent to such short wavelengths. The quartz alternative now being tested does not transmit below 2000 angstroms, which sets the apparent ultimate limit for photolithography. The best commercially available instrument can replicate features as small as 1.25 micrometers. Engineers are divided on the likelihood of high-volume, production-line machines (as opposed to laboratory curiosities) going much below this to the ultimate resolution of about 0.5 micrometer.



Silicon wafers containing computer memory chips. The chips have been tested and in a substantial fraction of cases been found to be defective (chips marked with black dots). [Source: Schlumberger Limited]

To reach below 1 micrometer, it may be necessary to use x-rays or beams of electrons or ions. X-ray lithography would work in much the same way as photolithography and thus is the logical next step: a beam of x-rays shining through a mask would expose a resist material. The intrinsic resolution could be quite high because of the short x-ray wavelength (soft x-rays with wavelengths ranging from about 4 to 50 angstroms are being investigated). But certain other difficulties limit the practical resolution to about 0.1 micrometer.

One of the factors is that x-ray resists do not work the same way as photoresists, whose solubility in developing solutions is determined by structural changes in the resist induced by absorption of light by chemical bonds. In the case of x-rays, changes in the resist follow from energy deposited by free electrons liberated by the absorption of the x-rays. The electrons can travel laterally in the resist and thereby expose a wider area than that which absorbed the x-rays.

A difficulty that further complicates x-ray lithography is that resists take too long to be exposed to be practical for production lines when conventional x-ray tubes are used as sources. Sources with greater brightness would shorten exposure times. Alternatives being considered are electron storage rings that produce synchrotron radiation, high-energy laser or electron beams to produce intense bursts of x-rays when the beams vaporize a target material, and high-intensity, water-cooled, rotating anode tubes. Hewlett-Packard's Donald Hammond thinks that once the market potential of x-ray lithography becomes clear, a fair amount of ingenuity in developing new x-ray sources will be stimulated.

Use of a computer-controlled electron beam eliminates the need for a mask altogether, since all the information about the pattern is contained in the computer's memory to be retrieved for steering the beam to the places where an electron-sensitive resist is to be exposed. So far, only IBM is using so-called direct writing by electron beam for the production of microcircuits. Observers give the impression that eventually such machines will be widely used. A 4-year-long, \$310-million VLSI project just completed in Japan had as its primary goal the development of this technology and a number of electron beam systems were built as a part of the program.

A principal problem with electron beam lithography is cost. For x-ray lithography, says Hammond, "the equipment expense may be in a range similar to optical equipment, and, if the technical problems can be solved, it's a distinct advantage." But electron beam systems are expected to sell for \$1.5 million to \$2 million, as compared to \$600,000 for the most costly optical systems. Moreover, the time required to steer an electron beam over an entire wafer may be ten times that needed for the exposure of a pattern by photolithography. Thus, the effective capital cost per wafer produced could be 40 times as great with an electron system. The speed of electron beam writing may be increased severalfold with more research on brighter electron sources and more sensitive resists, but the cost means that the systems will not be used until the last drop is squeezed out of optical lithography.

Another reason for sticking with photolithography is familiarity; the technology is well worked out. Electron-sensitive resists work the same way as x-ray resists, except that scattering of the high energy electrons by atoms in the resist is much more violent than for the lower energy electrons produced by x-ray absorption, so that the resolution obtainable is normally poorer than with x-rays. (Laboratory experiments with electrons have resulted in very small feature sizes, but for volume production of microcircuits a resolution of about 0.3 micrometer is considered the best that can be achieved.) The properties of a resist that are to be optimized are sensitivity or speed (for quick exposure), contrast (for features with sharp edges), and resistance to the electron scattering effect (for high resolution). Comparable specifications have long been fulfilled for photolithography; resists are still an active area of research for electron beam lithography.

The highest resolution lithographic technique may be one that has hardly been explored: ion beam lithography. Lepselter concluded that a direct-writing ion beam system could achieve a resolution of less than 0.1 micrometer because the ions, much heavier than electrons, would not scatter far in the resist. A recent experiment at Cornell University's National Research and Resource Facility for Submicron Structures has verified that ion scattering is not a serious limitation. Source brightness has been even more a problem for ion beams than for x-rays and electron beams. But recently new liquid metal sources for ion beams have been developed that are 10,000 to 100,000 brighter than older sources. Robert Seliger and his co-workers at Hughes Research Laboratories, in particular, reported in early 1979 on a high-intensity scanning ion probe that has drawn new attention to this intriguing alternative. An extra feature of ion beams is that they can be used to etch silicon dioxide directly, so that in some cases the entire lithography process can be bypassed by steering the ion beam across the wafer in the desired pattern. Although groups at both IBM and Texas Instruments have used electron beam lithography to make LSI demonstration microcircuits with 1 micrometer features, no system for ion beam lithography has been built.

While the focus has been on new lithographic technologies, Texas Instruments' Heilmeier emphasizes that, "There is more to reaching sub-two-micron geometries than just the ability to make patterns of those dimensions. You also have to be able to do the other processing steps and the quality of the silicon starting material has to be greatly improved." One kind of improved processing is the replacement of wet etching with acid solutions with a dry process. There are several contenders, but the one getting almost as much attention as lithography itself is called reactive ion etching. The sample is placed in a chamber with an atmosphere of chemically reactive carbon-fluorine compound at a low pressure of about 0.1 torr (1.3×10^{-4} atmosphere). An electrical discharge creates a plasma of reactive radicals (ions) with an energy of a few hundred electron volts. The radicals vertically strike the surface, where they react to form volatile species that are removed by the low pressure. Because of the moderate ion energy, the process is anisotropic; that is, the etching is mainly in the vertical direction, not laterally under the resist as with acid etching solutions. Thus, the edges of features are sharply defined and are of the size expected. A related technique called plasma etching that is less anisotropic is being used by some manufacturers already.

The quality of the silicon starting material is critical for VLSI microcircuits. To cite just one example from a recent National Research Council report, consider the electrical resistivity of silicon.† Ideally, the resistivity of a wafer should be the same everywhere (before processing begins). The NRC report estimates that VLSI requires material with at most a 1 percent variation in resistivity from point to point in the wafer, but the best commercially available silicon exhibits a 5 to 10 percent variation. Moreover, point out Bullis and Scace of NBS, "In many cases the tools to measure properties to the accuracy required by VLSI are yet to be developed. We are dealing with very small variations in a minute amount of material."

Formation of metal interconnections in VLSI microcircuits also presents severe materials requirements. The traditional contracting metal, aluminum, tends to dissolve silicon. Some solubility helps to ensure a good electrical contact. But in VLSI circuits, the amount of doped silicon under the contact can be so small that almost all of it is taken up by the aluminum, thereby destroying the device. A method that has worked in LSI microcircuits is the use of alloys of silicon, aluminum, and other elements such as copper as contacting materials. Another way around the problem is the use of intermetallic compounds of silicon and metals such as platinum or palladium. The compounds, having fixed compositions, cannot dissolve additional silicon. But the applicability of either technique to the smaller dimensions of VLSI has yet to be demonstrated, and considerable basic research to study the metallurgy of these metal semiconductor systems is needed.

To the outsider, the prospect of a new generation of microfabrication tools that are not just incremental improvements on the existing technologies makes VLSI seem more challenging than just the expected next step in a continuous line of microcircuit developments. Interviews with several semiconductor industry executives, however, reveal the quite contrary feeling that, except for the high cost of the new equipment (*Science*, 2 May, p. 480), the microfabrication technologies required for VLSI circuits are neither exceptional nor a cause for great concern. This attitude on the part of the semiconductor industry may in part be attributable to the fact that most integrated circuit manufacturers have not been large vertically integrated companies, such as IBM and AT & T, and therefore do not have basic research laboratories of the type that would develop new microfabrication equipment. Moreover, they do not generally devise new processing equipment in their laboratories but rely on other firms that specialize in manufacturing the instruments to offer them commercially.

In any case, this relaxed attitude is not universal. Three and a half years ago, Ivan Sutherland and Carver Mead of the California Institute of Technology and Thomas Everhart of Cornell University, in a report to the Defense Department's Advanced Research Projects Agency, were already writing:‡ "In spite of the revolutionary nature of the changes in fabrication and design methods imposed by submicron geometries, U.S. industry appears to be treating these changes as further incremental progress. . . . Unless positive steps are taken, the existing U.S. investment in today's fabrication methods may be made obsolete by the new fabrication technologies, producing less vigorous competition domestically, and placing the United States in a disadvantageous position in defense and international trade."

The National Research Council report contained a similar conclusion. Summing up the situation on the threshold of the VLSI era, the report said: "Thus far, the semiconductor electronics industry has been based firmly in physics and chemistry. A reduction in scale of the characteristic dimensions of electronic devices in the micrometer and submicrometer range is imminent, and technical applications are outstripping their scientific base . . . a sustained, long-range program of research in microstructure science and engineering is necessary to provide an understanding of the base on which future technological developments must rest."

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†National Research Council, Solid State Sciences Committee, *Microstructure Science, Engineering and Technology* (National Academy of Sciences, Washington, D.C., 1979).

‡I. E. Sutherland, C. A. Mead, and T. E. Everhart, "Basic limitations in microcircuit fabrication technology" (report R-1956-ARPA, Rand Corporation, Santa Monica, California, November 1976).