Josephson Tunnel-Junction Electrode Materials

C. J. Kircher and M. Murakami

Summary. Josephson superconducting devices of the tunnel-junction type have exciting potential for use in building ultrahigh-speed computers. We consider the properties of superconducting metals that are needed for such devices that would be used in integrated computer circuits operated at a temperature near absolute zero. Recent advances in lead-alloy thin-film materials are described that have led to substantial improvements in lead-alloy Josephson device reliability. The properties of a $Pb_{0.84}In_{0.12}Au_{0.04}$ alloy, of Nb, and of Nb_3Sn are discussed as examples of three different groups of materials that are of interest. Investigations of lead-alloy and niobium devices have progressed to the point that it is evident that they have good potential for fabricating integrated circuits containing large numbers of devices.

Josephson superconducting devices have exciting potential for use in building ultrahigh-speed computers. These devices, based on the phenomena theoretically predicted by Brian Josephson in 1962, possess two key properties that are essential to building such computers: fast switching speeds and low power dissipation levels (*1*, *2*). The switching speeds of $\sim 10^{-11}$ second obtained for recent Josephson logic devices are faster than those of the most advanced semiconductor devices (*3*). In addition to having fast switching speeds, the devices must be small and closely packed, because the time required for electrical signals to propagate between devices can be the main factor limiting computer performance. (Electrical signals travel only ~ 1.5 millimeters in the device switching time of $\sim 10^{-11}$ second; thus to achieve the highest performance most of the many thousands of logic and fast memory devices in a high-speed computer should be located within a few centimeters of each other.) The low power dissipation of Josephson devices ($< 10^{-6}$ watt per device) should allow them to be packed densely without incurring heat removal problems (*1*, *4*). For very fast semiconductor logic circuitry, sufficiently dense packaging is already difficult to achieve because the power dissipation of the transistors (> 100 times higher than that of Josephson devices) exceeds the limits for which direct liquid cooling could be used to maintain safe operating temperatures. It is therefore necessary to use bulky heat sinks that result in lower packaging densities. For the potential of Josephson devices to be realized, novel materials and processes must be developed to enable them to be fabricated with the electrical characteristics desired for logic and memory devices and with the ability to withstand cooling to ~ 4 K above absolute zero (by immersion in liquid helium), the temperature region at which these devices operate.

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Josephson Devices

The type of Josephson device most suitable for high-speed computer applications is a SQUID (Superconducting QUantum Interference Device) composed of several superconducting tunneling junctions that share common electrodes (*2*). A schematic cross section through the center of such a device is shown in Fig. 1. The junction portions of the device consist of two electrodes separated by an ultrathin (5 nanometers) insulating layer. The electrodes are superconductors (metals that have an infinitely small electrical resistivity when cooled to below a characteristic temperature $T_c \approx 10$ K). The junction regions are defined by windows in a thicker insulating layer. The ultrathin insulating layer is typically an oxide grown on the base electrode. It is sufficiently thin that current flow can pass through it by electron tunneling; hence, it is referred to as a tunneling barrier. The current-voltage characteristic of such a junction has two branches, as shown in Fig. 2. A normal tunneling-current branch (b) for which a voltage occurs across the tunneling barrier, and a superconducting or Josephson tunneling-current branch (a) for which no voltage develops across the barrier. Because the Josephson current is very sensitive to magnetic fields, the junction can be switched from one branch to the other by passing a small current through a thin film wire (the control line in Fig. 1) located in close proximity to the junction. The remaining element of the device is a superconducting ground plane which is used to confine electrical signals to the close proximity of the device, thereby permitting close packing of devices without incurring cross-coupling between them. The control line and ground plane are separated from the junction electrodes by insulating layers not shown in Fig. 1. In addition, a thin-film layer of a nonsuperconducting metal is used to provide load and damping resistors. Integrated logic and memory circuits can be obtained by using the electrode and control-line layers for device interconnections. Such circuits (*5*) contain up to 14 thin-film layers that range in thickness from 0.02 to 2 micrometers, and are patterned in shapes with minimum dimensions of 2.5 μm by means of photolithography techniques similar to those developed for fabrication of semiconductor circuits. Most of the layers are prepared in vacuum by evaporating a source material and condensing the vapor on a silicon substrate containing any previously deposited patterned layers.

Electrode Materials

The properties desired for Josephson junction electrode materials can be divided into two categories: those which affect the junction characteristics needed for logic and memory device design and those needed to make possible the fabrication of thin-film, multilayer integrated circuits.

Properties desired for junctions. The superconducting property of the electrodes that is of most importance for junctions is the energy gap E_g. (When a

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metal is cooled below its superconducting transition temperature, T_c, its conduction electrons attain a lower energy state in which they are grouped into pairs. The energy gap can be thought of as the energy required to break up the pairs.) The size of the energy gap influences two features of the normal branch of the junction current-voltage characteristics (see Fig. 2, branch b): the energy gap voltage V_g at which the normal tunneling current rises steeply and the current level I_s below the energy gap. The value of E_g must be large compared to the thermal energy of the electrons in order for the value of I_s to be small compared to the maximum Josephson current I_m and in order for V_g to be well defined, as desired for logic and memory device design. To operate devices at 4.2 K, the boiling temperature of conveniently available liquid helium, a value of $E_g \gtrsim 2.5 \times 10^{-3}$ electron volts is needed. Such E_g values are obtained by using superconducting materials having a $T_c \gtrsim 7$ K. Of the elements, only lead and niobium have high enough T_c values. There are, however, a sizable number of alloys and intermetallic compounds that would also satisfy the E_g (T_c) requirement.

Electrode properties can also affect the tunneling barrier and hence the value of I_m, a junction characteristic that should be controlled to within ± 30 percent for proper circuit operation, as well as the value of the junction capacitance which affects the switching speed of a junction. The I_m value is exponentially dependent on the barrier thickness; as a consequence the barrier thickness typically needs to be controlled to within less than one atomic layer in average thickness. To achieve this degree of control, it is advantageous for several reasons to use an oxide grown on the lower junction electrode as the tunnel barrier. The growth rate of the oxides formed on many metals at low (ambient) temperatures decreases very strongly with increasing oxide thickness, leading to the growth of oxides having a very uniform thickness (*6*). Moreover, the growth rate becomes slow at oxide thicknesses similar to those desired for tunnel barriers (in part because electron tunneling from the metal to the surface of its oxide is an important factor governing the oxide growth), favoring good control of the oxide thickness. In addition, oxides are among the most chemically stable compounds of metals; thus use of an oxide tunnel barrier favors good stability of junction properties.

The tunnel barrier material will also affect the value of C_j, the junction capacitance per unit area. Since the switching and resetting times required for junctions are governed by the rate at which the capacitance can be charged and discharged (*7*), small C_j's are desired for devices. The C_j value is determined by the ratio of the dielectric constant of the tunnel barrier to its thickness. Thus, superconductors having metal oxides with small dielectric constants are favored for devices.

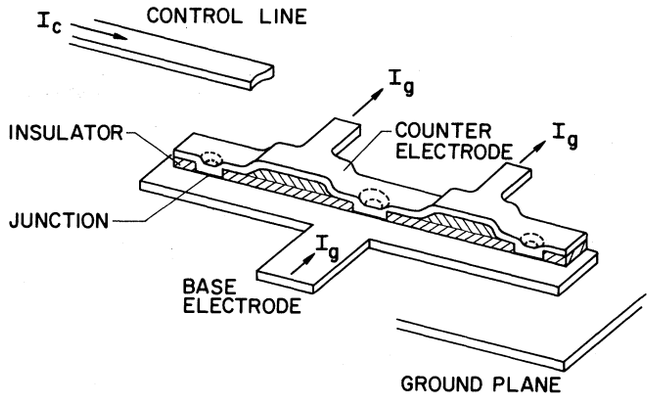

Fig. 1. Schematic cross section of a three-junction SQUID.

Unfortunately, efforts to use metal oxide tunnel barriers have not been successful for all superconductors of interest. This has led to the exploration of tunnel barriers that can be deposited, rather than grown, on the lower electrode (*8*). Such an approach has the advantages that the barrier material characteristics could be selected independently of those of the electrode—thereby avoiding the high dielectric constant oxides of some potential electrode materials, for example. In addition, the same barrier could be used with different electrodes. However, a problem with this approach is that deposited layers typically grow in a nonuniform manner on the thickness scale of interest for tunnel barriers. They initially form as nuclei at local sites (similar to the water droplets that form when steam condenses on a cool surface) and become a uniform, hole-free film only at larger thicknesses. The difficulty in obtaining pin-hole–free barriers with well-controlled I_m values is thus increased. It is not clear from the experiments that have been tried with this approach whether it could meet the requirements for integrated circuit applications.

Properties desired for integrated circuits. Integrated circuits involve the preparation on a substrate of many superimposed layers of different thin-film materials that are patterned into very small geometries. For Josephson circuits, most of the preparation is carried out at near-ambient temperatures, but the circuits are operated at 4 K. Thus, a large number of materials and processes must be compatible with each other to allow such circuits to be made successfully. Because of the great diversity of materials, fabrication techniques, and structures possible, as well as the trade-offs that can be made between them, the requirements for this compatibility can really only be considered with any degree of completeness for a rather specific set of the variables. However, a few general constraints that integrated circuit compatibility places on the choice of electrode materials are discernible from the experience we have gained to date.

The first concerns the magnitude of superconducting penetration depth, λ, an exponential decay length that describes the distance that magnetic fields penetrate into a superconductor before they become vanishingly small. For proper electrical operation of circuits the thickness of the superconductors must usually exceed $\sim 1.5 \times \lambda$ to avoid undesirable penetration of magnetic fields (*9*). However, for small geometries to be patterned on them, the film thicknesses must be small compared to their lateral dimensions. Because each successive layer in a multilayer structure is typically made with a greater thickness than that of those that precede it in order to ensure the coverage of underlying edges, it is important for the first patterned layers to be as thin as possible, for example, ~ 0.1 μm for Josephson devices. Thus, electrode materials with small λ values of ~ 0.1 μm are desirable for use in integrated circuits.

Another superconducting property that can be a constraint on the usefulness of a material for integrated circuits is the superconducting coherence length ξ, a measure of the distance over which a change in the structure or composition of a material will cause a change in its energy gap or transition temperature. In the course of preparing multilayer struc-

tures, materials are necessarily exposed to a variety of ambients, chemical solutions and cleaning processes that can alter the composition or structure of the surfaces of the materials to which they are exposed. For materials with values of ξ that correspond to thicknesses of few atom layers, for example, high-energy gap, high-transition temperature superconductors having the A-15 crystal structure such as Nb_3Sn and Nb_3Ge, these procedures may cause deterioration of the characteristics of junctions and interconnections between superconductors (*8*).

There are several other constraints that the multilayer nature of integrated circuits places on the materials and processes which can be used to prepare them. The stresses present in thin films that are prepared on substrates held at temperatures less than ~ 1/4 of their melting temperature, for example, niobium and other high melting temperature alloys, are typically very high and may exceed the values that underlying thin films or photoresist stencils can withstand. Also, the temperature at which some superconducting materials must be prepared to exhibit desirable superconducting properties, for example, above 500°C for the A-15 superconductors, is too high for many other useful thin-film materials to withstand.

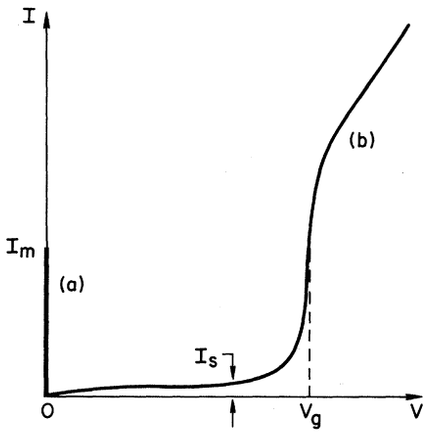

Fig. 2. Current-voltage characteristics of an interferometer similar to that shown in Fig. 1.

Finally, the thermal expansion coefficient of a material can be important. During cooling of devices from ambient to liquid helium temperatures the thin films are constrained to follow the dimensional changes of their relatively massive substrate. A difference in thermal expansion coefficients between film and substrate thus can cause large stresses to develop in the films. These stresses are a problem for superconductors with low melting temperatures, such as those containing lead, which typically have both high thermal expansion coefficients compared to those of useful substrate materials and a lesser ability to support stress without deforming.

Comparing materials. In comparing the properties discussed above with those of various superconducting materials that have been used or have potential for use as Josephson junction electrodes, we find that the materials can be classified into three groups. The properties of a representative material from each group that has been used to prepare successful junctions have been summarized in Table 1. The first group is that of the superconductors with low melting temperatures, exemplified by the $Pb_{0.84}In_{0.12}Au_{0.04}$ alloy and including, for example, lead, tin, indium, and gallium and their various alloys. This group is distinguished from the others primarily by the mechanical properties of its members. They have low values of intrinsic stress σ_i, but larger values of thermal stress σ_T and a greater susceptibility to stress relaxation.

The second group is exemplified by niobium and includes, for example, tantalum and vanadium. The third is exemplified by Nb_3Sn and includes, for example, Nb_3Si, V_3Si, Nb_3Al, and other alloys of niobium, vanadium, or molybdenum with aluminum or silicon. Films of members from both of these groups are typified by their superior mechanical strength and by the large stresses they contain at ambient temperature. The members of the third group are distinguished from those of the second primarily by their much smaller coherence length (ξ) values, by the high substrate temperatures T_s typically required to prepare them, and by the potential they offer for obtaining junctions with reduced capacitance compared to those of the second group because of the elements they contain that form lower dielectric constant oxides.

The present status of efforts to prepare junctions or integrated circuits, or both, from these materials varies. Substantial experience has been gained in the use of lead-alloy Josephson junctions. A process has been developed and successfully used to fabricate experimental integrated circuits containing ~ 100 SQUID devices (*5*). The materials used and the functions they serve are listed in Table 2. The substrates are oxidized silicon wafers, chosen principally for their

Table 1. The properties of several superconducting materials that have been used as electrodes in Josephson junctions. Each is representative of one of the three groups discussed in the text.

Properties (units)	Pb-In-Au	Nb	Nb_3Sn
Superconducting			
T_c (K)	7	9.2	17
λ (nm)	150	85	170
ξ (nm)	~ 30	~ 30	~ 3
Tunnel barrier			
I_m Control	Good	Good	Unknown
$C_j(\mu F/cm^2)$	4.3	~ 15	≥ 2
Mechanical stress			
σ_i	Low	High	High
σ_T	High	Low	Low
Preparation conditions			
T_s (°C)	≤ Ambient	~ Ambient	≥ 500

Table 2. Thin film layers used in lead-alloy logic circuits.

Layer	Material	Thickness (nm)	Function
1	Nb	300	Ground plane
2	Nb_2O_5	25 to 35	Ground plane insulation
3	SiO	145 to 275	Ground plane insulation
4	$AuIn_2$	30 to 43	Terminating, loading, and damping resistors
5	SiO	200	Logic interferometer isolation and resistor insulation
6	$Pb_{0.84}In_{0.12}Au_{0.04}$	300	Ground plane contacts and logic interferometer inductance
7	$Pb_{0.84}In_{0.12}Au_{0.04}$	200	Base electrodes, interconnections, and resistor contacts
8	SiO	275	Junction definition and insulation
9	PbO/In_2O_3	6.5	Tunneling barriers
10	$Pb_{0.71}Bi_{0.29}$	400	Counterelectrodes
11	SiO	100	Counterelectrode protection layer
12	SiO	500	Control line and interconnection insulation
13	$Pb_{0.84}In_{0.12}Au_{0.04}$	800	Control lines and interconnections
14	SiO	2000	Protective layer

high thermal conductivity and their suitability for use as the structural members in packaging large numbers of integrated circuits. Most of the superconducting layers are lead alloys which allow low-capacitance junctions to be formed. The alloy additions were selected to obtain films with improved chemical, mechanical, and superconducting properties compared to those of pure lead. The insulation layers are primarily SiO, selected because it can be prepared at the low substrate temperature and low stress levels desired for use with lead-alloy films. The tunnel barrier is an oxide grown on the Pb-In-Au base electrode alloy.

A scanning electron micrograph of a logic SQUID prepared by this process is shown in Fig. 3. The two ~ 2.5-μm-wide control line loops (Fig. 3A) pass over the top of the device. The four junctions (Fig. 3B) of the same size are faintly visible beneath the inner control line. The counterelectrode (Fig. 3C) occupies the center region of the device, with the base electrode (Fig. 3D) extending beneath most of the region under the control lines. Logic devices of this type have been operated with an average logic delay of 1.3×10^{-11} second (*10*). Memory cells suitable for use in a memory with a 1×10^{-9} second access time have been fabricated using similar techniques and operated with a stored energy of only $\sim 6 \times 10^{-20}$ joules (watt-second) (*11*).

The experience gained to date indicates that with further development this process has good potential for meeting the yield, tolerance, and reliability levels that will be required to make computers with large numbers of Josephson integrated circuits. The principal materials-related concern is the stability of the devices during thermal cycling between 300 K and 4.2 K. Devices similar to that shown in Fig. 3 will withstand ~ 100 cycles before the first failures are observed in a population of 100 devices (*12*). Computers made with Josephson devices would probably not be subjected to very large numbers of thermal cycles (several hundred are estimated), but they would contain a very large number of devices. Thus, it is clear that further improvement in the thermal cycling stability of lead-alloy devices is needed. Investigation of the strain behavior of lead and lead-alloy thin films has recently resulted in the development of lead-alloy junctions with significantly improved thermal cycling stability, as discussed below.

For the case of niobium electrode materials, SQUID devices have been made with niobium base electrodes, niobium-oxide tunnel barriers, and counterelectrodes of either niobium (*13*) or lead alloys (*14*). At present, only those with lead-alloy counterelectrodes have been made with current-voltage characteristics with the low I_s values desired for integrated circuit applications. Much less experience has been gained with these devices than for the all lead-alloy devices. However, arrays containing substantial numbers of individual devices have been made successfully. They exhibit excellent thermal cycling stability and the desired values of the Josephson current can be obtained with reasonable reproducibility and uniformity. These devices offer good potential for integrated circuit fabrication. Much of the experience gained during the development of circuits with lead-alloy junctions could be applied to the development of circuits using niobium electrodes. The principal concern with them is the ~ 3.5 times higher values of their junction capacitance which would reduce computer performance by approximately a factor of 2 (*15*), according to estimates based on present circuit design concepts. It is not yet clear whether the effect of this capacitance can be reduced or circumvented.

For Nb_3Sn and other materials in the third group, small numbers of large area junctions have been made, usually with lead counterelectrodes. Some junctions with current-voltage characteristics of good quality have been obtained. The capacitance of Nb_3Sn:Pb junctions was found to be promisingly low (*16*), although this result may have been due to the presence of excess tin on the surface of the Nb_3Sn (*17*). However, too little experience has been gained to date to allow a realistic assessment of the potential of such junctions for integrated circuit applications. For example, the effect on the

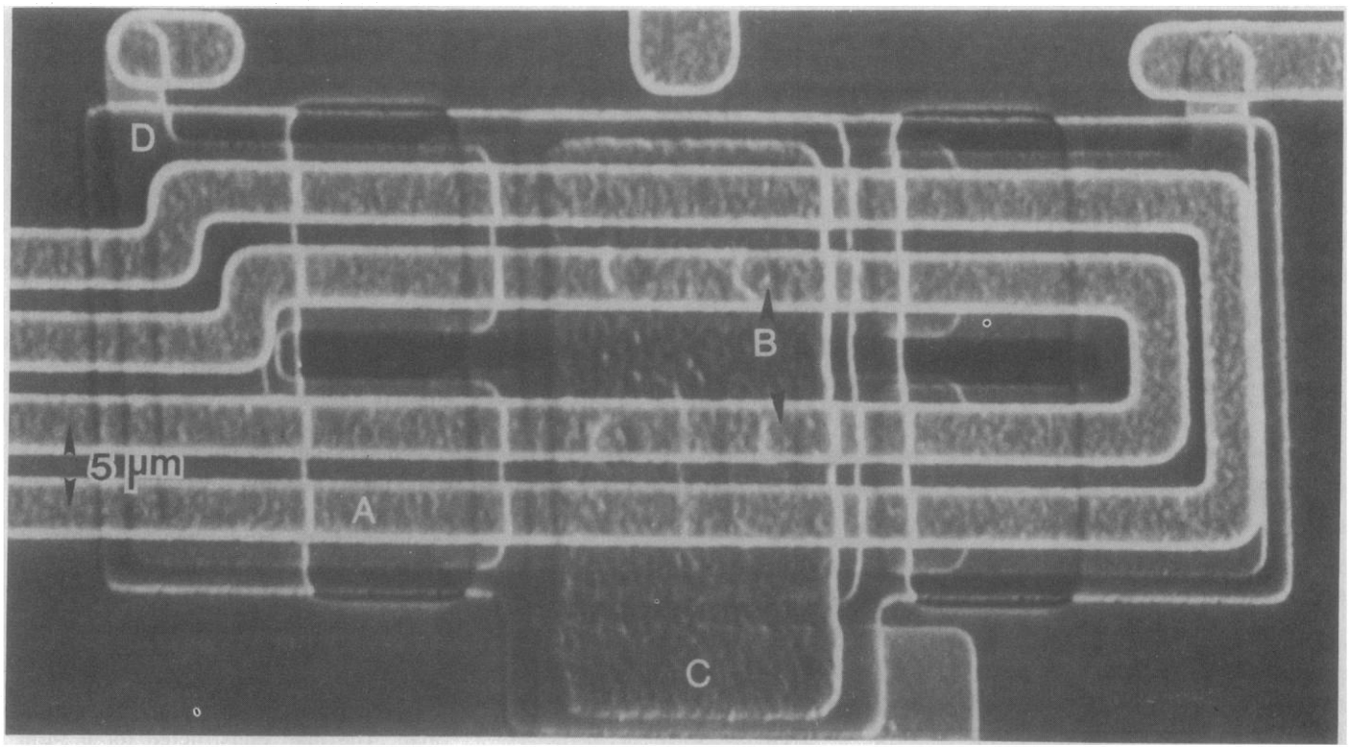

Fig. 3. Scanning electron micrograph of a Josephson logic interferometer containing 2.5-μm-diameter junctions.

junction properties of preparing the junctions by methods compatible with integrated circuit fabrication are not yet known. The development of a barrier formation process that would provide reproducible Josephson currents in the range needed for integrated circuits has not yet been attempted. A consistent set of materials and processes compatible with the ~ 700°C substrate temperatures needed for preparation of these materials has not yet been devised.

Lead-Alloy Junctions with Improved Thermal Cycling Stability

The nature of the cycling problem. The failure of lead-alloy junctions occurs as a short circuit that develops during thermal cycling because of the rupture of the tunnel barrier oxide. The rupture occurs abruptly after some number of cycles, giving rise to an additional nontunneling current in the current-voltage characteristic that grows with additional cycling until it becomes dominant. This additional current has the properties of a superconducting microbridge of ~ 0.1-μm size shunting the tunnel barrier (*18*). The microbridge is believed to form because of stress relaxation in the junction electrodes during cycling.

Hillocks, micrometer-size protrusions that grow up from the film surface when a lead-alloy film on a substrate is repeatedly cycled to 4.2 K (*19*), are macroscopic evidence that stress relaxation is occurring. Such hillocks are suppressed when lead-alloy films are covered by additional layers, thus they are not observed in failed devices. Nevertheless it seems likely that device failures are due to the formation of "incipient" hillocks.

Hillocks can occur in a thin film when it is subjected to a compressive stress in the plane of the film. Such a compressive stress can develop in (initially stress-free) lead-alloy films during thermal cycling: the difference in thermal expansion coefficients of lead and the underlying silicon substrate are such that a lead-alloy film would be under tensile strain (elongation) during the cooling. If some relaxation of this strain occurs, the film would be compressively stressed upon rewarming to ambient temperature. According to this picture, hillock formation should be reduced if strain relaxation in the lead-alloy films could be reduced during cooling so that the films would return to ambient temperature in their original near-zero stress condition. We would thus like to determine the mechanisms by which strain relaxation can occur in lead-alloy films and to determine the amount of strain that such films will support elastically at 4.2 K, that is, without strain relaxation.

Strain relaxation. The amount of strain that a film actually supports elastically at 4.2 K, ε'_{33}, can be determined by using an x-ray diffraction technique to measure the spacing between atom planes in the film material after it has been cooled to 4.2 K (*20*). The total amount by which the film is strained during cooling, ε_{max}, can be calculated for lead by using known thermal expansion coefficient data for lead and silicon. The amount of strain relaxation is then $\Delta\varepsilon = \varepsilon_{max} - \varepsilon'_{33}$. The stresses corresponding to the strains can be calculated from the known elastic constants of lead.

The dominant strain relaxation mechanism in a material in a given region of stress and temperature can be identified by preparing a deformation mechanism map. The map constructed for 0.2-μm thick Pb-In-Au films (*21*) is shown in Fig.

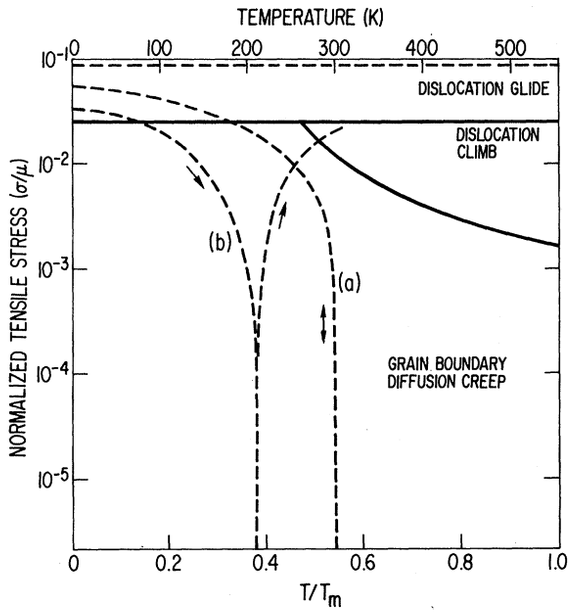

Fig. 4. Deformation mechanism map for Pb-In-Au thin films.

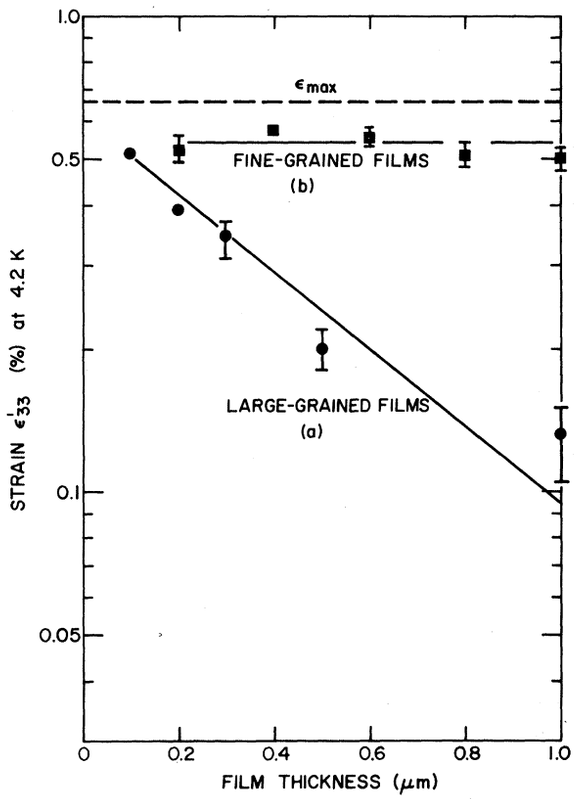

Fig. 5. Strain at 4.2 K for Pb-In-Au films with (a) large-grain and (b) small-grain sizes.

4. It was prepared by calculating for each stress σ (normalized by its shear modulus μ) and temperature, the strain relaxation rate for all relevant mechanisms to identify the dominant (fastest) mechanism. The σ-T map can then be divided into regions labeled by the dominant mechanism. The boundary between two regions is located at the set of (σ, T) values where the strain relaxation rates of the two corresponding mechanisms are equal. Three regions (mechanisms) are evident in Fig. 4. Also shown in Fig. 4, curve a, is the calculated (σ, T) trace that would be followed by a lead film (initial $\sigma = 0$) on a silicon substrate when cooled to 4.2 K, assuming no strain relaxation occurs. It is seen that the fields of two deformation mechanisms are traversed during cooling, that is, grain boundary diffusion creep at $T \geq 200$ K and dislocation glide at $\sigma/\mu > 2 \times 10^{-2}$. Because the cooling rates are very rapid near 300 K, the amount of strain relaxation by diffusion creep (strain relaxation by transport of atoms along the film grain boundaries) should be small. Thus, dislocation glide (strain relaxation inside grains of a film by shearing between planes of atoms) is expected to be the dominant deformation mechanism during cooling. If no strain relaxation occurs during cooling, the (σ, T) path during rewarming would reversibly follow the cooling curve, provided that the heating rate is sufficiently high (near 300 K) that diffusion creep is again negligible. If, however, dislocation glide does occur during cooling, then the path followed during rewarming would be along a curve such as curve b in Fig. 4: the tensile stress would reach 0 near 200 K, becoming compressive between 200 and 300 K and lying within the diffusion creep field, producing a driving force for hillock formation.

We would thus like to prevent dislocation movement in the electrode materials to improve the thermal cycling stability of lead-alloy devices. For bulk materials this is accomplished primarily by alloying or adding impurities to interrupt the almost perfect periodicity of the crystal structure within the grains of the material, thereby creating obstacles which inhibit or prevent dislocation motion. The stress that a material will support is $\sigma_c \propto l^{-1}$, where l is the spacing between the obstacles. Lahiri (*19*) added gold or indium or both to lead (to retard grain boundary movement), and this resulted in the formation of small intermetallic compound particles in the films. Both a lower incidence of hillock formation and an improvement in thermal cycling stability were obtained (*22*). The elastic strains supported by these alloys as well as by pure lead are very similar and are below ε_{max}. Thus, the primary effect of such additions was to improve the uniformity of the strain relaxation, rather than to reduce its average value.

For thin films, additional obstacles to dislocation movement are present, for example, the native oxide on the film surface, the substrate, and grain boundaries. Thus, the film thickness, h, and grain size, g, may be thought of as obstacle spacings where $l \simeq h$ or g.

The level of elastic strain ε'_{33} supported by $Pb_{0.84}In_{0.12}Au_{0.04}$ films of various thicknesses and grain sizes that were deposited on silicon substrates and cooled to 4.2 K is shown in Fig. 5. The dependence of ε'_{33} on film thickness for large-grained films (prepared by deposition on substrates held at 24°C) is given in curve a (*18*). For this case the film thickness controls the level of strain relaxation $\Delta\varepsilon = \varepsilon_{max} - \varepsilon'_{33}$. It is seen that ε'_{33} is less than ε_{max} and decreases with film thickness, that is, strain relaxation occurred during cooling at a level that decreased with decreasing film thickness. Decreasing the film thickness from ~ 0.45 μm to ~ 0.23 μm, which resulted in a decrease in $\Delta\varepsilon$ of ~ 30 percent, also resulted in a decrease in the level of hillock formation and a tenfold improvement in thermal cycling stability (*23*).

The effect of reducing grain size of $Pb_{0.84}In_{0.12}Au_{0.04}$ films is shown in Fig. 5, curve b (*24*), which gives the strain level supported by fine-grained films prepared at 77 K according to a process developed by Huang *et al.* (*14*) in order to obtain $g < h$. In this case the grain size controls the strain behavior: ε'_{33} is thickness-independent and nearly equal to ε_{max}, similar to the results previously obtained for pure lead films (*25*). At $h = 0.2$ μm (the minimum thickness currently used for lead alloy Josephson junction base elec-

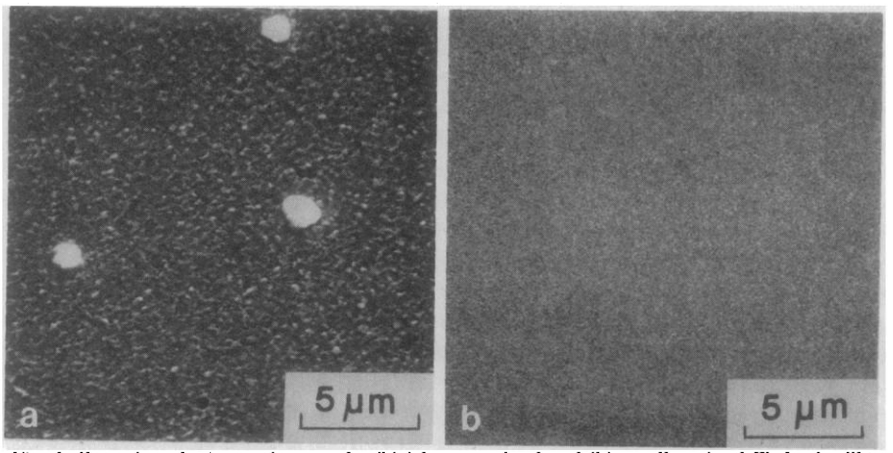

Fig. 6. Scanning electron micrograph of (a) large-grained and (b) small-grained Pb-In-Au films after repeated thermal cycling.

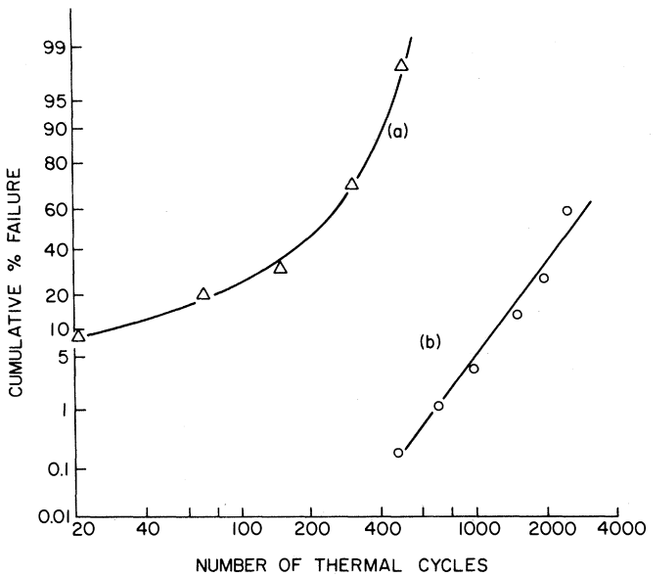

Fig. 7. Cumulative percentage failures for Josephson junctions made with (a) large-grained and (b) fine-grained base electrodes.

trodes, chosen to maintain $h > \lambda$), the strain relaxation upon cooling from 300 K to 4.2 K is much smaller in a fine-grained film than in the large-grained film. Thus, upon rewarming to room temperature, a compressive stress that can cause hillock formation is expected for the large-grained films, but not for the fine-grained films.

In Fig. 6, scanning electron micrographs are shown for two such 0.2-μm-thick films that have been cycled repeatedly to 4.2 K. In Fig. 6a a large-grained Pb-In-Au film (of the type used to prepare the device of Fig. 3) that was cycled 100 times can be seen to have several hillocks that developed during cycling. In Fig. 6b, a fine-grained film is shown that was cycled 725 times. No changes were visible. Nor were any cycling-induced changes evident in either the more sensitive x-ray analyses carried out on such films (*24*) or the more stringent tests to promote hillock formation (*12*). Thus, the fine-grained films exhibit significantly improved strain behavior.

Devices with improved thermal cycling stability. The stability during thermal cycling of devices fabricated with 0.2-μm-thick, fine-grained Pb-In-Au alloy base electrodes is substantially better than that of otherwise similar devices prepared with large-grained base electrode films (*12*). Figure 7 shows the best results obtained for each case from several controlled experiments in which ~ 1300 large area junctions were used. (The large junctions, chosen to enhance the probability of failure, were equivalent in area to ~ 375 devices of the type shown in Fig. 3.) The junctions with the fine-grained base electrodes appear to follow a log-normal statistical distribution with the first failures occurring only after 400 cycles between 300 K and 4.2 K. The companion junctions with large-grained base electrodes showed ~ 100 percent failure at this point. The use of fine-grained base electrodes has thus improved the junction cycling stability by more than a factor of 100. Further significant improvements in the thermal cycling stability in lead-alloy junctions may be obtainable by using fine-grained films for the junction counterelectrodes. The potential for meeting the device stability levels required for computer applications by using such fine-grained lead-alloy film electrode materials appears to be very good.

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