New Methods of Processing Silicon Slices

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Summary. Through the use of room-temperature, radio-frequency plasma ionization of gases, the insulating, conducting, and semiconducting materials associated with the fabrication of silicon integrated circuits can be patterned to submicrometer dimensions. A tutorial description is presented of the fabrication techniques used in the past with an overview of where plasma processing has made noteworthy improvements in the lithography of materials.

Within the semiconductor component factories for the last decade there has been a proliferation of fabrication methods generally classed as dry processing. To appreciate the advantages and limitations of such processes requires some basic knowledge of the classical fabrication of silicon integrated circuits (IC's). This knowledge will also be applicable to some of the other articles in this issue dealing with the fabrication of microscopic geometries.

A silicon IC typically starts with a slice of single-crystalline material about 0.5 millimeter thick and 100 millimeters in diameter whose mechanical and electrical characteristics are held to critical specifications. Many IC's are fabricated on this slice simultaneously by (i) growing or depositing specific layers of materials, (ii) partially removing these materials to define microscopic geometries, and (iii) altering the electrical properties of these materials. In this way a three-dimensional structure can be constructed by varying the geometries in two dimensions while the thickness is essentially constant throughout a particular material layer. The first layer on the slice is usually epitaxially grown single-crystal silicon or oxidized silicon.

Thousands of metal-oxide-semiconductor (MOS) transistors are used in a single pocket calculator, so I will choose this device as a typical semiconductor part. The completed structure of such a device is sketched in Fig. 1. Table 1 shows the materials and typical dimensions of such a structure. In other semiconductor products such as linear circuits, bipolar logic, Schottky and so on, different materials and processes are used, but the techniques are similar enough for descriptive purposes. In this case we start with an initial oxidation of the slice of the order of 1000 angstroms and deposit silicon nitride of the order of 1000 angstroms. (Note that neither of these layers is evident in the finished product.) Throughout the fabrication process the manipulation of layer dimensions and properties is effected by the use of secondary materials that protect or "resist" the etching, oxidation, deposition, or ion implantation to which other parts of the slice are exposed. In this case the nitride layer protects the area the transistor will later occupy from thick oxidation, as in the LOCOS (local oxidation of silicon) process (*1*).

To pattern this material we make use of another secondary material—photoresist. The photoresist pattern is determined by yet another secondary material, chrome, with a photomask pattern which itself was patterned with photoresist. A master mask was used to expose this "working plate" photomask. The master mask itself was made by photoreduction of a "reticle," which replicates what we wish chip geometries to be. This is a rather tortuous path for such a simple result, and I have made the explanation complete to show how important the proper execution of material lithography is to the manufacturing process. One blemish in the pattern of the reticle for just one material layer can destroy every chip on every slice in the manufacturing line. Because of its great importance, lithography has been studied with intensity, and this has led to several advanced techniques that are discussed later in this article.

Continuing with the description of the MOS fabrication process, Fig. 2 shows the stages of producing the "moat" area in which the MOS transistor will reside. The nitride surface is coated with a polymeric material that is photosensitive to ultraviolet light. In this case the photoresist is assumed to be negative, which means that it will be polymerized where the ultraviolet light strikes it. Thus the mask that produces this pattern is clear where the pattern will become opaque in the resist. Now the photoresist layer is "developed" in a solvent solution, which washes away all the unpolymerized resist and leaves the resist that was exposed to ultraviolet, as shown in Fig. 2b. A batch of several resist-patterned slices can now be etched simultaneously by placing them in a hot phosphoric acid retort. The edges of the resist may tend to lift during this operation and degrade the geometric definition, as in most wet etching processes. Plasma (dry) etching is now fairly common at this process step and avoids the photoresist lifting problem. The resulting slice pattern is shown in Fig. 2c. Many of these patterned slices are now placed in a furnace tube and subjected to a hot oxidizing environment for several hours. The nitride layer oxidizes very little, while the surrounding silicon is oxidized to a thickness of about 10,000 Å. This thick "field" oxide is used to space the MOS conductors away from the silicon substrate so that parasitic MOS transistors will not be created. The finished oxidation pattern is shown in Fig. 2d.

It is not my purpose here to require the reader to become a process expert, and I have omitted many steps (such as channel stops and cleaning steps) while trying to retain enough detail to highlight areas where dry processing can be used to advantage. To continue with the fabrication process, the moat area is stripped to the bare silicon. A very clean gate oxide is now grown to a thickness of nearly 1000 Å. Polysilicon is deposited and patterned in a lithographic manner similar to that described above. The wet etching of polysilicon MOS gate electrodes has traditionally been more art than science. Dry etching allows so much improvement that narrower gate dimensions have been readily achieved. This is very desirable for very large scale integrated circuits (VLSI). The previous moat patterning step did not require any alignment with an underlying pattern. The

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Table 1. Semiconductor materials and common dimensions for the MOS transistor shown in Fig. 1.

Material	Thickness (Å)	Minimum dimension (μm)
Primary		
Silicon oxide (gate)	1,000	
Polysilicon (gate)	5,000	5
Doped silicon (source, drain)	7,000	5
Silicon oxide (field)	10,000	5
Aluminum	10,000	7
Secondary		
Photoresist	5,000	5
Silicon oxide (initial)	1,000	10
Silicon nitride (moat)	1,000	10
Chrome	1,000	5

silicon gate pattern must, however, be placed within the moat area. After several steps we now have the cross section shown in Fig. 3a. The source and drain areas may now be created in the silicon substrate without additional lithographic techniques by using the thick field oxidation and the silicon gate electrode to protect the material they cover. Either furnace tube diffusion of dopant materials (such as phosphorus or boron) or ion implantation may be used to create the source and drain areas. In the more modern ion implantation method, ions of the dopant are accelerated in an ion gun structure and a beam of these ions is focused and scanned across the slice surface in a uniform, controlled-dosage manner. Subsequent furnace tube processes drive these ions to the proper crystallographic locations to create an active transistor, as shown in Fig 3b.

This should be enough exposure to the basic problems of semiconductor fabrication. High-quality, low defect density material lithography must be accomplished. To do this, resist patterning and alignment to previous patterns must be precise to less than 1 micrometer over a linear dimension of 100 mm. While one layer of material is being modified, the layers of material exposed beside it and underlying it must not be harmed. For example, when the polysilicon gate was formed above, polysilicon was removed over oxide. The etchant for this silicon must not attack the oxide at a high removal rate. The advantage of dry processing is its ability to define very small (< 1 μm) widths. Removal of a specific material without affecting others is more difficult.

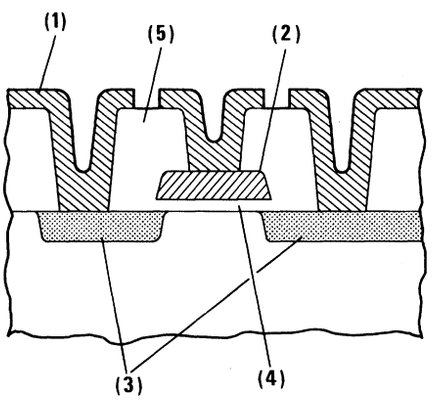

Fig. 1. A metal-oxide-semiconductor transistor structure with material and dimensions outlined in Table 1. Shown are (1) aluminum leads, (2) silicon gate, (3) source and drain, (4) gate oxide, and (5) field oxide.

Masks and Pattern Generation

The patterning sequence outlined in Table 2 will be used to trace how the ideas of the circuit designer are reduced to the material patterns desired. Through computer simulation and modeling techniques, the designer defines the pattern requirements for every layer of the desired device. A pattern generation program is written and stored on a medium such as computer magnetic tape. This tape is used to manipulate an x, y stage, which holds a plate coated with photographic emulsion beneath a tiny spot of light; the exposure can run to hours. The photosensitive plate is developed by traditional photographic methods. This makes an oversized image (ten times the typical size) of one layer of one chip. The oversizing makes the effect of dirt and emulsion defects less important.

The reticle is mounted on a repeating printer and reduced with lenses to the desired image. One exposure is made of one chip, then the resist-covered chrome master is very accurately stepped to an adjacent location and again exposed. All levels must register from top to bottom at every x, y location. This mask level is developed with solvent and etched to describe the geometry accurately. To preserve these master masks, a set of several submasters may be contact-printed and used to produce working plates.

Although each step can be performed at a relatively low defect level, there are about 100 material levels in a simple device where something can go wrong. If the level integrity is as good as 0.995, one still loses 40 percent of the devices; if it is as poor as 0.98, one loses 97 percent.

One of the first uses of electron beam exposure machines has been in making photomasks. The patterning can be used to make masters or working plates, depending on the cost and complexity of the final product. Unfortunately, many electron-sensitive materials tend to have adhesion problems when wet-etched. Once again, dry processing can be used advantageously.

Table 2. Traditional photomask fabrication.

Operation	Materials affected
1. Reticle pattern generation	Emulsion
2. Master photomask	Resist, chrome
3. Submaster photomasks	Resist, chrome
4. Working photomasks	Resist, chrome
5. Semiconductor fabrication	See Table 1

Although the mask system discussed above virtually eliminates mask-associated defects, the slow throughput makes

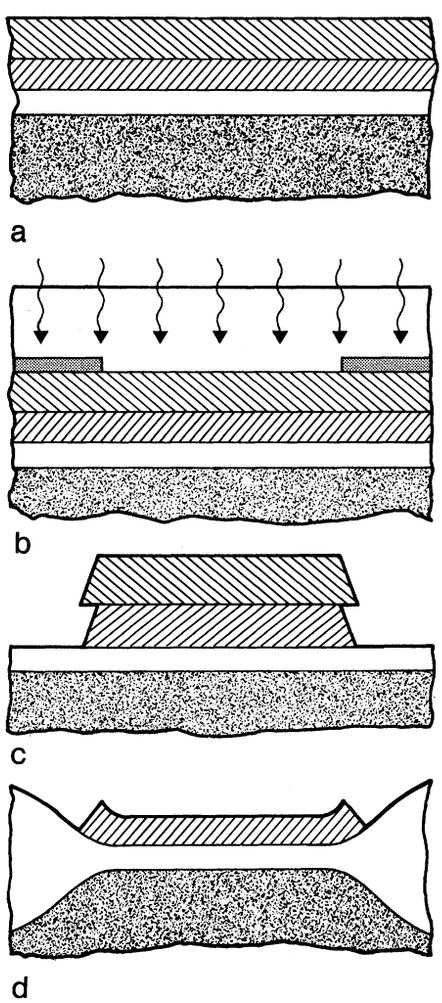

Fig. 2. How material layers are manipulated by overlaying other materials for protection: (a) unpatterned sandwich of silicon, oxide, nitride, and photoresist; (b) exposing the resist pattern to ultraviolet light; (c) after etching nitride; and (d) after furnace tube oxidation.

the process expensive. Another modern approach uses electron beam techniques to define a chrome oversize reticle. Now, instead of stepping a reduced image on a mask, one directly steps this reduced image onto the resist-coated silicon slice. Geometries as small as 1 to 2 μm can be defined in this manner on resist, and with dry processing the resist survives the subsequent patterning operation.

What might be considered the ultimate short circuit of the mask process is the approach of "writing" on the material desired. Although there is activity in this area, maturity is several years away. In the meantime we can come close to this approach by coating the slice itself with electron beam-sensitive resist and generating patterns by computer software directly on the slice itself. This has the great advantage of chip-by-chip alignment and extremely fine geometry generation. The disadvantage is increased pattern generation time.

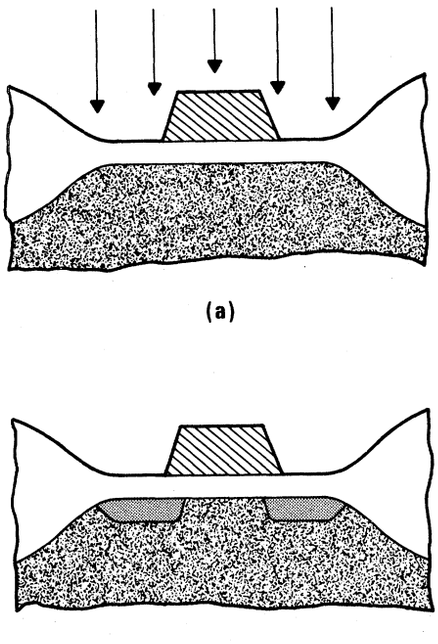

Fig. 3. Placing the source and drain automatically by aligning the gate within the moat area: (a) as patterned and (b) after ion implantation and furnace drive.

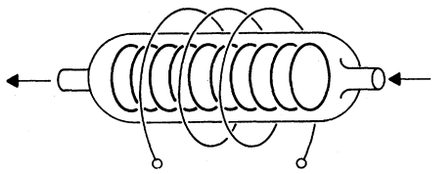

Fig. 4. Older tubular plasma reactor that holds slices upright.

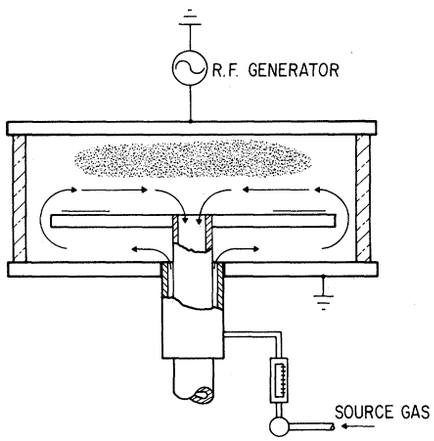

Fig. 5. Radial flow reactor with slices flat on lower surface.

Plasma Machine Evolution

The use of cold discharge tube reactions in the semiconductor industry is by no means new. The first major use of plasma processing was in removing common organic photoresists (*2*). A schematic representation of a typical apparatus in shown in Fig. 4. In this apparatus the slices are held upright in a carrier, much as in a furnace tube. The chamber is evacuated to a pressure of a few torrs and a radio-frequency generator is connected to the terminals shown. A mixture of argon and oxygen is introduced into the chamber and generates a glow discharge of relatively low magnitude in the classical plasma discharge sense. This creates an oxidizing environment, which rapidly converts the organic photoresist to the volatile products carbon dioxide and water vapor. Here we have the underlying principle of all semiconductor dry etching processes. A solid material is converted to gaseous byproducts, which are removed by the vacuum pumping system.

The active species generated in a tube reactor must have a sufficient lifetime to reach the surfaces of interest. Some etches and depositions can be made only by generating the active species near the surface of the slice. Sterling and Swann (*3*) showed how chemical vapor deposition could be promoted between two capacitor plates. The extension of this idea to a plasma reactor of the radial flow type was demonstrated by Reinberg (*4*),

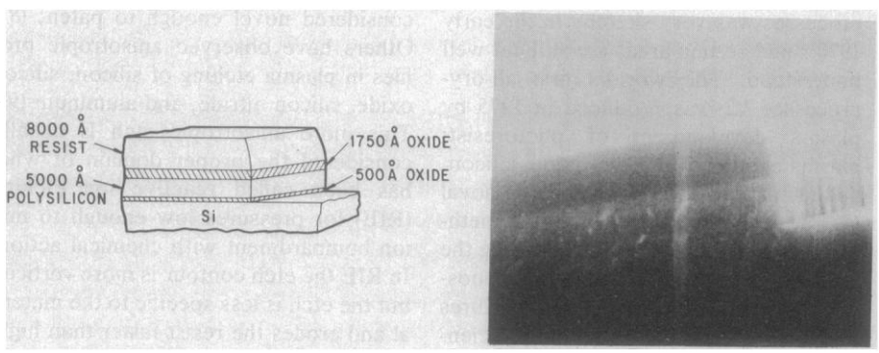

Fig. 6. Plasma etching of multiple layers.

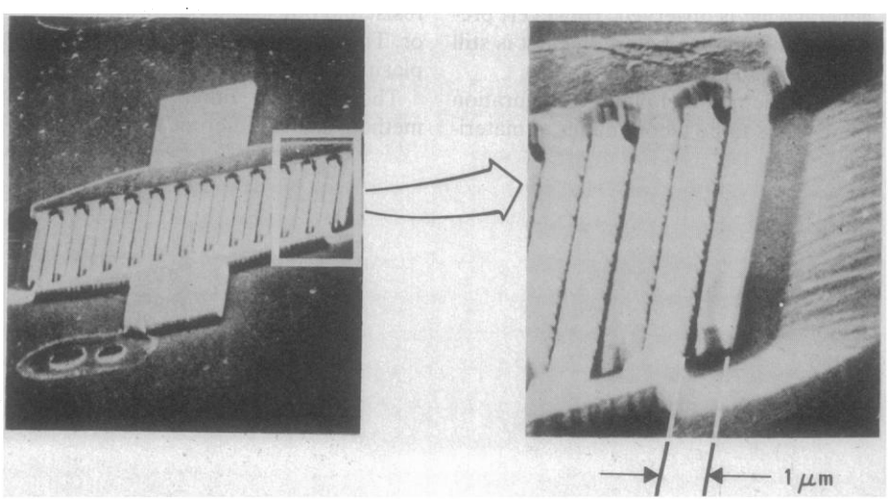

Fig. 7. Reactive ion-milled microwave bipolar transistor.

Table 3. Solid materials deposited and removed with gases used for the plasma process.

Solid	Gases
Depositions	
Silicon nitride ($Si_xN_yH_z$)	Silane (SiH_4) and ammonia (NH_3)
Silicon oxide ($Si_xO_yH_z$)	Nitrous oxide (N_2O) and SiH_4
Amorphous silicon	SiH_4 and argon
Material removal	
Silicon oxide (SiO_2)	Silicon tetrafluoride (SiF_4) Carbon tetrafluoride (CF_4) C_3F_8, C_2F_6, C_5F_{12}, CHF_3
Silicon	CF_4 and O_2 Carbon tetrachloride (CCl_4) and hydrogen chloride (HCl)
Silicon nitride (Si_3N_4)	CF_4
Vanadium, titanium, tantalum, molybdenum, tungsten	CF_4
Chrome and chrome oxide	CCl_4
Aluminum	CCl_4, boron trichloride (BCl_3)
Photoresist	Argon and O_2

and a sketch of such a reactor is shown in Fig. 5. Such reactors have been in extensive production use at Texas Instruments since 1972, and there are now several manufacturers of similar equipment.

Development of Dry Processing

The scientific understanding of plasma processes was very sketchy in the early 1970's and certain areas are still not well understood. The world's first all-dry-processed IC was produced in 1975 by plasma development of photoresist; plasma etching of nitride, oxide, silicon, and aluminum; and ozone resist removal (*5*). Nevertheless, virtually all the methods were worked out by determining the volatile products of the solids and choosing likely combinations of gas mixtures to produce them. More recently, scientists at IBM (*6*) and Bell Laboratories (*7*) have studied the action of a common fluorocarbon etchant, CF_4, in the etching of silicon in enough detail to explain in general what is observed. However, predicting an outcome before the fact is still a low-probability exercise.

With the parallel-plate configuration there tends to be a continuum of material removal processes as pressure is changed. At pressures of 0.1 to 10 torrs the plasma etching performed is sometimes referred to as chemical plasma etching. In this region one can obtain fairly high specific etch ratios of silicon to oxide by using a fluorinated gas. The etch characteristics tend to be isotropic, although when silicon is etched with a chlorinated species the profiles obtained are quite vertical, and this process was considered novel enough to patent (*8*). Others have observed anisotropic profiles in plasma etching of silicon, silicon oxide, silicon nitride, and aluminum (*9*). This more anisotropic etch is usually considered the proper domain of what has been called reactive ion etching (RIE) for pressures low enough to mix ion bombardment with chemical action. In RIE the etch contour is more vertical, but the etch is less specific to the material and erodes the resist faster than higher pressure etches do. As the pressure is lowered still further we enter the sputter etching or ion milling regime, where energetic ions of argon "sandblast" away resist and other materials with equal vigor. The removal rate is lower than that in plasma etching.

There is one other plasma etching method that is different from those discussed above. A high-power-density microwave discharge can produce metastable atoms with long lifetimes which etch material almost as if it were immersed in acid—that is, isotropically. There is some evidence that the etching species produced in this reaction is not the same as the species in the reactions described above.

Applications of Dry Processing

A plethora of plasma etch gases and combinations can now be used to remove almost any material employed in the fabrication of silicon IC's, photomasks, and magnetic bubble structures. The emphasis has been on the small dimensions obtainable at low defect densities. Shown in Table 3 is a list of materials and the etch gases used for their removal. The list is by no means complete, as many manufacturers consider their gas recipes trade secrets. The vertical section in Fig. 6 illustrates some of the exciting possibilities for structures that can be realized by plasma etching with nearly zero undercut. In Fig. 7 the close spacing and narrow geometries of a microwave transistor structure show what can be achieved by direct writing with an electron beam on the resist over the material to be patterned. These are but a few of the many advances that can be expected in material lithography when plasma etching is combined with modern resist techniques.

References

1. J. A. Appels, K. Kooi, M. M. Paffen, J. J. H. Schatorje, W. H. C. G. Verkuylen, *Philips Res. Rep.* **25**, 118 (1970).
2. C. E. Gleit and W. D. Holland, *Anal. Chem.* **34**, 1454 (1962).
3. H. F. Sterling and R. C. G. Swann, *Solid-State Electron.* **8**, 653 (1965).
4. A. R. Reinberg, U.S. Patent 3,757,733 (1973).
5. T. C. Penn, *IEEE Trans. Electron Devices* **ED-26**, 640 (1979).
6. J. W. Coburn, H. F. Winters, T. J. Chuang, *J. Appl. Phys.* **48**, 3532 (1977).
7. W. R. Harshbarger, T. A. Miller, P. Norton, R. A. Porter, *Appl. Spectrosc.* **31**, 201 (1977).
8. A. R. Reinberg and R. Rao, U.S. Patent 4,069,096 (1978).
9. C. J. Mogab and W. R. Harshbarger, *Electronics* **115**, 117 (1978).