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Microstructure Fabrication

Robert W. Keyes

Microstructures, structures imposed on surfaces or thin films that have transverse dimensions ranging between a fraction of a micrometer and several mils (1 micrometer = 10^{-6} centimeter, 1 mil = 2.5×10^{-3} centimeter), are the basic hardware of the vast information processing and transmission industries. All of solid-state electronics, including logic, memory, and switching circuits, is based on "integrated" electronics, the fabrication and interconnection of a large number of very small device structures on a single piece of silicon (*1*).

The success of integrated electronics has several origins. Among these are low power consumption, high operating speed, and high reliability. The power consumption and high operating speed are rather directly associated with miniaturization. Miniaturization reduces capacitances and reduces the time for electrons to travel through a device. While it may not be apparent that miniaturization is an aid to reliability, such has, indeed, turned out to be the case. The small size of the transistor, and especially of the integrated circuit transistor, has made possible new production and assembly techniques. Integrated electronics places a large number of components on a thin slab of silicon about 5 mm square, a "chip," that can be handled as a single unit. Reliability results from the small number of interconnections that must be made by conventional soldering or other bonding techniques, such connections being an important source of failures. The increase in the number of components per manipulable unit has also led to a dramatic cost decrease (*2*).

The author is a member of the research staff at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.

The great reduction in power per device and the greatly increased reliability of solid-state elements combined with lower costs has made possible large increases in the size (as measured by the number of circuits) of electronic systems. The high speed of solid-state circuitry combined with the increase in size that is made possible has led to great increases in the power of large electronic computers. It has also led to the development of small and low cost, but powerful, information processors.

Another class of digital switching systems also provided a major incentive for the improvement of digital systems—the need for a vast number of switches for use in the telephone system. Indeed, the laboratories of the American Telephone and Telegraph Company played a major role in the early development of digital electronics.

The quest for even smaller and more highly integrated devices continues unabated. The central theme of the search for improved digital devices continues to be miniaturization, and the transistor remains the basic device used in electronic switching systems and calculators. The key parameter that measures the status of integrated circuit technology is the area per circuit, or its inverse, the number of circuits per unit area. The historical development of this parameter is shown in Fig. 1, and it can be seen that the area per circuit has been reduced throughout the past decade by a factor of 2 every 3 years (*3*). One is naturally led to wonder how far this curve can be extrapolated.

An almost equal contribution to the increase in the number of components per chip has come from increase in the size of the chip (*3*). Both the increase in the chip size and the miniaturization of the components give rise to many difficult and interesting problems.

Thus, a rather complex engineering art devoted to the fabrication of microstructures has developed. The art involves the use of photo- and cathodolithography, chemical etches, epitaxial growth, ion implantation, diffusion, oxidation reactions, and many other physical and chemical processes (*4*). An example of a complex microstructure is shown in Fig. 2 (*5*).

A major part of the impetus for the development of microstructures has come from silicon microelectronics. But there are many other applications:

- Magnetic bubble devices
- Integrated optics
- Gallium-arsenic (GaAs) microwave devices and circuits
- Acoustic wave devices
- Superconducting devices
- X-ray optics
- Magnetic recording
- Catheters and implantable medical sensors
- Intracellular biological instrumentation
- Displays
- Video recording

Microstructure fabrication is complicated. It requires mastery of many skills, tools, and processes. All of the process steps interact. Fine details, such as the exact vertical profile of a hole created in a masking layer, may determine the success or failure of the next process step.

An example will better illustrate the problems of microstructure fabrication. Consider the fabrication of the structure shown in Fig. 3. Here an n-type region has been created by diffusion of a donor impurity into a surface of p-type silicon, forming a p-n junction diode. There is a metal contact to the n region, and the contact line is insulated from the p-type surface by a layer of silicon dioxide. The diameter of the diode is on the order of 10^{-3} cm.

The fabrication begins with the application of a layer of photoresist to the oxidized surface of a silicon wafer. The photoresist is then exposed to light in the region where the diode is to be formed. Photoresist is a polymeric mixture that is deposited as a thin layer, perhaps 1 μm thick, upon an SiO_2 film on a silicon wafer. Irradiation with light in the near ul-

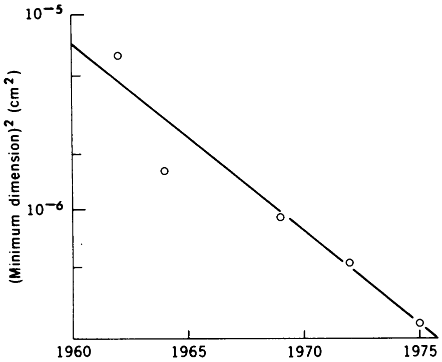


Fig. 1. The area factor in integrated electronics as a function of time (3).

traviolet region of the spectrum modifies the chemical properties of the photoresist and, in "positive" photoresist, makes it more soluble in certain developers. Thus, one step frequently used in microstructure fabrication is the projection of the image of a mask onto the photoresist layer. It becomes possible to remove the exposed region of the photoresist by dissolving it with a suitable developer. The SiO_2 layer can then be removed in the areas that were exposed to light by hydrogen fluoride (HF) etches. The photoresist is resistant to HF etches, and the SiO_2 in the unexposed areas is not affected by the etch. After etching, the remaining photoresist can be removed by a solvent, leaving a silicon substrate covered with SiO_2 only in the unexposed areas. The SiO_2 film acts as a barrier to the contact of impurities in a gaseous phase with the silicon. Thus, when the silicon wafer covered by the patterned SiO_2 film is exposed to, for example, a gas containing phosphorus at high temperatures, the phosphorus, being very soluble in silicon, diffuses into the exposed areas rapidly. An idealized description of this sequence of process steps is shown in Fig. 4. The effect of this doping is very important in electronics, since phosphorus is a donor impurity and a region of n-type or electron conductivity is produced where it is present.

Many physical phenomena, however, obstruct the formation of the ideal structure depicted in Fig. 4g. The technical literature is well supplied with papers devoted to each of the steps illustrated in Fig. 4. None is as straight forward as appears at first sight. It is instructive to discuss them further, since much of the essence of microstructure fabrication is revealed by examining them in detail.

Figure 4a suggests that the thickness of the photoresist and SiO_2 layers are independent of position. While the layer thickness is not an extremely critical process parameter, its control cannot be entirely neglected since the time needed for the subsequent developing or etching steps depends on it. The wafers used in modern silicon technology have diameters of from 2 to 4 inches (1 inch = 2.54 cm), and maintaining uniformity of, say, the temperature at which oxidation takes place across the wafer is not a trivial task.

Figure 4b shows a well-defined boundary between the exposed and unexposed areas of the photoresist. In fact, the dimensions of the structures produced in modern microelectronics are comparable to the wavelength of the exposing light, so that diffraction prevents such sharp contrast from being achieved. Furthermore, high-resolution projection exposure schemes require that the light be monochromatic to avoid the problems of chromatic aberration in the lenses. The photoresist must be reasonably transparent to ensure that the full thickness of the photoresist is exposed to the light. The silicon surface is, however, reflective, so that the interference of the incident and reflected light produces standing waves in the photoresist (6). The resulting spatial periodicity of the exposure of the photoresist is revealed by the scanning electron micrograph of Fig. 5 (7). Complicated effects of this kind are clearly important to microstructure fabrication. It must also be apparent that, as the amount of exposure received is a continuous function of position, the time of development required to remove a given region of photoresist will also be a continuous function, and that the profile of the developed photoresist will depend on the time of development. In particular, the size of the opening in the photoresist, to which Fig. 4 is oriented, will depend on the time.

Development of the photoresist proceeds somewhat as shown in Fig. 6, with simultaneous lateral and vertical removal of material. The tapered edge of the resist film may be a disadvantage, as the exact point at which the film is thick enough to protect the underlying SiO_2 layer during the succeeding etching step, and thus the size of the hole that will be

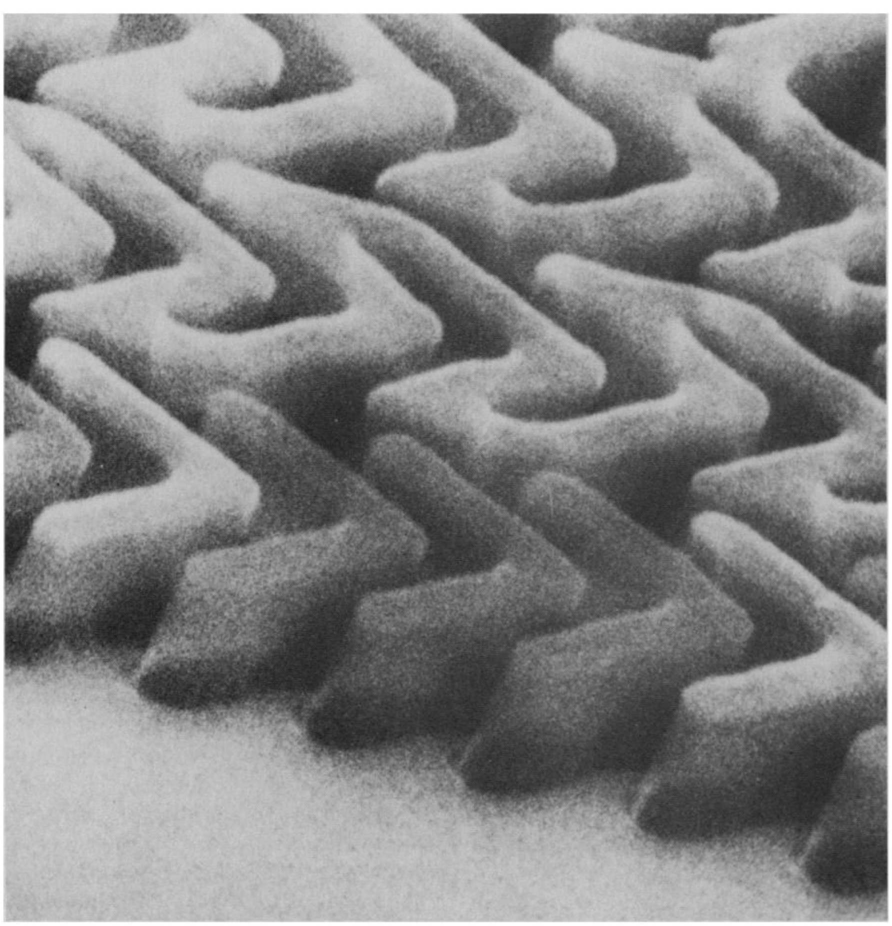


Fig. 2. A pattern developed in photoresist for use as an ion-milling mask (5). The bars are 0.5 μm wide and 1.5 μm high. The mask was used to fabricate permalloy patterns to control magnetic bubbles.

produced in the SiO_2, is not clearly defined. Prolonging the development beyond the point shown in Fig. 6b allows continued lateral development and increase in the size of the opening. Also, however, achieving perfect adhesion of the photoresist film to the SiO_2 is difficult, and the developer may invade the interface between the two layers, producing the undesirable results shown in Fig. 6d.

The developed photoresist, Fig. 4c, is then used as a mask to etch the SiO_2 layer. Again, perfection is hard to achieve. Etching for too short a time will leave a certain amount of oxide in the hole. Etching for too long a time can cause undercutting, as shown in Fig. 7c. After removal of the photoresist, the wafer is exposed to a diffusant, affording additional opportunities for deviations from idealized behavior. Time and temperature of diffusion are important and can produce results resembling Fig. 8, a or b. Diffusion can proceed rapidly along interfaces in certain cases, leading to junction profiles of the kind shown in Fig. 8c. Preferential diffusion along crystalline defects can give rise to a profile resembling that shown in Fig. 8d.

Next, a metal connection is to be made to the diffusion-doped region. Aluminum is frequently used for this purpose because it has high electrical conductivity and does not enter the silicon and alter its properties. The aluminum is also evaporated through a mask that defines the shape and location of the conductor. Examples of the region of contact between the aluminum and the doped semiconductor are shown in Fig. 9. It is seen that the current will be forced to flow through a narrow constriction if the profiles are as shown in Fig. 9b. The high current densities may cause electromigration of the aluminum atoms, leading to the open circuit shown in Fig. 9c.

Also, silicon is somewhat soluble in aluminum. One can thus encounter the situation shown in Fig. 9d, where enough silicon has been dissolved to allow the metal to completely penetrate the doped region, shorting the junction.

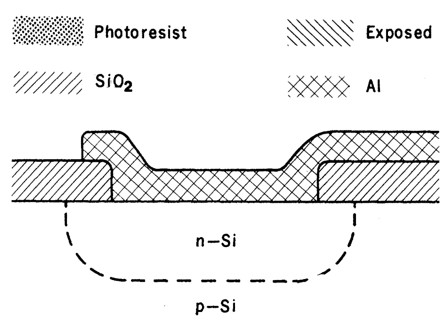
None of the problems illustrated in Figs. 5 to 9 are insurmountable. Many ingenious ways to avoid the difficulties described are known. Sometimes these are guided by physical or chemical knowledge; frequently, however, they are empirical fixes.

The microstructure engineer must also be aware of constraints that have little to do with chemistry and materials science but that tend to be more closely related to mechanical technology. One of the most difficult of these is registration or alignment. A substrate is usually passed through several process steps in order to form a desired structure. For example, fabricating a transistor may involve diffusing a base dopant through a window in SiO_2, subsequently diffusing an emitter dopant through a somewhat smaller opening in an SiO_2 layer, and, finally, using masking layers to form contacts to these transistor elements. It is necessary to ensure that the emitter region is created in the correct position within the previously diffused base region. The mask that is used to define the emitter region lithographically must be precisely located with respect to the geometrical structure already established on the substrate by previous processing steps. This positioning is known as alignment. It may require that separate structures that can be easily located but have no electronic function be provided on the substrate.

Alignment all over a large substrate is made more difficult by dimensional changes that may take place during processing at high temperatures. Materials soften at high temperatures and can deform under the force of gravity or the stresses that accompany temperature gradients and contacts between different materials.

Further, economic factors also constrain the utilization of microstructure fabrication technology. These are the factors that control the cost of production, such as throughput, the rate at which substrates can be processed by the fabrication tools, capital investment required, and demands on operator time and skill. Naturally, all these elements of cost must be weighed against the value of the product produced.

It is common experience in the microstructure art that obtaining reproducible results requires careful control of all aspects of the fabrication processes, such as temperatures, pressures, and time. High standards of cleanliness and reagent purity must be enforced. Seemingly identical apparatuses and starting materials often yield different results.



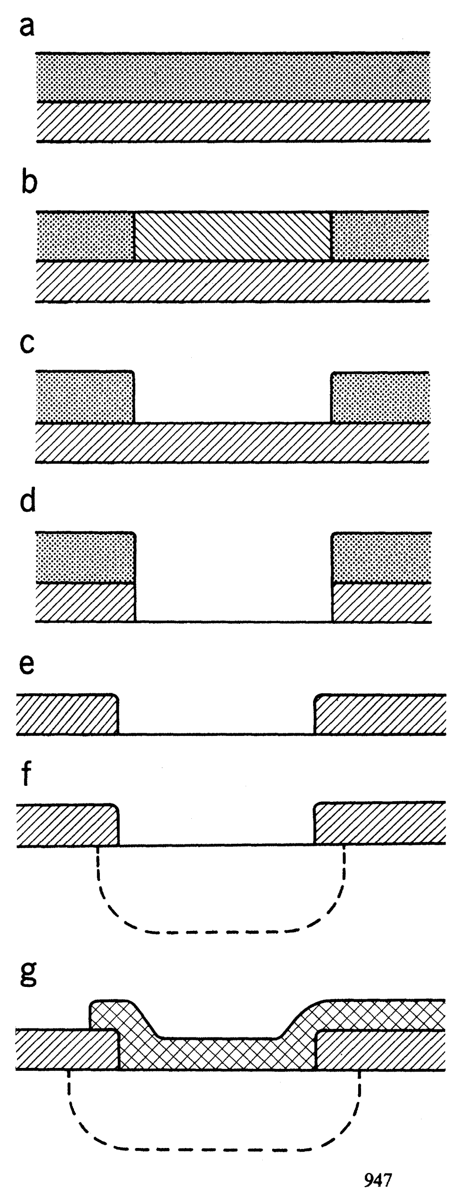
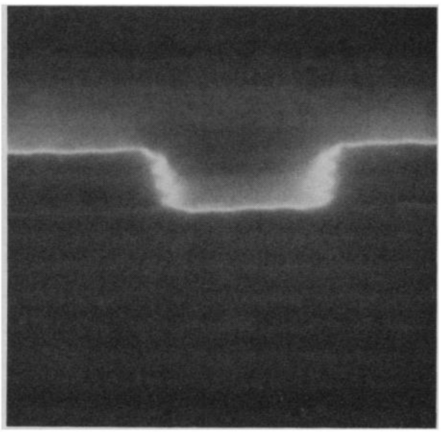


Fig. 3 (left). A diode fabricated on the surface of a wafer of silicon. An n-type region has been created by diffusing a donor impurity through an opening in a layer of SiO_2 on the silicon. Electrical contact is made to the n region by a deposited aluminum conductor. The SiO_2 insulates the silicon from the aluminum. Fig. 4 (right). The process steps that are used to produce the structure shown in Fig. 3. (a) A film of SiO_2 has been formed by oxidizing the silicon, and a layer of photoresist has been deposited on the SiO_2. (b) Shading shows a region of the photoresist that has been exposed to light and thereby made more soluble. (c) The exposed photoresist has been removed. (d) An etchant that reacts with the SiO_2 but not with the photoresist has been used to remove the SiO_2 in the opening created in the photoresist. (e) Another solvent has been used to remove the unexposed photoresist. (f) Donor atoms have diffused into the silicon through the opening in the SiO_2 to produce an n-type region. (g) Additional masking steps, not shown, have permitted aluminum to be evaporated onto the diode in a pattern that forms a contact to the n region of the diode (see Fig. 3 for legend).



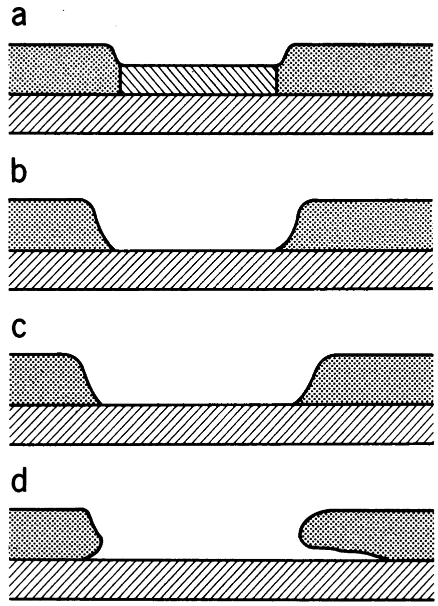


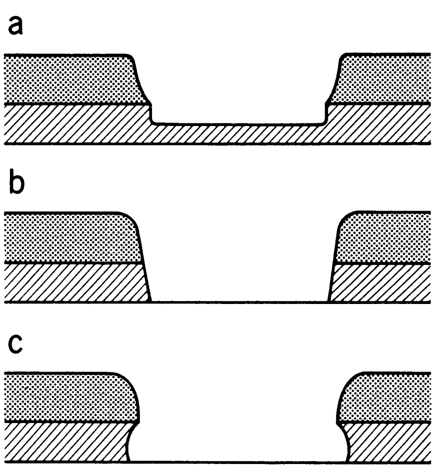
Fig. 5 (left). Standing wave pattern developed in a layer of photoresist (7). Fig. 6 (right). Development of the photoresist. (a) Although exposure increases the solubility of photoresist in the developer, there is only a finite ratio of the rate of dissolution of the exposed photoresist to that of the unexposed region. In addition, the exposure received is not a perfect step function at the boundary of the exposed area. Thus, dissolution proceeds laterally as well as vertically. (b) The opening in the photoresist has penetrated to the surface of the SiO_2. (c) With continued development the opening continues to enlarge. (d) Poor adhesion of the photoresist to the SiO_2 has allowed the developer to penetrate the interface (see Fig. 3 for legend).

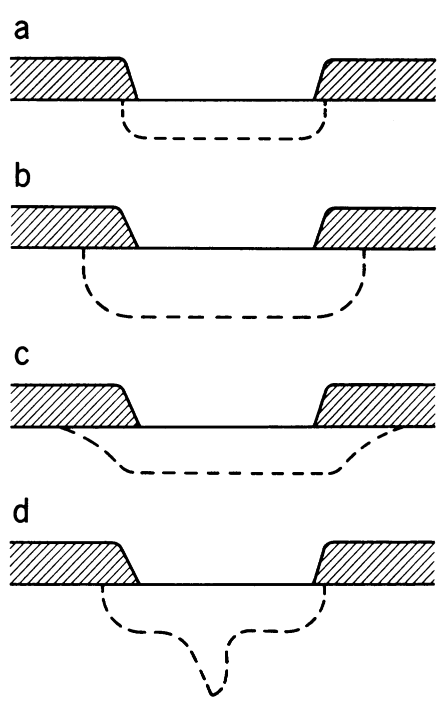
Recipes must be carefully followed, with little understanding of which aspects of a process are critical or what contaminants are important, and why.

The technique of microstructure fabrication has grown up as art in response to a continuous economic and functional motivation to push to the smaller and smaller. Progress has been made by adaptation and invention to meet the needs of the moment. By and large, the art has grown rapidly, adapting and improving old methods to new situations and inventing as needed and possible. The rapid development has outstripped basic understanding of the fundamental mechanisms underlying the techniques. It must be recognized, however, that the optimal exploitation of microstructural technology, the maximization of performance, yields, and utilization of available silicon area will depend on a detailed interpretation of each step in fabrication as a chemical or physical process.

The rush to smaller dimensions has left many unsolved problems in its wake. What chemical reactions are involved in etching? In epitaxial growth? What is the atomic origin of defects in epitaxial layers? What are the photochemical reactions in photoresist? Are there better ones?

Ancient potters, armorers, and jewelers successfully fabricated many useful structures with primitive understanding. Modern microelectronics, however, is not a cottage industry. It is frequently necessary to provide duplicate manufacturing facilities that produce devices or material modifications that can be used interchangeably; that is, it is required that the properties of a structure or device be independent of the facility in which they were produced. One wishes to have the flexibility to redesign a facility to increase its throughput or rate of output. Many process steps are needed, there are numerous opportunities for





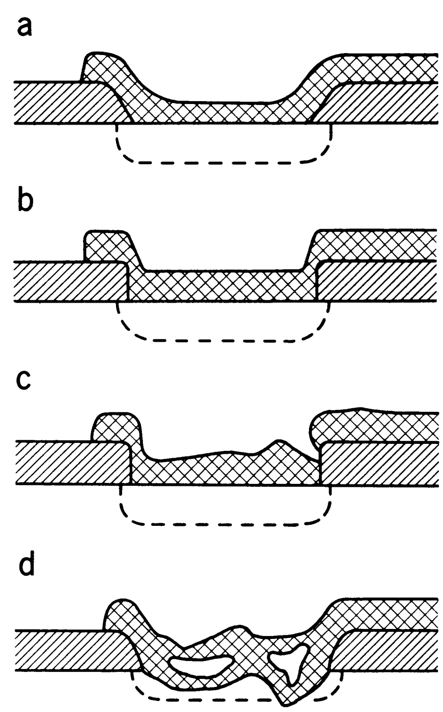


Fig. 7 (left). The opening in the photoresist is used to mask the etching of a hole in the SiO_2. (a) An early stage of development. (b) The opening in the SiO_2 has reached the silicon. (c) Prolonged etching can lead to removal of SiO_2 underneath the photoresist masks (see Fig. 3 for legend). Fig. 8 (center). A donor impurity is diffused into the silicon from a gaseous phase. (a) A shallow n region has been created. (b) Continued diffusion, longer times or higher temperatures, increase the extent of the n region. (c) Surface diffusion has caused spreading of the n region along the SiO_2-silicon interface. (d) A crystal defect, such as a dislocation, has provided a path for anomalously high diffusion and led to penetration of the junction to unanticipated distance from the surface (see Fig. 3 for legend). Fig. 9 (right). (a) Masking steps, not shown, have permitted the deposition of aluminum in selected areas to form a contact to the n region. (b) A sharp vertical profile in the SiO_2 opening may cause a reduction of the cross section of the aluminum conductor where it passes from the SiO_2 insulator to the silicon surface. (c) The high current density in the constriction shown in (b) has led to electromigration of aluminum atoms and opening of the conductor. (d) Solution of silicon in the aluminum has resulted in deformation of the metal-semiconductor interface and penetration of the aluminum through the n region (see Fig. 3 for legend).

something to go wrong, and rapid diagnosis and correction of changes in process results are essential. Analysis of causes of failure in equipment and correction of processes to eliminate the causes is required.

The many gaps in the knowledge of exactly what is happening during the fabrication of a microelectronic device have led to the notion of a "qualified" technology (*8*). That is, large changes in the properties of the devices produced may be caused by small changes in the process, changes that are so small that the process is ostensibly the same, and that may be difficult to detect. Thus, a process technology must be qualified by using it to successfully produce a large number of devices for testing before it can be used to manufacture a marketable product. Only in this way can confidence that a process is capable of providing similar results day after day be established.

However, the uses of microstructure fabrication are so numerous that it is essential to optimize utilization of the technology. In addition, the era of rapid advance through borrowing from other fields and ingenious invention will sooner or later terminate. Until now progress has come easily and it has been possible to neglect the basic chemistry and physics underlying the various arts that constitute microstructure fabrication. The advantages that can be realized from basic understanding will grow in importance, and detailed understanding of the physics and chemistry that limit microfabrication will help to eliminate the barriers. There are difficult and novel problems to solve. But many new analytical tools have entered our laboratories since the dawn of solid-state electronics—lasers, scanning electron microscopes, and the varied apparatus and methods of surface physics, to name a few. We are face to face with a frontier of science.

Upon observing the practice of microstructure fabrication, one cannot fail to notice a resemblance to certain aspects of modern metallurgy. For example, the precipitates produced by metallurgical processing have a dimensional scale similar to that of electronic microstructures. Inhomogeneities on a scale of 10^{-6} to 10^{-3} cm control the desirable properties of a structure. This preoccupation with the properties of solids on a microscopic scale produces a common interest in techniques and in interactions with basic science. Thus, both microstructure fabrication and physical metallurgy: (i) rely on phenomena that take place in the solid state; (ii) depend on analytical tools that are capable of chemical analyses with the highest possible spatial resolution; (iii) involve the motion of atoms through solids, controlled by diffusion, solution, nucleation, and precipitation; (iv) involve interface phenomena at the contact between different solids; and (v) are sensitive to crystal defects.

Table 1. Sales in 1975 of selected industry groups (*9*).

Industry	Sales ($\$10^6$)
Electrical and electronics, office equipment and computer, telecommunications	112
Chemicals, drugs	77
Auto	95
Steel, metals and mining, natural resources and fuels	200

It must further be noted that both metallurgy and microstructure fabrication are practical disciplines; they are oriented toward the economic production of structures that have a useful role in commerce and industry. In this respect, both are engineering rather than scientific disciplines. In contrast, their capability for deep probing of phenomena on an atomic scale and under unusual conditions produces new discoveries and leads to new concepts that enhance basic science. Notions such as dislocations and epitaxy, which were developed by metallurgists, and hot electrons and "hopping" conduction, which grew in electronics, have had profound impacts on the intellectual development of solid-state physics.

This is not to say that microstructure fabrication is a branch of metallurgy. The detailed motivation of the two disciplines is rather different in that metallurgy concentrates on the mechanical properties of solids, whereas microstructure fabrication controls the electronic properties of structures made from magnetic materials, semiconductors, and insulators. The basic difference, of course, is that microstructure fabrication involves control of the fabrication process in detail at the dimensional level of the structure, while metallurgical processing exercises control at a much grosser level. The application of lithography, with the attendant use of exposure tools, clean rooms, resists, masks, and etchants is the province of microstructure fabrication. Crystalline defects are usually undesirable in microstructures; the metallurgist can frequently use them to advantage. Metallurgy also encompasses its extractive aspects. There is no doubt that microstructure fabrication is a distinct activity.

A very rough idea of the economic significance of microstructures is provided by Table 1. Here sales are tabulated by industry groups (*9*). Microstructure fabrication, the heart of modern microelectronics, is an essential ingredient in the electrical and electronics, office equipment and computer, and telecommunications industries, which account for sales of more than \$100 billion.

Viewing the economic significance of the microstructure art and comparing its content as an engineering or scientific discipline to that of metallurgy, one is inescapably led to the conclusion that microstructure fabrication constitutes a discipline that deserves recognition as such. Indeed, such recognition seems inevitable in view of the rapidly increasing role of microstructure fabrication in the world economy. We are on the threshold of a new interdisciplinary field. Chemistry, physics, and empiricism are combined into the creation of novel physical structures that have enormous economic impact, that, indeed, form the basis of whole new industries. Unanticipated phenomena are encountered and inject surprises into basic science. There is here the seed of a new branch of knowledge. Unique opportunities for applied research in the materials sciences exist. There can be little doubt that institutions of higher education will seize this occasion, and that one can look forward to the creation of departments of microstructure fabrication in our universities.

Summary

The development of integrated electronics has given rise to a complicated microstructure fabrication art. There is a need for more basic understanding of the processes that are part of this art. Microstructure fabrication promises to become an independent discipline providing a scientific basis for the art.

References

1. R. F. Petritz, *IEEE J. Solid-State Circuits* **SC-2**, 130 (1967); S. Triebwasser, *Science* **163**, 429 (1969).
2. J. A. Haddad, *Digest of Technical Papers, 1974 International Solid-State Circuits Conference*, (IEEE, New York, 1974), pp. 50–51.
3. G. E. Moore, in *Technical Digest 1975 International Electron Devices Meeting* (IEEE, New York, 1975), pp. 11–13.
4. M. Fogiel, *Modern Microelectronics* (Research and Education Association, New York, 1972); S. K. Ghandi, *The Theory and Practice of Microelectronics* (Wiley, New York, 1968).
5. B. J. Lin, *IBM J. Res. Dev.* **20**, 213 (1976).
6. F. H. Dill, *IEEE Trans. Electron Devices* **ED-22**, 440 (1975).
7. E. J. Walker, *ibid.*, p. 464.
8. P. Aigrain, *ISSCC Digest of Technical Papers, 1976 International Solid-State Circuits Conference*, (IEEE, New York, 1976), p. 49.
9. *Business Week*, 28 June 1976, pp. 62–84.