NANOCOMPUTING
▶LIMITS TO GROWTH

The End—Not Here Yet, But Coming Soon

For years researchers showed up skeptics by cramming chips with more and more transistors. One day the skeptics will be right

Ever since the advent of silicon chips, doomsayers have seen limits to the technology just over the horizon. Challenges in controlling the lithography used in drawing the patterns on the chips and limitations of the materials themselves have loomed as insurmountable roadblocks at one time or another. So far, researchers have found ways around all these obstacles. But this time, many say, real physical barriers may be in sight.

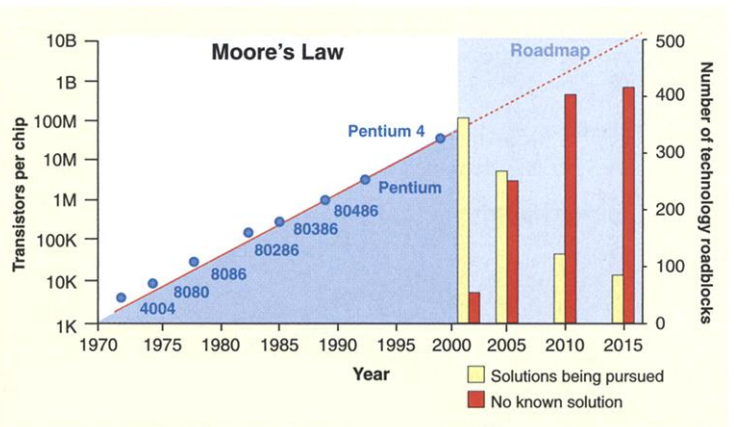
The barriers threaten Moore's Law, the 1965 prediction by Intel co-founder Gordon Moore that manufacturers would double the number of transistors on a chip every 18 months, with resulting declining prices and increasing performance. The semiconductor has stayed on track for 4 decades. But the latest edition of the annual International Technology Roadmap for Semiconductors—a joint effort of semiconductor industry associations in Europe, Japan, Korea, Taiwan, and the United States—lists reasons for thinking that may soon change.

The Roadmap explores "technology nodes"—advances needed to keep shrinking the so-called DRAM half-pitch, half the spacing between cells in memory chips. Currently, the industry is moving to a DRAM half-pitch of 130 nanometers, about three-thousandths the width of the proverbial human hair. The Roadmap forecasts that researchers must lower that figure to 35 nanometers by 2014, simply to continue doubling the number of transistors. In the year 2000 update (available online at public.itrs.net), 12 working groups representing various aspects of chipmaking assess whether those technology node targets can be achieved.

Their conclusions are laid out in dozens of spreadsheets in the Roadmap, giving such arcana of semiconductor production as the wavelength of the light needed in the lithography and the required grain size in the silicon substrates. The spreadsheets are color coded. White cells show technologies in production; yellow ones, known solutions under development; red ones, problems with no known solutions.

The 2000 edition shows plenty of red cells. Experts can't imagine how to get silicon wafer grain sizes down to the 60 nanometers believed necessary for the chips of 2003. Nor do they agree on the lithography methods that will be needed in 2003 (see p. 785).

Despite the red flags, industry officials are confident of finding solutions in time to meet at least the near-term technology node targets. "Historically, the industry has always faced these red areas, but with sufficient research they have all been overcome," says Juri Matisoo, vice president for technology at the Semiconductor Industry Association, a San Jose, California–based industry group.



How much Moore? Problems loom for efforts to pack more transistors on chips.

SOURCES: INTEL, INT'L TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

So far, manufacturers have crammed more transistors into the same space by simply shrinking, or scaling in industry parlance, all of the features of an integrated circuit in roughly equal proportions. But around 2014—the last year the current Roadmap covers—the technology will hit what one researcher says is truly the ultimate "red brick wall": A key feature called the gate oxide will become so thin that it will effectively disappear. "It will be the end of scaling as we know it," Matisoo says.

The gate oxide is a layer of material that separates the chip's gate electrode—which controls the flow of electrons through the device—from the channel through which that current flows. It might be thought of as a wall that keeps electrons traveling down the proper corridor. As the gate oxide gets thinner, electrons are more prone to break out of the corridor and leak away.

Currently this gate oxide is made of silicon dioxide. Experts have long debated just how thin it could get before leakage becomes unacceptable. In what may be a brush with the ultimate limit, last December Intel researchers led by S. J. Lin reported making a standard three-terminal transistor —the architecture used in today's chips— with a gate oxide a mere three atoms thick (see sidebar, p. 786). The little transistor not only works, but it precisely follows the pattern of increased speed and lower voltage requirements that has always accompanied scaling. "It's amazing," says Jason Jenq, head of the front-end processing research program at Semiconductor Research Corp., an industry consortium based in Research Triangle Park, North Carolina, that funds semiconductor research at universities.

"People have always speculated when transistors are going to stop working," says Gerald Marcyk, director of component research at an Intel laboratory near Portland, Oregon. "That's part of the reason we did [this transistor]: I was tired of seeing stories on the end of Moore's Law." But even Marcyk agrees that three atomic layers is the limit for silicon dioxide.

To improve the oxide, researchers are working with materials such as zirconium and hafnium, which are better insulators than silicon dioxide and thus are better at confining electrons. Unfortunately, so far interaction between the silicon substrate and the zirconium or hafnium materials has kept them from achieving their full insulating potential. Jenq says researchers are trying various surface treatments to condition the silicon before the deposition of the zirconium or hafnium. If the problem can be overcome, scaling could continue until about 2010.

Looking farther into the future, researchers are trying to modify slightly the current planar gate architecture, in which the gate is a simple layer of material on top of the oxide which is on top of the conducting channel. One of the most promising approaches is to use a double gate, in which the conducting channel is a small vertical fin with thin vertical layers of oxide and gate material on both sides. Such structures could allow scaling to continue until 2014 or possibly later.

As for what comes next, Jenq says, all bets are off. "It could be molecular devices or single electron devices or something with nanotubes," he says. But it will certainly be something different from what lies at the heart of semiconductors in use today.

–DENNIS NORMILE

With reporting by Robert F. Service.