PERSPECTIVES: DEVICE PHYSICS

Pushing the Limits

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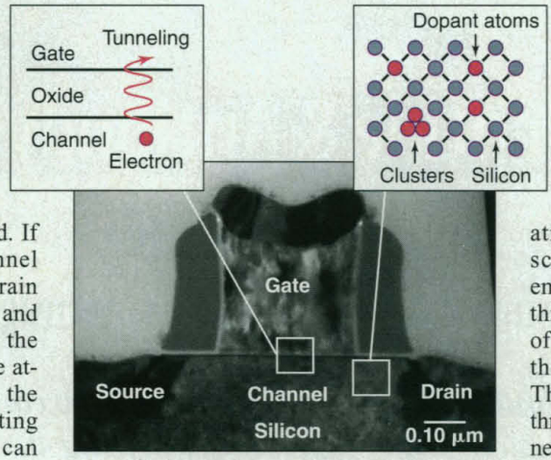
For the past 30 years, the semiconductor industry has followed Moore's law, which states that transistor performance and density double every 3 years (*1*). Although not truly a law, Gordon Moore's statement has yet to be violated. But now it seems to be in serious danger. Fundamental thermodynamic limits are being reached in critical areas, and unless new, innovative solutions are found, the current rate of improvement cannot be maintained.

The dominant electronic device used today in integrated circuits is the silicon-based metal oxide semiconductor (MOS) transistor, which consists of a source, drain, channel, and gate region (see the figure). The source region provides a supply of mobile charge carriers, enabling current to flow from the source to the drain when the transistor is turned "on." The source and drain regions are electrically isolated from one another by an oppositely charged channel region. A controlling gate electrode is separated from the channel by an insulating oxide material. By applying a voltage across the insulating material, an electric field is created. If the applied voltage repels the channel charge and attracts the source and drain charge, a conducting layer is formed, and current can flow from the source to the drain. In contrast, if the applied voltage attracts the channel charge and repels the source and drain charge, no conducting layer between the source and drain can form, and the transistor is "off." The transistor thus acts as a digital switch that is turned on or off by applying a voltage to the gate. Individual switches are combined to form the building blocks for microprocessor and memory chips.

For more than 30 years, the switching speed of the MOS transistor has been increased by reducing the size of the device. For proper operation, MOS transistor scaling theory requires all vertical and lateral dimensions to be scaled simultaneously (*2*). At the same time, the total amount of charge in the source, drain, and channel regions must not decrease in order to maintain low device resistance. Charge in the source, drain, and channel regions is created by locally adding dopant atoms to the silicon lattice. In silicon, each silicon atom is covalently bonded to the four nearest neighbors in the lattice. Adding a dopant atom with five valence electrons increases the mobile charge concentration by donating an unbound electron. A dopant atom with only three valence electrons needs to accept an extra electron to substitute a silicon atom; the localized trapping of the extra electron effectively creates a positive free charge referred to as a "hole." Transistor scaling requires an increase in the concentration of these donor and acceptor atoms to maintain a constant total charge in the source and drain regions.

The dopant concentrations in MOS transistors have increased more than 100-fold over the past 20 years and are on the order of 1% of the silicon lattice density for current device technologies. The maximum thermodynamically stable concentration of atoms in silicon, or solid solubility, varies for different dopant atoms. It is a fundamental thermodynamic property and is not dependent on the method of incorporation of the dopant atoms. Above the solid solubility limit, the dopant atoms begin to interact with each other as a result of electrochemical interactions and the strain fields caused by the atomic size mismatch of the dopant atoms and the silicon lattice. This leads to the formation of clusters of dopant atoms, which are not located on silicon lattice sites and do not increase the mobile charge density (*3*). Unfortunately, the charge concentrations needed for current process technologies are at the solid solubility limit for the dopant atoms currently in use. New dopant atoms have been evaluated, but none have yet been found to create higher concentrations of mobile charge. Thus, unless new methods are developed, future scaling of the transistor will result in a loss of total charge, an increase in resistance, and a potential decrease in performance.



Cross section of a MOS transistor. Electron tunneling through the gate oxide (**left inset**) and high-concentration dopant interactions (**right inset**) are posing fundamental limitations to continuing historical transistor scaling trends.

Scaling of the gate oxide insulating material is facing an equally critical fundamental limit. The gate oxide–silicon system can be thought of as a parallel plate capacitor. By applying a voltage on the gate electrode, charge is attracted or repelled at the silicon interface. Thinning the insulating oxide material increases the electric field and results in a stronger coulombic force, which increases the charge density in the silicon and leads to lowered resistance and improved device characteristics. However, increasing the electric field in the insulating oxide can cause the material to break down, resulting in device failure. For previous technology generations, this has determined the minimum oxide thickness that could be used.

As supply voltages are scaled with each generation, the oxide thickness has been scaled to maintain the same maximum electric field. However, within the last few technology generations, a new fundamental limit to the scaling of the insulating oxide has emerged. The oxide layer has become so thin that quantum mechanical tunneling of electrons from the silicon substrate to the gate electrode is now possible (*4*). The probability of an electron tunneling through a potential barrier depends exponentially on the thickness and potential energy of the barrier. State-of-the-art gate oxide thicknesses are currently between 1.5 and 2.0 nm (*5*). This represents 3 to 4 atomic layers of oxide. At these dimensions, current flow through the gate oxide as a result of electron tunneling becomes substantial. The tunneling process does not appear to damage the oxide, but the resulting gate leakage can cause circuit failures because circuit designs assume no appreciable gate current. Even if circuit techniques can be designed to deal with the leakage, the amount of power consumed will become unacceptably large.

If the insulating gate dielectric cannot be scaled, MOS device performance will be severely degraded. Scaling of the gate dielectric is required not only for the capacitive coupling of the gate to the channel that decreases device resistance; it is also critical for scaling the transistor length. Increased coupling of the gate to the channel allows a

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higher doping density to be used in the channel while maintaining a low resistance when the transistor is switched into the conducting state. This increase in the channel doping density increases the channel barrier, thereby improving the isolation between source and drain when the transistor is turned off. This permits the lateral distance between the source and drain regions to be scaled. Thus, decreased capacitive coupling and inability to scale lateral dimensions may result if oxide thickness cannot be scaled.

Statistical fluctuation is also a potentially fundamental limit for continued transistor scaling (*6*). The transistor dimensions have become so small that the number of dopant atoms that control the electrical characteristics is on the order of a hundred. As a result, small changes in the exact number and distribution of the atoms can cause appreciable changes in the device behavior. The statistical nature of the dopant distribution is inherent to the fabrication process and cannot easily be changed. For very large integrated circuits that can use more than 10 million transistors, this statistical variation can cause serious design problems. Unless ways for reducing statistical variation are found, it may not be possible to scale dimensions to the point where tens of atoms determine the device characteristics.

Solutions for these problems have not yet been found (*7*). It has been proposed that the semiconductor material must be changed to continue transistor scaling. Alternate semiconductor materials such as GaAs and SiGe have been evaluated for more than 20 years, but although these materials have found a niche for certain applications, neither has been able to solve the problems of silicon without causing even more complex problems. Alternate insulating materials for the gate dielectric are also under evaluation. By using an insulating material with a dielectric constant much larger than that of SiO_2, the thickness of the material can be increased while still increasing the capacitive coupling. The increase in thickness would strongly decrease the electron tunneling current and would permit continued scaling of the transistor. Unfortunately, no material with a substantially increased dielectric constant that is also compatible with MOS transistors has yet been found.

A substantial effort is being made to increase charge concentrations by creating metastable states that are far from thermodynamic equilibrium. Processes such as laser annealing and epitaxial growth have been proposed for creating ultrahigh mobile charge concentrations. Unfortunately, these carrier densities are fragile, and the metastable states are extremely difficult to maintain during processing of the device.

These fundamental issues have not previously limited the scaling of transistors and represent a considerable challenge for the semiconductor industry. There are currently no known solutions to these problems. To continue the performance trends of the past 20 years and maintain Moore's law of improvement will be the most difficult challenge the semiconductor industry has ever faced.

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PERSPECTIVES: POLYMER CHEMISTRY

Nanoscale Polymerization Reactors for Polymer Fibers

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The synthesis of a high-performance polymer from inexpensive starting materials usually requires sophisticated polymerization catalysts and postprocessing steps to control the product's morphology and hence its macroscopic properties. Alternatively, expensive monomers can be used to impose morphological order; for example, this is how the bullet-proof Kevlar is made by DuPont. On page 2113 of this issue (*1*), Kageyama *et al.* introduce a "microprocessing" method that may make it easier to achieve high control over polymers made from simple starting materials.

Kageyama *et al.* use a titanocene catalyst supported within the pores of a mesoporous silica for the in situ production of polyethylene with a novel fibrous morphology. The nascent polymer chains cannot fold within the narrow reaction channels of the honeycomb-like support and therefore grow out of the porous framework before they assemble, resulting in the formation of extended-chain crystalline fibers (see bottom panel in the figure). By using regularly arranged nanoscopic, one-dimensional polymerization reactors, the authors thus achieve oriented growth of polyethylene macromolecules that normally requires postprocessing steps.

Earlier reports on mesoporous catalyst systems containing high concentrations of accessible and structurally well-defined active sites indicated their potential for controlling olefin polymerization reactions (*2*, *3*). These investigations also gave first indications of the influence of such catalysts on polymer morphology. Kageyama *et al.*—who coined the term "extrusion polymerization" for their fascinating concept of oriented nanoreactors—demonstrate that conceptually new material properties can result from combining the rational design of organometallic catalysts with nanotechnology.

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The application of porous catalyst supports as microreactors is well-established in industrial processes with fourth-generation Ziegler-Natta catalysts (*4*, *5*). Excellent polymer particle morphology control is achieved by the granule technology, brought to perfection in the Spheripol process of Himont in Italy. In this process, polymerization inside porous catalyst grains results in fragmentation of the grains and formation of spherical polymer granules (see top panel in the figure). An immense improvement of the material strength can be achieved by orienting the crystalline phase of the polyolefin, but this requires expensive postprocessing steps. Bidirectionally extended polyolefin films and ultratough polyethylene fibers, such as Dyneema (which is produced and commercialized by DSM), are examples of oriented, high–molecular weight materials that have tensile strengths up to two orders of magnitude higher than those of standard high-density polyethylene products.

The conventional $TiCl_3$-based Ziegler-Natta catalysts used in the processes described above suffer from structural inhomogeneity of the different reaction centers, resulting in products with broad molecular weight and uneven comonomer distributions. Olefin comonomers are used to alter the crystallinity of the polyolefins to control their properties. This is