for runs 100 through 103 were scaled from figure 1 of (7). The ^{37}Ar rates for runs 104 through 114 were scaled from figure 1 of (35). Data for runs 115, 116, 118 through 122, and 124 through 126 were taken from figure 6 of (1). The average solar neutrino capture rate over all 91 runs used differs slightly from the best average for all the available Homestake data (1); including Homestake data from before the IMP 8 launch gives a different average. In the joint Homestake–IMP 8 data, the average neutrino capture rate is 0.527 captures per day with a standard deviation of 0.315 captures per day.

15. Corresponding values for the solar wind flux are 3.91 $\times$ 10^8 and 0.67 $\times$ 10^8 cm^{-2} s^{-1} for the 91 points used in the two sets. There is no significant skew to either data set.
16. Values from the beginning of 1973 through the end of March 1991 were obtained originally from the Solar Environment Laboratory (National Atmospheric and Oceanic Administration) in Boulder, CO, and were updated through the end of September 1994 with daily sunspot numbers obtained from the National Geophysical Data Center by means of the World Wide Web.
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AFM Fabrication of Sub-10-Nanometer Metal-Oxide Devices with in Situ Control of Electrical Properties

E. S. Snow and P. M. Campbell

Metal wires and metal-oxide-metal junctions were fabricated by anodic oxidation with the conducting tip of an atomic force microscope (AFM). The width of the wires and resistance of the junctions were controlled by real-time, in situ measurement of the device resistance during fabrication. Because the properties of nanometer-scale devices are very sensitive to size variations, such measurements provide a more accurate method of controlling device properties than by controlling geometry alone. In this way, structures with critical dimensions of less than 10 nanometers were fabricated with precisely tailored electrical properties.

The electrical characteristics of device structures with feature sizes of 10 nm or less are extremely sensitive to variations in size. Because of this sensitivity to local geometry, reproducible device characteristics require near-atomic control of the fabrication. Although a few lithographic techniques can produce features in the 10-nm size regime (*1*), it is unlikely that one can achieve reproducible device properties in such small structures through control of device geometry alone. However, the use of a high-resolution processing technique in conjunction with real-time in situ measurement of device properties during critical fabrication steps as feedback for process control should allow the fabrication of devices with features smaller than 10 nm with precisely tailored electrical properties.

To implement such an approach, we need a fabrication process that does not interfere with the measurement of device properties during fabrication. One such process is atomic force microscope (AFM)–based anodic oxidation, a relatively new technique that has proven useful for lithography and device fabrication in the sub-100-nm size regime (*2*, *3*). An electrically biased AFM tip in contact with a surface is used under ambient humidity to produce a local surface oxide. Because the oxidation process produces no measurable current flow between the tip and sample, and because the technique can produce small feature sizes with no proximity effects (*2*), this process is well suited for the tailoring of small structures controlled by in situ electrical measurements.

In this report, we describe the use of in situ electrical measurements to control the fabrication of metal-oxide device structures with feature sizes ~10 nm. We used AFM anodic oxidation of thin Ti films to fabricate fine metal wires and Ti-TiO_x-Ti lateral junctions. Both the wire width and the junction resistance are controlled by in situ real-time measurement of the device resistance. In this way, metal wires with widths of 5 to 10 nm were achieved with predetermined resistance values. Such structures demonstrate the potential of in situ electrical measurements to produce devices of size $\leq$10 nm with precisely controlled electrical properties.

The scanning tunneling microscope (STM) under appropriate bias conditions can be used to selectively oxidize nanometer-sized regions of a H-passivated Si surface (*4*). A similar technique can be used to oxidize the surface of deposited Ti films (*5*); this oxidation process can completely penetrate suitably thin Ti films to produce lateral metal-oxide-metal device structures with variable junction resistance (*6*). Recently, such junctions were used to fabricate a single-electron tunneling device that was operational at room temperature (*7*). Because these and similar structures require feature sizes of order 10 nm, it is necessary to develop fabrication schemes such as de-

Naval Research Laboratory, Washington, DC 20375, USA.

scribed above if reproducible device properties are to be achieved.

To fabricate the wire and lateral oxide junction devices, we first used optical lithography and liftoff to pattern 7-nm-thick evaporated Ti films on a 60-nm-thick thermally grown SiO_2 layer on a Si wafer (*8*). Each metal pattern consisted of a wire (typically 2 to 4 μm in width) connected to large contact pads. After liftoff, the devices were cleaned in chemical solvents, mounted in a chip carrier, and wire-bonded. The bonded devices were then mounted in an AFM (Park Scientific Instruments Universal Ambient AFM). Electrical leads were attached to the chip carrier so that electrical measurements could be made on the devices during AFM operation.

For the oxidation step, we used Si Ultralevers (Park Scientific Instruments). The anodic oxidation proceeds through an electrochemical reaction that is driven by a negative electrical bias applied to the tip in the presence of ambient humidity (*9*). The devices shown here were fabricated in ~40% ambient humidity. The oxidation process does not produce any measurable current flow between the tip and sample and does not perturb the real-time measurement of the electrical characteristics of the device during oxidation. The electrical resistance of the device was used as an automated feedback control over the tip voltage to control both the width of fine metal wires and the resistance of lateral metal-oxide-metal junctions.

With the Si tips, we could oxidize the entire thickness of the Ti film (7 nm) with a tip-sample bias >10 V (the tip is biased negative with respect to the sample). The high resistance of a single metal-oxide-metal junction fabricated in this voltage range (>10^{12} ohms) is evidence for complete oxidation. Smaller biases yield incomplete oxidation and lower junction resistances.

Such exposures to high voltage (>10 V) were used to define fine metal wires from the larger starting structures. First, the tip was biased at −12 V and scanned (scan speed s = 1 μm/s) over a rectangle that covered about half the width of the starting wire. This step restricted the current flow to half the width of the wire along a small section of its length. The tip was then positioned on the unoxidized side of the wire and scanned toward the oxidized region while the device resistance was monitored. During this step, the electrical resistance of the structure increased as the current was slowly constricted by the oxidation (Fig. 1A, inset). At a predetermined increase in resistance (ΔR), the tip voltage was automatically and suddenly dropped to zero, thus establishing a wire of known resistance whose width w was related to ΔR by $\Delta R = (\rho L/T)(1/w - 1/w_0)$, where w_0 was the initial width of the wire, L was the length of the wire, and ρ was the resistivity of the Ti film of thickness T.

Typical data from a measurement of ΔR versus time recorded during the oxidation process [the time is linearly proportional to the wire width, that is, $w(t) = w_0 - vt$, where v is the velocity of the tip perpendicular to the scan direction] are well fit (Fig. 1A) by the simple relation between ΔR and $w(t)$. This particular run was programmed to produce a 15-nm-wide by 500-nm-long wire. Because the oxidation produces a 2- to 3-nm swelling of the film, the Ti oxide can be imaged with the AFM (Fig. 1B). This image shows a narrow opening through the oxide, which has a width that is in approximate agreement with the value predicted by the resistance measurement (*10*). To test the path of the current, we oxidized a small section of the constriction at −12 V, which changed the resistance of the structure from ~10^5 to >10^{12} ohms. Thus, there are no parasitic leakage paths, and all of the current flows through the channel defined by the oxidation.

Both the starting Ti film and the fabricated wires exhibit linear current-voltage (*I-V*) characteristics in the temperature range from 4.2 to 300 K. The only change in the electrical properties caused by the oxidation is an expected increase in resistance resulting from the constriction of the current flow to the narrow channel defined by the oxidized regions.

In addition to the narrow wires described above, it is also possible to fabricate lateral metal-oxide-metal junctions with controlled resistance. We monitored the device resistance while slowly increasing the voltage on the tip during repeated scans across the width of the wire. Above a

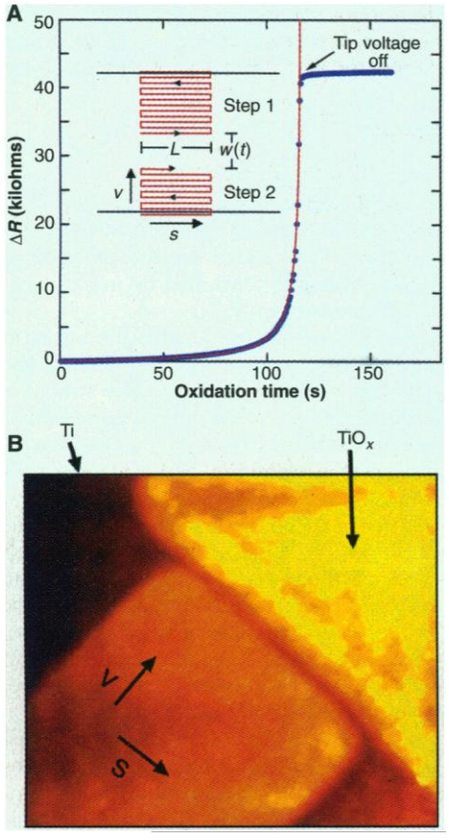

Fig. 1. (**A**) The measured change in device resistance recorded during fabrication of a constriction (blue dots) and a fit to the data (red line) assuming that the width of the constriction is a linearly decreasing function of time. (**Inset**) Diagram of the fabrication process. The wire has a width $w(t)$ as a function of time and a length L, s is the scan speed, and v is the tip velocity perpendicular to the scan direction. (**B**) An 850 nm by 850 nm AFM image of the finished structure. The observed pattern results from the swelling of the oxidized portions of the Ti film. The vertical color scale ranges 10 nm from black to white.

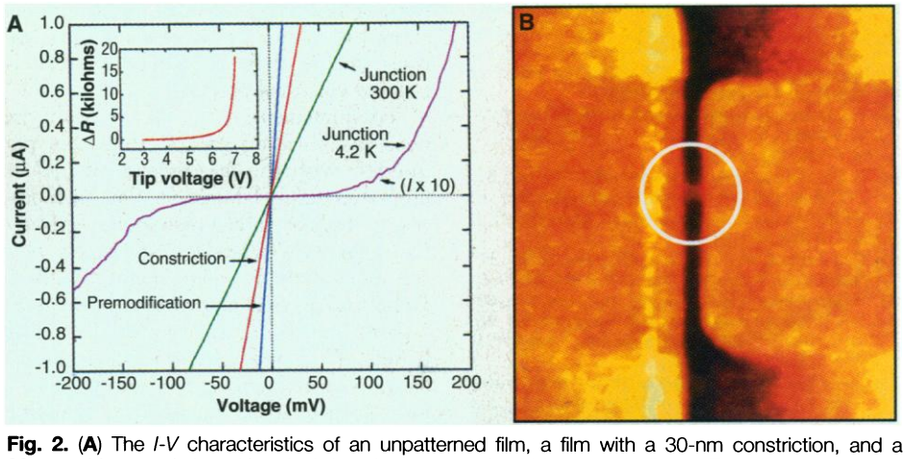

Fig. 2. (**A**) The *I-V* characteristics of an unpatterned film, a film with a 30-nm constriction, and a 30-nm-wide constriction with a single junction measured at 300 and 4.2 K. (**Inset**) The measured change in device resistance recorded during the fabrication of a junction. (**B**) A 900 nm by 900 nm AFM image of the constriction and oxide junction (indicated by the circle). The vertical color scale ranges 4 nm from black to white.

threshold voltage, the oxidation began to increase the wire resistance. When the desired junction resistance was achieved, the tip voltage was dropped to zero (Fig. 2A, inset). The value of the room-temperature junction resistance can be varied continuously, although for high-resistance junctions, the resistance changes rapidly, and it is thus more difficult to achieve a precise predetermined value.

For a single-junction device (Fig. 2B) with moderate resistance ($\sim 10^5$ ohms), the *I-V* curves at 300 K (Fig. 2A) were linear, but they became nonlinear for larger resistance values. At 4.2 K, the *I-V* characteristics exhibited a suppression of the conductivity around zero bias. We found that this low-temperature conductivity suppression is a general property of these lateral junctions. We also observed a correlation between the magnitude of the 300 K junction resistance and both the 4.2 K zero-bias resistance and the voltage range over which the suppression occurs. This suppression indicates a transition from the metallic-like behavior of the unoxidized wire to tunneling through the insulating oxide junction. The low-temperature, low-bias conductivity suppression was observed for all of the samples with lateral oxide barriers.

The fine wires and lateral tunnel junctions form the building blocks from which more complex electronic device structures can be constructed. An example is the single-electron tunneling device fabricated by Matsumoto (*7*), which consisted of a pair of STM-fabricated oxide junctions crossing a 30-nm-wide Ti wire. The ability to fabricate such structures with controlled electrical properties should facilitate the successful application of such devices.

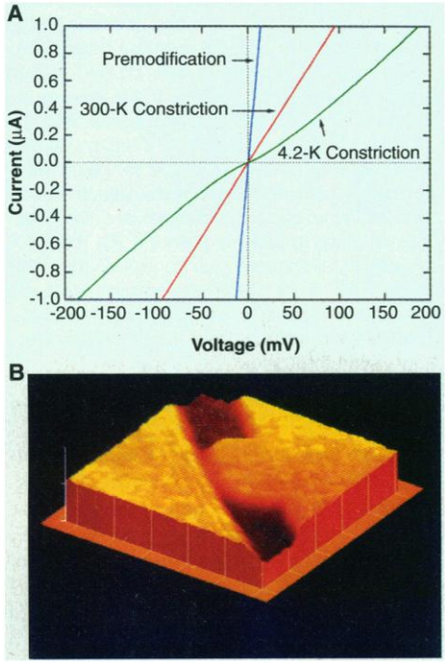

Fig. 3. (**A**) The *I-V* characteristics of an unpatterned film and a film with a constriction of <10 nm measured at 300 and 4.2 K. (**B**) An AFM image of the 120-nm wire and the narrow constriction. The vertical tick marks are spaced by 7.5 nm, and the horizontal tick marks are spaced by 100 nm.

To explore the minimum feature size that can be achieved by this technique, we fabricated a series of successively narrower wires and compared their *I-V* characteristics. We used as our signature of a good wire an *I-V* characteristic at 4.2 K that exhibits little or no zero-bias conductivity suppression, because such a suppression indicates that some portion of the wire has been inadvertently oxidized. To form the narrowest wires, we used a two-stage constriction process. The purpose of the first constriction (1 μm by 120 nm) was to provide a relatively narrow starting structure. Within this narrow region of the first constriction, we formed the second constriction by using only very fine tip translations. In this second constriction, the width was reduced by 0.5 nm with each successive scan, which resulted in fine control of the resistance of the constricted wire. The final result was a 200-nm-long wire of extremely narrow width (Fig. 3B). The narrowest wire we have fabricated by this technique was obtained with a resistance increase that corresponds to a final wire width of 3 nm. The *I-V* characteristics of this device (Fig. 3A) show only a slight suppression of the zero-bias conductivity at 4.2 K, which indicates that the 300 K resistance is not dominated by oxide junctions extending across the wire.

For such narrow wires, the resistance measurement may lead to an underestimate of the actual geometric width. One indication of this is that the in situ resistance data were no longer fit by a simple linearly decreasing wire width. This error could have resulted from a variety of sources, most important of which may be nonuniformities caused by the grain size of the metal film. Although the linearity of the *I-V* characteristics indicated no dominate oxide junctions, the finite grain size of the metal produces nonuniformities of similar size in the oxide (Fig. 3B). These nonuniformities lead to width fluctuations that may dominate the resistance and result in an underestimation of the average width of the wire. Further reductions in size will require more uniform metal films. Additional errors could arise because the intrinsic resistivity of Ti increases as the film is constricted to very narrow dimensions. Such a change in resistivity in long, narrow wires has been noted by researchers who formed small metal wires by pressing an STM tip into a metal substrate and slowly retracting it (*11*).

An AFM image from after oxidation (Fig. 3B) indicates that the swelling from the oxidation just bridges the channel for this particular structure. This contrasts with the device in Fig. 1, which has a 15-nm-wide effective electrical width and an ~10-nm-wide gap in the surface swelling. Although this gap cannot be seen in the images of the narrowest wires, the lack of significant zero-bias conductivity suppression indicates the presence of an unoxidized Ti wire buried beneath the surface oxide. On the basis of the AFM images and the resistance data, we estimate this wire to be between 5 and 10 nm wide. The electrical properties of these devices have been precisely and controllably determined, although their geometrical dimensions are not measurable to this precision.

We have combined proximal probe-fabrication techniques with in situ electrical measurements to produce 5- to 10-nm-wide metal wires and lateral metal-oxide-metal junctions with controlled electrical properties. The ability to fabricate structures in this size regime with such finely tailored electrical properties may allow the realization of useful devices whose operating characteristics are critically dependent on device geometry but for which control of geometry alone would be difficult if not impossible to achieve by conventional nanofabrication methods.

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10. The exact dimensions of the wire are obscured by several effects. First, the AFM image indicates a rounding of ~20 nm in radius at the edges of the oxide; this rounding is the result of both an actual rounding of the oxide edge and tip convolution effects. Second, the profile of the oxide below the surface is unknown. These effects lead to an uncertainty in the width of the electrically active region. In this size regime, the electrical measurements appear to be the more accurate estimate of the width. For constrictions down to 10 to 20 nm, the resistance data are well fit assuming the wire width decreases linearly with time. Consequently, we take as our estimate of the width the value established by the resistance.
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