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7. The ammonium and nitrate series can only be interpreted after annual snow accumulation rate measurements have been calculated for the GISP2 ice core because, unlike the other species measured in this study, ammonium and nitrate flux (accumulation times concentration) series differ notably from their concentration series (*3*) as a consequence of the depositional and postdepositional processes that are unique to these species (*19*).
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Gallium Arsenide Transistors: Realization Through a Molecularly Designed Insulator

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A GaAs-based transistor, analogous to commercial silicon devices, has been fabricated with vapor-deposited cubic GaS as the insulator material. The *n*-channel, depletion mode, GaAs field-effect transistor shows, in addition to classical transistor characteristics, a channel mobility of 4665.6 square centimeters per volt per second, an interfacial trap density of 10^{11} per electron volt per square centimeter, and a transconductance of 7 millisiemens for a 5-micrometer gate length at a gate voltage of 8 volts. Furthermore, the GaAs transistor shows an on-to-off resistance ratio comparable to that of commercial devices.

Gallium arsenide (GaAs) has over the last decade become the semiconductor material of choice in a number of "niche" applications: for example, optoelectronics [lasers and light-emitting diodes (LEDs) for optical communications and consumer electronics], microwave monolithic integrated circuits (MIMICs) (used in wireless communications such as cellular telephones), and very high frequency analog and digital signal-processing circuits (used for high–data-rate real-time processing) (*1–3*). However, except for specialty, primarily military, applications, GaAs has been unable to compete with silicon technology in the area of digital electronics.

At present, logic circuits, such as those used in the central processing unit of a modern personal computer, are based on silicon complimentary metal-oxide-semiconductor (CMOS) circuits, the basic component of which is a metal-oxide-semiconductor field-effect transistor (MOSFET) (*4*). Requirements for the development of the next level in digital electronics include greater speed, lower power consumption, and the incorporation of optoelectronics directly into the circuits (*5*). It has long been known that GaAs and related III-V compound semiconductors are faster than silicon (up to six times), and because of their direct band gap, they have the potential for the development of on-chip optoelectronics. However, present GaAs technology in the field of digital electronics (logic circuits) is limited by the inability to manufacture a GaAs analog of a MOSFET device, that is, a metal-insulator-semiconductor FET (MISFET) (*6*).

Present GaAs FET devices are metal-semiconductor FETs (MESFETs), which while faster than silicon MOSFETs suffer from several drawbacks. First, MESFETs consume more power than MISFETs. The undesirable power consumption is one of the barriers to very large scale integration (VLSI) of GaAs-based circuits. Second, the lack of any insulator between the gate and the channel results in large current conduction through the gate electrode. To circumvent the problems of current leakage across the gate, device architects must implement highly intricate and complex circuit designs. Because both of these problems are inherent in MESFET devices and are not readily solved, the entry of GaAs into the mainstream of high-performance digital electronics has been inhibited. To overcome the limitations of both silicon MOSFETs and GaAs MESFETs, it is thus necessary to develop GaAs-based MISFET devices.

The MISFET was first proposed in the 1930s by Lilienfeld (*7*) and Heil (*8*). We acknowledge earlier attempts to produce a GaAs MISFET (*9*), but a combination of either poor gate passivation (*10*) and insulating properties (*11*) or processing difficulties have precluded its realization (*12*). An ideal gate material for a MISFET device would have the following properties: a high band gap (insulating) material with low electrical conduction, a large breakdown field, good chemical and operational stability, and good interface properties with the chosen semiconductor (*13*). Furthermore, the following properties, although not nec-

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essary, would be desired: a crystal lattice and coefficient of thermal expansion matching those of the semiconductor, good thermal conduction, and a material that could be readily fabricated within current industry standards. In the case of silicon, the native oxide (silica, SiO_2) admirably fulfills these requirements, but GaAs does not grow a suitable oxide (*14*). Attempts to apply silicon technology have failed (*15*) because, although insulating materials with low electrical conduction may be deposited on GaAs, the presence of electronically active interface states considerably reduces the efficiency of the GaAs surface as a charge carrier. Thus, if a new material is to be designed for the gate of a GaAs MISFET, it must reduce the number of interface states, that is, it must passivate the surface of GaAs (*16*).

We recently reported the metal organic chemical vapor deposition (MOCVD) of a metastable face-centered-cubic phase of gallium sulfide (GaS) (*17*). The growth of a cubic phase of GaS, rather than the thermodynamically stable, hexagonal layered structure (*18*), is determined by the use of the predesigned molecular motif present in the single-source precursor, $[(t\text{-Bu})GaS]_4$ (Fig. 1). This molecularly designed cubic phase of GaS exhibits a large band gap (>3.5 eV), forms a nearly lattice-matched layer on GaAs, and has a low electrical conduction ($\approx 2 \times 10^9$ ohm·cm). This phase also successfully provides electronic passivation of the surface of GaAs (*19, 20*). Cubic GaS would thus appear to be suitable as a gate material for a GaAs MISFET.

We have realized a class of GaAs FET through the use of molecular control over the growth of the insulating gate material (Fig. 2). Because our goal was to demonstrate the feasibility of the GaS-GaAs FET, rather than fabricate a device with optimum features, and because the methodology for the processing of cubic GaS was unknown, we kept the fabrication steps simple and the device geometry large in order to have a reasonable fabrication yield (*21*). The use of simplified processing reduced the chance of a GaS-related processing error destroying all of the devices in a fabrication run.

Deposition of cubic GaS was performed in an atmospheric-pressure horizontal-flow hot-walled MOCVD chamber, as previously described (*18*): Argon was used as a carrier gas, the precursor $[(t\text{-Bu})GaS]_4$ was sublimed at 220°C, and the substrate was heated to 390°C. A film of GaS 500 Å thick was grown on a previously prepared epilayer and subsequently etched to 300 Å. The epilayer consisted of a 0.5-μm layer of *n*-type GaAs (Si-doped, $N_D = 4 \times 10^{16}$ cm^{-3}) grown on 0.8 μm of undoped GaAs, which acted as a buffer region to the semi-insulating GaAs

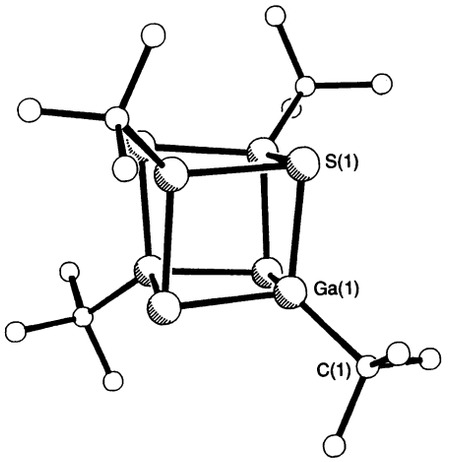

Fig. 1. The molecular structure of $[(t\text{-Bu})GaS]_4$, the single-source precursor responsible for the MOCVD growth of cubic GaS. Hydrogen atoms have been omitted for clarity.

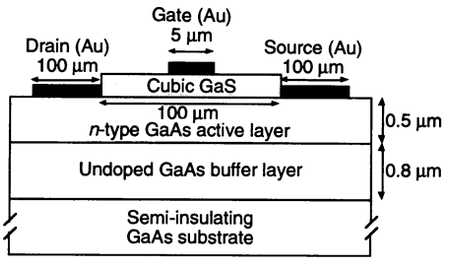

Fig. 2. Schematic diagram of the GaS-GaAs FET; not to scale.

substrate (Fig. 2). Both the active and buffer regions were grown by molecular beam epitaxy. The cubic GaS grows on (100)GaAs in a near-epitaxial manner (*19*), such that only the {200} and {400} reflections are observed by x-ray diffraction. The individual FET devices were isolated by mesa-etching, whereas contact photolithography was used to define the device mesas as well as the source, drain, and gate contacts. The GaS was removed from the source and drain contact areas before metallization by acid etching (Fig. 3). The devices have a 5-μm-long gate, and gold was used as the gate metal. The device processing yield was ~40%. Failure of the gate metal to stick to the GaS was the main processing failure. To obtain the necessary parameters of the channel (such as mobility and channel depth) and provide a direct comparison between our GaS-GaAs FET and a standard GaAs MESFET, we fabricated both devices using identical procedures and masks. Both types of device were characterized by capacitance (*C*) versus voltage (*V*) and current (*I*) versus voltage measurements.

The behavior of the drain-to-source current versus voltage (I_{DS}-V_{DS}) curves at different applied gate voltages (V_g) are close to that of an ideal transistor (Fig. 4); the transconductance of the transistor shown in Fig. 4 at $V_{DS} = 8$ V and $V_g = -5$ V is 7 mS. This value is calculated from the data in Fig. 4, taking into account the series resistances of the drain-gate and source-gate paths by standard procedures. Additionally, a channel mobility of 4665.6 cm^2 V^{-1} s^{-1} was determined, comparable to the values for MESFETs and near the textbook value for GaAs (4700 cm^2 V^{-1} s^{-1}). The transistor characteristics shown in Fig. 4 are typical of those obtained from the better of the GaS-GaAs FETs fabricated, the worst having values for the transconductance ~50% of the above values, the best being around 20 mS.

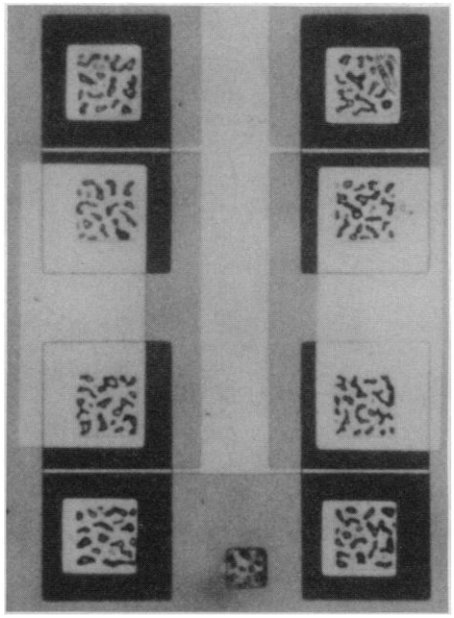

Fig. 3. An optical micrograph of four GaS-GaAs FETs after fabrication.

By comparing the I_{DS}-V_{DS} curves for the GaS-GaAs FETs and the GaAs MESFETs, we determined that there exists an effective negative charge density (10^{-6} C cm^{-2}) at the GaS-GaAs interface in the former. As a consequence, the transistor threshold voltage obtained for the GaS-GaAs FETs was −6 V (extrapolated to $V_{DS} = 0$ V); although this is acceptable for a developmental device, it is somewhat larger than desired.

To obtain information regarding the GaS gate insulator, we performed high-frequency (100-kHz) *C*-*V* measurements on the Au-GaS-GaAs structure. The resistivity of the GaS ($\approx 10^9$ ohm·cm) was comparable to our previously measured values [2×10^9 ohm·cm (*18*)], and the maximum interface trap density (D_{it}) was 9×10^{10} eV^{-1} cm^{-2}. This interface trap density, although acceptable from the device operation point of view, can be improved with a decrease in imperfections in the GaS film (see above). The gate capacitance was

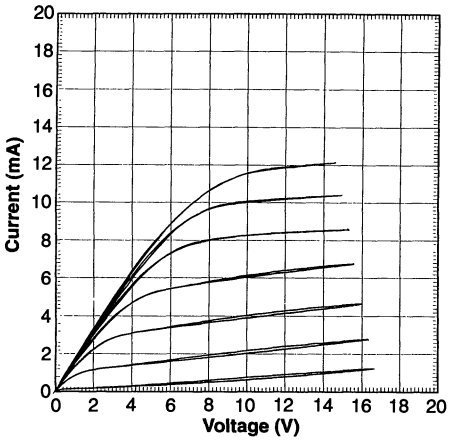

Fig. 4. The drain-to-source current (I_{DS}) as a function of the drain-to-source voltage (V_{DS}) at different gate biases (V_g, 1 V per step) for a typical GaS-GaAs FET.

≤1.6 pF, consistent with 300 Å GaS with a relative dielectric constant of 11.

The molecular design of a cubic phase of GaS allows for the fabrication of a new class of GaAs transistor, what we term a FET with an insulating sulfide heterojunction. This device is in the general class of a MISFET and represents the first step toward the realization of a III-V analog to the commercial silicon MOSFET device. These GaS-GaAs devices have isolation between the gate circuit and the source-drain circuit superior to that of GaAs MESFETs of comparable geometry. In contrast, the lack of any insulator between the gate and the channel in MESFETs results in large current conduction through the gate electrode. In addition, the GaS-GaAs FETs show better on-off switching properties, as measured by the resistance ratio, than MESFETs under comparable operation conditions. Our experimental data demonstrate that, even without optimization, the cubic phase of GaS can be used to construct a GaAs MISFET with good transconductance and input-to-output isolation and acceptable dc characteristics. A further advantage of cubic GaS lies in its method of growth, MOCVD, the accepted method of growth of GaAs-based devices. Thus, the ability to grow a gate insulator layer by the same methodology is a distinct advantage of cubic GaS as a potentially viable material for the enablement of GaAs digital devices. This cubic GaS insulating phase should make it possible to design new types of III-V–based devices.

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Diamond Coating of Titanium Alloys

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A titanium alloy was coated with a thin layer of synthetic diamond by chemical vapor deposition methods, achieving exceptional adhesion. Scientific and technological opportunities exist for the development of diamond-coated metal alloys and for a better understanding of adhesion mechanisms of hard, brittle coatings. An indentation method of wide applicability for measuring the adhesion of such coatings is discussed.

There has been considerable effort in recent years in the development of bonding technologies for metal and ceramic materials to produce strong interfaces of known mechanical reliability with a major emphasis on obtaining quantitative measures of adhesion (*1*). These efforts have necessarily crossed several science and engineering disciplines, including chemistry, materials science, and mechanics. Such attention arises from the increased use of metals with ceramics in high-technology applications from turbine engines to microelectronics. For example, advanced electronic packaging involves numerous metal-ceramic couples for device attachment and interconnections with chip carriers (*2*). In this application, thin metal films are deposited on a ceramic substrate. Problems in reliability may arise with ceramic packaging as with other metal-ceramic bonds because of materials processing or temperature changes in fabrication and use (such as heat generated by an electronic device). The large residual stresses that result may cause failure of the interface, substrate, or film. Specifically for the thermally induced stresses in a film or coating, σ_{th}, the magnitude scales with differences in the coefficient of thermal expansion, $\Delta\alpha$, and with temperature change measured from the stress-free state (usually the processing temperature), ΔT, by

$$\sigma_{th} \approx E\Delta\alpha\Delta T \quad (1)$$

where E is the film's Young's modulus.

These issues of reliability associated with metal-ceramic systems are greatly exacerbated for the related problem of synthetic diamond thin films deposited on metal substrates. In this case, enormous residual (thermal) stresses arise from large thermal expansion differences ($\Delta\alpha \sim 5 \rightarrow 10 \times 10^{-6}$ K^{-1}) and from an extreme value of the Young's modulus of diamond ($E \sim 1000$ GPa). The magnitude of the stress can be expected in this system of materials to exceed several gigapascals of compression.

Despite the large stresses expected for diamond-coated metals, a thin diamond layer is usually sought for many applications because of its extreme hardness, stiffness, thermal conductivity (at room tempera-

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