

Future Beam-Controlled Processing Technologies for Microelectronics

DIETER P. KERN, THOMAS F. KUECH, MODEST M. OPRYSKO,
AL WAGNER, DEAN E. EASTMAN

Beam-controlled processes that utilize photons, electrons, ions, and molecules have become essential in the fabrication of microelectronics. These processes are required for the deposition, patterning, etching, and characterization of semiconductor, packaging, and processing-related materials that form the basis of the integrated circuit. Fabrication techniques demand an increasing precision as the physical size of the device structures shrink to submicrometer dimensions. In this article, selected examples of beam-controlled processes expected to be important in the microelectronics industry are described. The continued rapid advances in microelectronics technology that underlie the electronic information-processing industry require the continued development and refinement of these new techniques.

HISTORICALLY, PERHAPS THE MOST SIGNIFICANT INDUSTRIAL development has been that of the electronic information-processing industry. The phenomenal growth of this \$400-billion electronics industry rests upon microelectronics technology, which can be traced to the invention of the transistor 40 years ago, followed by the invention of the monolithic integrated circuit 30 years ago. The semiconductor industry is perhaps the only industry that reports its progress on a logarithmic scale. In 1958, a chip contained a single circuit; today, chips contain as many as 10^6 memory bits or about 10^5 logic circuits. Such microelectronics advances have been the major contributor to the 20% to 30% reduction in the cost of computing per year over the past three decades. Looking to the future, continued progress is expected for at least the next decade. However, progress will not be easy, and continued microelectronics technology advances with increasing complexity are required to maintain this progress. In this article, we describe a number of beam-controlled processing technologies that will likely be important for future microelectronics. In particular, we consider selected examples of beam-controlled processing that use photons, electrons, ions, and molecules. Such beam-controlled processes are essential in the fabrication of microelectronics technologies including silicon technologies, compound semiconductor technologies, packaging technologies, optoelectronics technologies, and so forth. This review is not exhaustive and we have not emphasized areas that are primarily of scientific interest or have a narrow range of application.

The authors are at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598.

Photon Beams

Photon beams, ranging from the infrared spectrum to the x-ray spectrum, are used extensively in the production and characterization of integrated circuits (ICs) and packaging components. Characterization techniques range from optical microscopy and inspection to x-ray diffraction and topography, while fabrication techniques range from optical lithography through surface etching and deposition. In the following, selected examples of photon beam lithography with broad photon beams and focused photon beam microprocessing are described.

Photon beam lithography. Lithography technology is used to define and form the patterns of the various layers and features in semiconductor integrated circuit chips and is the most frequently used process as well as the most expensive IC manufacturing technology.

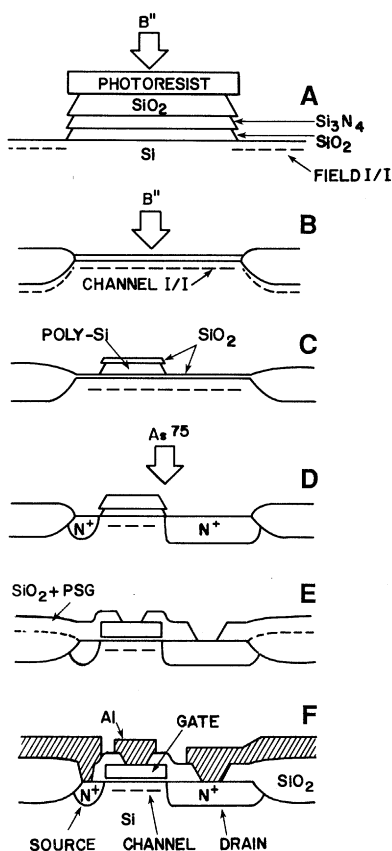


Fig. 1. Steps in the n-MOS FET fabrication process. These small transistors typically require lateral and vertical dimensions less than a few micrometers. Most of these processes utilize a beam-related or -assisted technology in achieving such small structures. (A) Multilayer SiO_2 , Si_3N_4 , and photoresist films are deposited. The FET channel, which is the device active region, is patterned. Boron-11 is ion implanted for isolation between devices. (B) Field oxide is grown for dielectric isolation between devices. SiO_2 and Si_3N_4 films are removed. The doping in the channel is adjusted by ion implantation. (C) SiO_2 is grown for the gate insulator. The polysilicon gate is formed by deposition and patterning. (D) Arsenic-75 is ion implanted to create n-type source and drain regions. (E) Interelectrode oxide (SiO_2 and phosphosilicate glass) is deposited to provide electrical insulation between wiring and the underlying devices. The ohmic contact holes are patterned and formed at the source and the drain. (F) Aluminum interconnect wiring to the source, drain, and gate of the FET is deposited and patterned (one level is shown).

connect wiring to the source, drain, and gate of the FET is deposited and patterned (one level is shown).

Optical lithography is the predominant patterning technique used in IC chip fabrication. Indeed, the complexity of various microelectronics fabrication processes is often measured in “mask levels.” (The simple n-MOS process in Fig. 1 has four mask levels.) Optical lithography is currently being practiced with resolutions down to about 1 μm , which is required for fabricating 1-megabit dynamic random access memory (DRAM) chips. In the future, it is expected that optical lithography technology will be extended over the next decade to about 1/3- μm resolution, which will be sufficient to fabricate 100-megabit DRAM memory chips (such chips will store about 5000 typewritten pages of text).

Since the late 1970s, optical projection lithography has replaced proximity and contact printing in microelectronics fabrication owing to advantages in dealing with mask defects, contamination, and so on. Optical projection printers, both step-and-repeat and wafer scanner types, consist of a photon source and lens system that images a mask containing the pattern onto the semiconductor wafer. A broad beam containing the pattern information is projected onto the wafer with an area $\geq 1\text{ cm}^2$ and a large full angle of impinging rays ($\text{NA} = \sin \theta = \text{numerical aperture}$) which corresponds to using a large solid angle of the rays leaving the source. In this way, a very high processing speed, or throughput, is achieved compared with focused beam techniques carried out with photons, electrons, or ions.

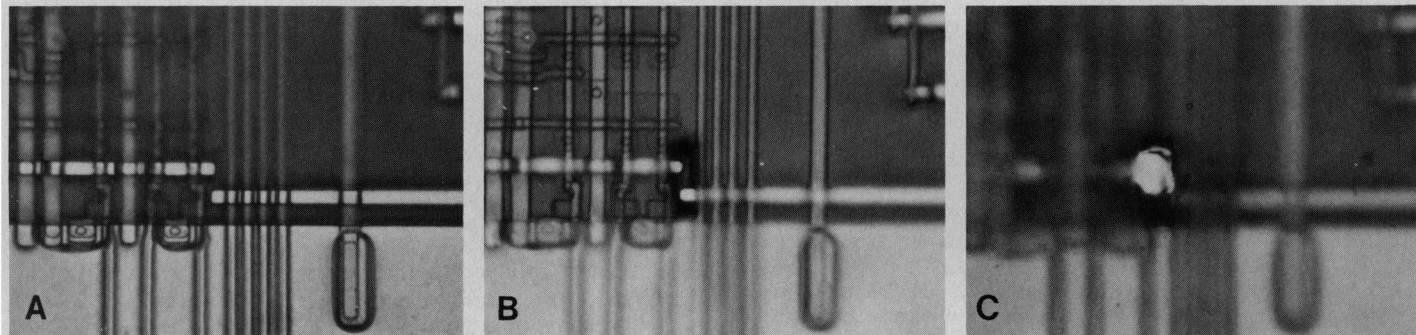
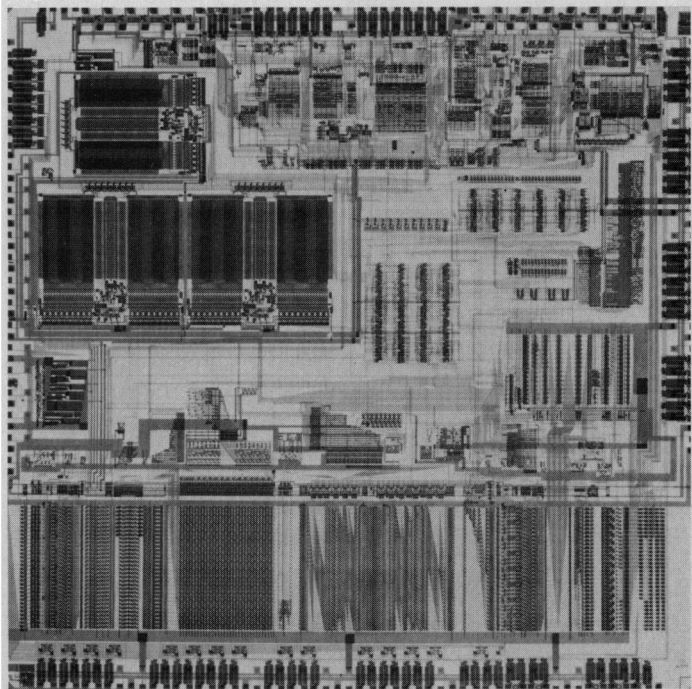


Fig. 2. The IBM $\mu\text{m}370$ chip (top) and sequential repair of routing error, that is, open wire (A), by laser microcutting through chip “passivation layer”

Table 1. Lithography sources and their resolution limits.

Source	Resolution limit* (μm)	Manufacturing availability†
Mercury arc lamp (H-line, 0.437 μm)	~ 0.8	Now
Mercury arc lamp (I-line, 0.365 μm)	~ 0.6	~ 1988
KrF excimer laser ($\lambda = 0.248\text{ }\mu\text{m}$)	~ 0.35	Early 1990s
X-ray storage ring ($\lambda \sim 0.001\text{ }\mu\text{m}$)	~ 0.15	Early to mid-1990s
Focused electron beam	≈ 0.1	Early to mid-1990s

*Approximate system-resolution limit in manufacturing. †Estimated times of availability for manufacturing. Focused electron beam systems within a 1- μm resolution are currently available. Relative throughputs of optical and x-ray systems are roughly comparable, whereas that of e-beam systems are about 100 times lower.

Table 1 summarizes important photon sources and their approximate resolution limits, throughputs, and manufacturing availability dates, together with a future state-of-the-art focused electron beam source. For optical sources, the resolution limit, or minimum printed linewidth, ℓ , is given by $\ell \approx 0.8\lambda/\text{NA}$ (1), where λ is the wavelength and the numerical aperture, NA, lies in the range $0.35 < \text{NA} \leq 0.55$. An additional important parameter for optical sources is the depth of focus, d , which is $d \approx \pm 0.25\lambda/(\text{NA})^2 \approx \pm \lambda$. Thus focusing becomes increasingly more difficult as resolution improves (smaller λ and larger NA), and shorter λ is preferred instead of larger NA for improving resolution because this maintains the largest possible depth of focus. Microelectronic lenses for projection printers are very complex, typically containing 20 or more optical elements, and require extreme precision (lack of optical aberrations, for example) owing to the large information content they must project. For example, a microelectronic lens contains about 25,000 lines/field of pattern information compared with about 500 lines/field for a television screen.

Optical lithography sources are expected to be available for resolutions down to about 0.35 μm and will be extensively used well into the 1990s (Table 1). Sources that can provide better resolution include x-ray and electron beams. Electron storage rings ($\lambda \approx 0.001\text{ }\mu\text{m}$) can provide an intense beam of “soft” x-ray (average $\lambda \approx 10\text{ }\text{\AA}$ or 0.001 μm) that reduce diffraction effects and thus permit improved resolution as well as larger depths of focus. These promising x-ray sources together with x-ray step-and-repeat printers and mask technologies are being developed in the United States, Germany, and Japan for lithographic fabrication of structures with dimensions less than 0.5 μm . The electron beam lithography source summarized in Table 1 is described later in this article.

The advent of high power excimer lasers has made possible direct projection processing in which mask patterns are directly formed in thin-film layers of insulators, metals, or semiconductors by etching (for example, by ablation) or deposition. For example, this technique appears promising for directly patterning polymer insulators used in microelectronics chip packages. Patterned metal films of aluminum (used for chip wiring) have been demonstrated with a resolution approaching $2\text{ }\mu\text{m}$ (2).

Focused photon beam microprocessing. An emerging photon beam technology is focused photon beam microprocessing. Focused photon beam microprocessing can be thought of as a laser-driven process that results in the modification of a surface in a micrometer-size area. The surface modifications are of particular interest to the microelectronics industry when such surface modifications result in the deposition of material or the etching, doping, or oxidation of a surface. These surface modifications can be induced by physical or chemical processes or a combination of both by means of infrared (CO_2 , diode, Nd:YAG), visible (argon ion, krypton ion, helium-neon) or ultraviolet (excimer, frequency-doubled argon) lasers.

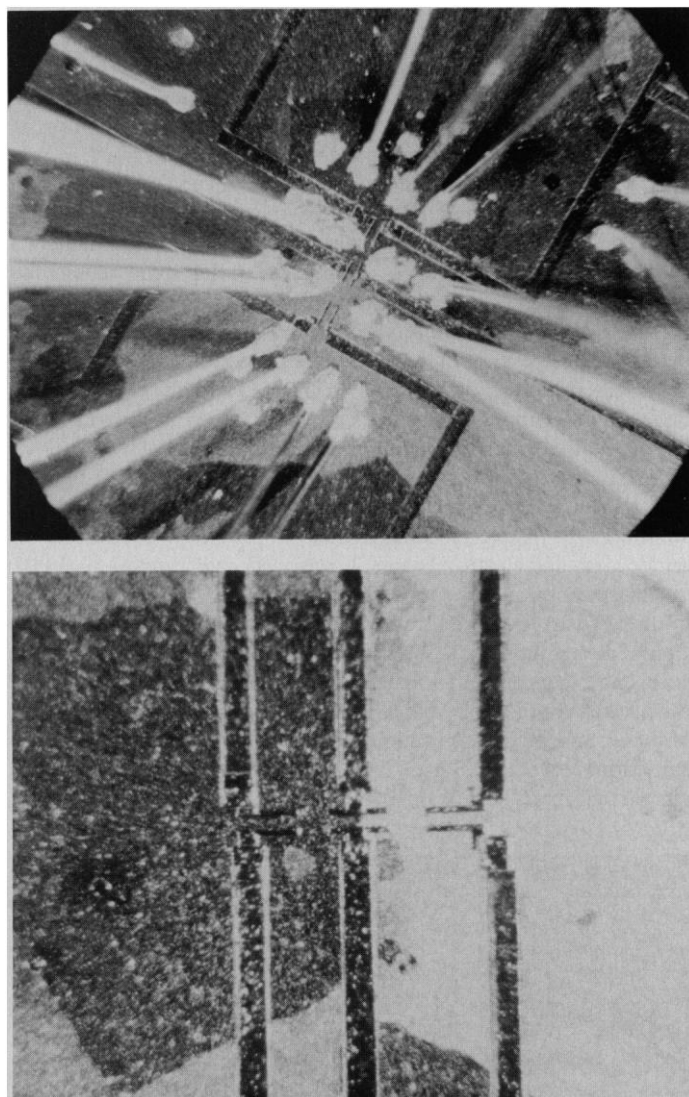


Fig. 3. High T_c superconductor material directly patterned by laser ablation. (**Top**) View of patterned film together with wire bonds. (**Bottom**) Magnified view showing lines selectively patterned within adjacent grains and across a grain boundary. Note that the different grains are clearly visible as light and dark areas through the use of an oblique-incidence illumination technique.

Chemical reactions can be driven on a surface by a focused laser either photolytically or pyrolytically. In either case, the surface is covered with a reactive medium, which can be a solid, liquid, or gas. Typically in a photolytic reaction, an ultraviolet laser is used. The laser energy directly breaks apart bonds of molecules in the reactive medium that can then go on to react, resulting in surface deposition or surface etching. In contrast, pyrolytic reactions are driven by the direct deposition of energy from the laser, which results in local heating of the substrate. Molecules from the reactive medium that come in contact with this micrometer-size "hot spot" decompose or react, thereby initiating some form of chemical reaction. Patterns are generated on a substrate by scanning either the focused laser beam across the substrate or, conversely, the substrate across the beam.

Because of the cost and complexity of laser-based systems and since the processes described here are slow (for large surface area modifications), the most successful applications of focused beam processing have been in special niche areas where spatial selectivity is required. Good examples are (i) photomask repair and (ii) circuit repair.

Photomasks can be thought of as the templates that are used to define the intricate patterns on an integrated circuit. Typically these masks are made of chrome patterns on quartz. Any defect on a mask is directly transferred to the IC and can result in a faulty or non-operable chip. Therefore much time and money is spent on locating, categorizing, and repairing these defects. This process becomes increasingly difficult as chip dimensions get smaller and smaller. Laser microfabrication techniques are well suited for repairing defects ranging from $25\text{ }\mu\text{m}$ in size to $1\text{ }\mu\text{m}$. Opaque defects, such as excess chrome, are readily repaired by laser vaporization with frequency-doubled Nd:YAG lasers. Clear defects, such as missing chrome, are repaired by the deposition of metal. Commercial laser photomask repair instruments are capable of repairing defects with a resolution of about $1\text{ }\mu\text{m}$ which is limited by thermal spreading and optical focusing. Finer features are repaired with focused ion beams.

Circuit repair is a well-established yield-enhancement technology for producing memory chips. Here, a laser is used to selectively disconnect faulty circuit elements from an array of redundant circuits thereby "wiring in" good elements. Laser microfabrication techniques bring an added degree of freedom to the circuit repair problem by providing the capability to directly add wiring. An example is the repair of a complex integrated circuit such as the IBM $\mu 370$ chip (Fig. 2 top). The chip is a 32-bit, 370 system microprocessor containing 200,000 transistors built in a $2\text{-}\mu\text{m}$ silicon gate n-MOS process. Figure 2A shows a magnified view of an area of the chip where a line was open due to a "routing" (chip design) error. The repair required two steps: (i) laser micro-cutting through the insulating layer to reach the metal lines (Fig. 2B) and (ii) the laser micro-deposition of a metal film to form an electrically conductive bridge (Fig. 2C) (3).

In addition to microelectronics applications, focused photon beam-processing techniques are being used in other fields. These include medicine, materials science, optoelectronics, and so on. A recent example is the use of focused excimer laser light to directly pattern high ($T_c \approx 92\text{ K}$) temperature superconductor materials. These materials are quite sensitive to many processing techniques, especially those that require contact with water. Therefore many of the processing techniques used to fabricate ICs are not readily applicable. However, an excimer beam can be used to directly pattern these films by etching. At IBM, excimer lasers have already been used to produce superconducting lines as narrow as $1\text{ }\mu\text{m}$, superconducting quantum interference devices (SQUIDS) that operate at liquid nitrogen temperatures, and Josephson junction devices. Figure 3 shows a region of a large-grained superconductor film patterned with an excimer laser, which provided the first direct

evidence that superconducting critical currents are indeed lower across grain boundaries (4).

Electron Beams

Key features that make electrons indispensable for microfabrication and characterization for microelectronics are (i) intense electron beams can be easily generated, for example, by using a hot filament, (ii) electron beams can be easily focused by electric and magnetic fields, and (iii) electrons efficiently interact with matter with a range of distances, or effective strengths, which can be controlled by an applied voltage. For example, with modest acceleration potentials of about 20,000 to 200,000 V and focusing magnetic fields, electron beams can be focused into spots a few angstroms in diameter. Thus objects can be imaged with essentially atomic resolution either by magnifying projection or by rapidly scanning such beams by means of time-varying electric or magnetic deflection fields at rates up to hundreds of megahertz. Electrons interact strongly with matter and, consequently, typical electron beam processes are performed in vacuum. The two main categories of processes are fabrication and characterization or analytical processes such as the various kinds of electron microscopy.

Electron beam microfabrication. Electron beam lithography is the main application of electron beams for microfabrication in semiconductor technology (5, 6). In electron beam lithography, the substrate is first coated with a thin film of radiation-sensitive material, commonly called a resist (in most cases an organic polymer). The electron beam irradiation changes the chemical solubility of the resist in the exposed areas. Subsequently, in a development step, the

more soluble part of the resist (either the exposed or the unexposed, depending on the polarity of the resist) gets removed and a pattern stays behind. This remaining resist then serves as a mask to transfer the pattern to the substrate, either by etching, deposition, or ion implantation, for example. Two features make electron beam lithography particularly attractive: the high degree of flexibility, accuracy, and speed with which original patterns can be directly generated with a computer-controlled beam and the high-resolution capability of electron optics.

The relative ease with which original patterns can be generated by a scanning focused beam under computer control makes electron beam lithography the main technology for fabrication of masks for other types of lithography such as standard optical projection lithography. This will continue to be true in the future for submicrometer optical lithography and for x-ray lithography as the resolution requirement becomes more demanding. Another application is direct-write lithography for manufacturing relatively low volume products, application-specific integrated circuits (ASICs), for which the demand is increasing due to the diversification of applications and sophisticated performance requirements. Even the highly specialized logic circuits of the biggest mainframe computers, such as those manufactured by IBM, fall into this category, because many different chips can be directly patterned without first preparing many different optical masks.

Electron beam lithography tools today are of the scanning type, in which a fine beam that can be rapidly turned on and off is steered to delineate a pattern serially. Such scanning tools have adequate speeds to prepare optical masks, which are used many times, but are relatively slow and can not compete with optical lithography tools in processing throughput. State-of-the-art tools can scan a beam at pixel rates of several hundred megahertz by using complex, variable-shaped spots that can expose about 100 pixels in parallel; thus processing rates of $>10^{10}$ per second can be achieved (a pixel is the smallest resolution spot in the pattern). The quick turn-around time of direct-writing tools together with the high resolution make such tools extremely suitable for development work even when future high volume manufacturing is done using optical lithography.

Areas with few practical alternatives to electron beam lithography are the development of submicrometer integrated circuits, research into limits of technologies, and the search for techniques and devices based on novel effects, which requires structures with 100-nm dimensions and below (7, 8). At this point in time, electron beam lithography is the only proven technology for sub-0.5 μm and even sub-100 nm work. As an example, Fig. 4 shows a scanning electron micrograph of gates from circuits of field effect transistors (FET). Circuits with gates as short as 70 nm have been fabricated with five levels of electron beam lithography, overlaid with an accuracy of better than 30 nm. Because of proper scaling of the devices to such small dimensions, they represent today's world record in transconductance, that is, current-drive capability, and switching speed for silicon transistors, with 13-ps switching time per stage in ring oscillators (9). These FETs are about ten times faster than the fastest CMOSFETs that are used today, and their dimensions correspond to densities that will allow for about 1 billion memory bits, or 1 gigabit, per chip in the future.

Fundamental resolution limits involve several factors: (i) the electron optical resolution, which can be a fraction of a nanometer, if current density in the beam and therefore exposure speed is not an issue, (ii) the range of secondary electrons with sufficient energy to expose the resist, (iii) the resolution, or effective size of the basic building blocks of the resist material. For poly-methylmethacrylate (PMMA), the most widely used resist for high-resolution applications, the latter two factors seem to limit resolution to ~ 10 nm, even if the electron-optical resolution is ten times better. In inorgan-

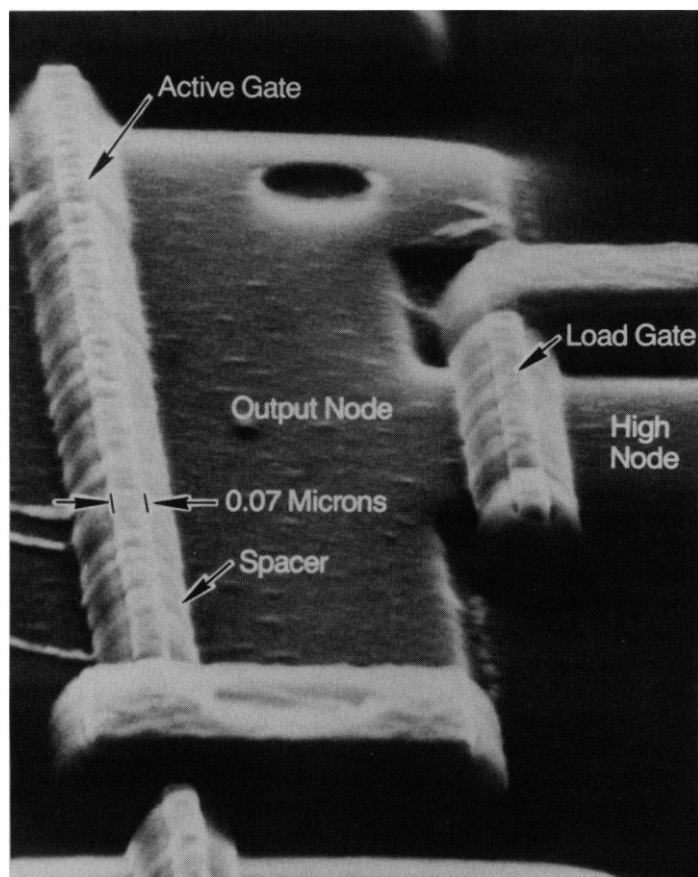


Fig. 4. High-resolution scanning electron micrograph of 70-nm gates in FET circuits.

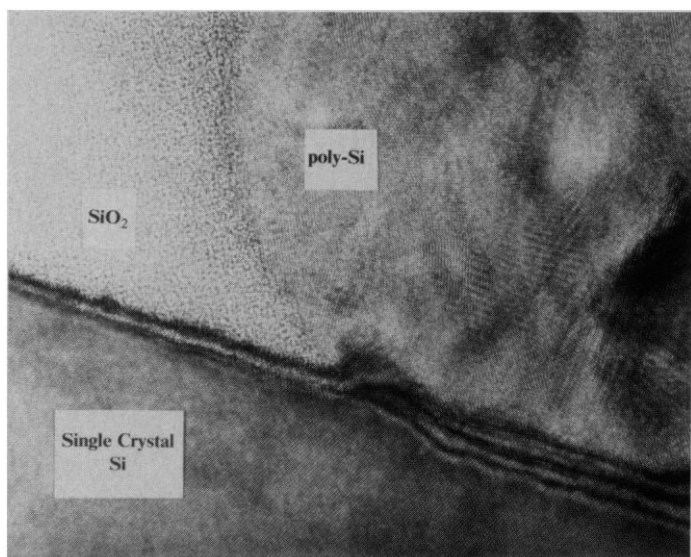


Fig. 5. Transmission electron micrograph of poly-silicon emitter contact in bipolar transistor.

ic resist materials such as AlF_3 , patterns with minimum dimension of 2 nm have been produced by electron beam lithography. These materials, however, require rather high exposure doses, so that breaking this apparent resolution limit of ~ 10 nm with highly sensitive material remains one of the challenges for electron beam lithography.

Another limitation that has a particular influence on the success of various types of lithography tools is the proximity effect. This is a modification of the effective exposure distribution in the resist caused by scattering of electrons in the resist and backscattering from the substrate. This effect cannot be eliminated, except for work on very thin substrates at high beam energies. With substantial computational effort, however, it can be predicted by simulation and then the dose that is given to individual pattern details can be adjusted so that ultimately the average dose for all pattern details becomes identical. This requires, however, that the electron beam tool is capable of adjusting the dose given to different pattern details, and the large amount of data-processing needed causes substantial problems with the high-density pattern ($\approx 10^{13}$ pixels) of future integrated circuits.

Normal operation of a scanning tunneling microscope (STM) has little or no effect on the sample. The STM can perform nanolithography by increasing the voltage and the tip-to-substrate distance so that a strongly confined electron beam with sufficient energy, formed by field emission, causes chemical reactions. Thin layers of electron beam resists have been exposed, including PMMA, Langmuir-Blodgett films, metal halides, and hydrocarbon contamination. Metallic deposits have been formed by decomposing metal-organic adsorbates and bumps have been created on the surface of metallic glasses by thermally and electrostatically enhancing surface diffusion. Atomic scale resolution has been shown in modifications to a single-crystal germanium surface. These concepts are very new and promising for ultrahigh resolution processing.

Electron beam characterization. Characterization techniques exploit the various effects that occur when an electron beam interacts with a sample: the electrons get absorbed in thin layers, depending on the local sample properties (in thin films of low atomic number material, essentially the phase of the electron waves gets shifted), they suffer material-characteristic energy losses, they excite secondary radiation in the form of photons (luminescence, x-rays) or secondary electrons, again with sample-specific energies and yields.

The scanning electron microscope (SEM) (10) in its various forms has come to play a key role in semiconductor technology, in particular because optical microscopy has poor resolution in the sub-micrometer regime. Sample preparation is simple—even production wafers or packaging modules can be inspected—because a focused electron beam is scanned across the surface, and secondary radiation is collected to form a point-by-point image. Major new developments are advances in the capability to focus significant currents into small spots, leading to high-resolution images with good signal-to-noise ratio. The advent of field emission sources and sophisticated electron optics has led to commercial instruments with better than 1-nm resolution and to high-resolution images with low energy electron beams (a few hundred electron volts), so that even insulating samples can be investigated without charging. Together with automation and improved metrology by means of laser interferometry, this opens the way for the use of SEMs for inspection and critical dimension measurements in the production line.

The transmission electron microscope (TEM) (11) has been the driving force for developments in electron optics earlier this century. In the conventional case, an unfocused electron beam is incident on a very thin sample and by using the transmitted electrons, magnifying projection electron optics form an image of the sample on photographic film with a resolution of a few angstroms. Thus, essentially atomic resolution has been achieved, in particular with the scanning version of the tool. Lattice imaging, where the contrast is improved as a result of the many atoms lined up in a properly oriented lattice-plane, has proven to be very powerful in materials research, in particular, interface studies. In Fig. 5, a cross section of a polysilicon emitter contact is shown by means of this technique. One can clearly distinguish the single crystalline silicon, the polycrystalline silicon, and the amorphous SiO_2 (12). The theory of image formation is well understood; the simulation of realistic images, however, which is necessary to understand phase-contrast images at the resolution limit, is computationally very intensive. The analytical capabilities of energy loss spectroscopy and filtering, and small area diffraction, for example, are becoming more and more important. A drawback is the rather complicated sample preparation: thinning to a few tens of nanometers is typically required and the sample size is limited. Recent advances in electron holography promise new possibilities for image evaluation and enhancement (13, 14).

An exciting new form of electron microscopy has become available with the invention of the STM (15). In an STM, a very fine metal tip is scanned across a sample at a height of only a few atomic spacings. At such spacings, a tunneling current occurs when only a few volts are applied between tip and sample. This tunneling current depends sensitively on the tip-to-sample spacing and is used to measure and control the height of the tip. In this way, scanning micrographs of this surface with a height resolution of one-tenth to one-hundredth of an atom and lateral resolution of approximately one to three atomic distances can be directly measured. Also, the electron energy distribution of the tunneling current depends on the electronic properties of the sample and can be used to select or view different types of surface atoms. Figure 6 shows a STM picture of the surface of GaAs, an important semiconductor used for solid-state lasers and high-speed electronic circuits. This picture shows the individual rows of Ga and As atoms with atomic resolution (16); this layer of Ga and As atoms gives rise to the surface properties of GaAs. This new technique is currently being refined and applied to many problems.

Noncontact electrical testing with focused electron beams is another application that will increase in importance as the complexity of circuits and packaging modules increases and critical dimensions further decrease. The current induced by the beam can directly

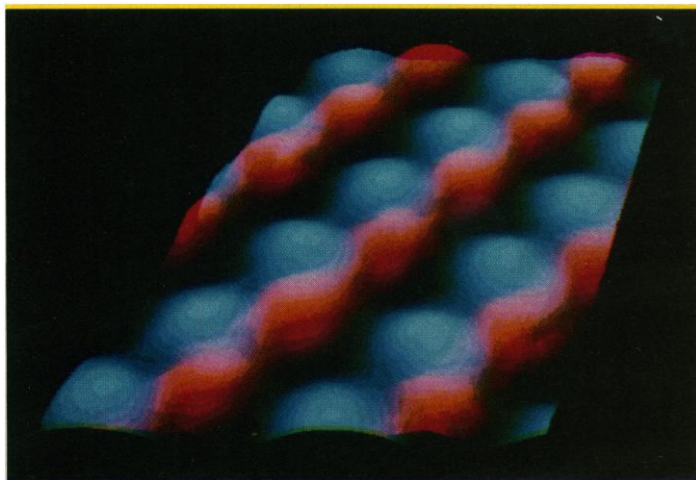


Fig. 6. Combined color scanning tunneling microscope (STM) images of the GaAs (110) surface, showing the Ga atoms (blue) and As atoms (red). The blue image was acquired by tunneling into empty states which are localized around surface Ga atoms, and the red image was acquired by tunneling into filled states which are localized around surface As atoms.

be detected on the substrate and in this way give information on electrical continuity (specimen current) and electronic properties (electron beam-induced current or EBIC). Another technique measures the energy of secondary electrons and thus the voltage at their point of origin on the specimen. Moreover, the electron beam can be chopped into pulses of picosecond duration, and thus fast changes in voltages on IC-lines can be sampled with high temporal resolution.

Ion Beams

When an ion enters a solid, it loses energy through collisions with the electrons and nuclei of the target. Eventually, the ion comes to rest within the target, resulting in the implantation of a new atom. The entire process takes place rapidly, often in less than a picosecond. Ion beams offer a powerful tool for depositing energy and implanting foreign atoms in matter. This capability has resulted in the widespread use of ion beams for the production and characterization of integrated circuits (17).

Conventional processing with broad ion beams. The energy deposited by the ion near the surface of the sample results in the ejection of atoms, secondary ions and electrons, and photons. Sputtering, that is, the ejection of atoms from the sample, is commonly used to erode thin films of materials. Sputtering is a nonselective process in which all materials can be eroded by an energetic (keV) ion beam. Reactive ion etching (RIE) can selectively remove materials with low-energy ions in the presence of chemically reactive species. For example, a plasma produced in a mixture of argon and chlorine gas will rapidly etch silicon, whereas almost no etching of silicon dioxide will occur. Materials analysis is another common application for ion beams. The composition of a target can be determined by analyzing the secondary ions, electrons, and photons. Impurities at concentrations of parts per billion can be detected by techniques such as secondary ion mass spectrometry.

In fabricating an integrated circuit, the electrical properties of the semiconductor are altered in highly localized regions to produce transistors, resistors, and so forth. This is accomplished by adding minute concentrations of dopant atoms such as boron and arsenic to silicon. Boron or arsenic ions are simply injected into the silicon through the process of ion implantation. The total number of

implanted ions can be measured by integrating the ion current over time and the depth of the ions can be controlled by selecting the ion energy. This provides such precise control of dopant concentrations that ion implantation has become the preferred method for incorporating dopants into silicon.

Conventional ion beam processing typically employs broad-area ion beams. In order to spatially localize the effect of the ion beam, a polymer resist containing the desired pattern is formed on the silicon wafer in a separate lithographic step. The polymer is sufficiently thick to block the ion beam whereas open regions in the polymer allow the ions to strike the wafer. Spatial resolution of $<0.2 \mu\text{m}$ laterally and $0.5 \mu\text{m}$ vertically into the silicon wafer are achievable.

Focused ion beams. Largely as a result of the development of high brightness ion sources, intense ion beams with current densities of 1 A/cm^2 can now be focused to a diameter of $0.1 \mu\text{m}$ or less (18). These finely focused ion beams can be scanned in a programmed pattern to selectively dope, sputter erode, or ion expose specific regions of a sample. This offers the potential of directly patterning a wafer without the usual lithographic steps. Unfortunately, the writing rate with focused ion beams is not yet economically competitive for routine conventional processes. However, the use of focused ion beams to repair defects in lithographic masks and for failure analysis and repair of integrated circuits has moved rapidly from research to development and manufacturing (19).

New chip designs frequently contain design and processing errors. Fabricating a new, corrected chip can take several months. The primary economic leverage that focused ion beams offer in chip work is to reduce the design and test phase of new integrated circuits by repairing these errors. An example that demonstrates chip repair is shown in Fig. 7 (20). The photo was produced by scanning the ion beam over the sample and detecting secondary electrons in a manner analogous to a scanning electron microscope. This scanning ion image shows a small section of a metal-encoded read-only memory in a microcomputer chip. Four bits in the memory corresponding to the four horizontal metal links are shown. This memory is usually programmed by thermally vaporizing the metal links with a pulsed laser. The link on the upper left was programmed

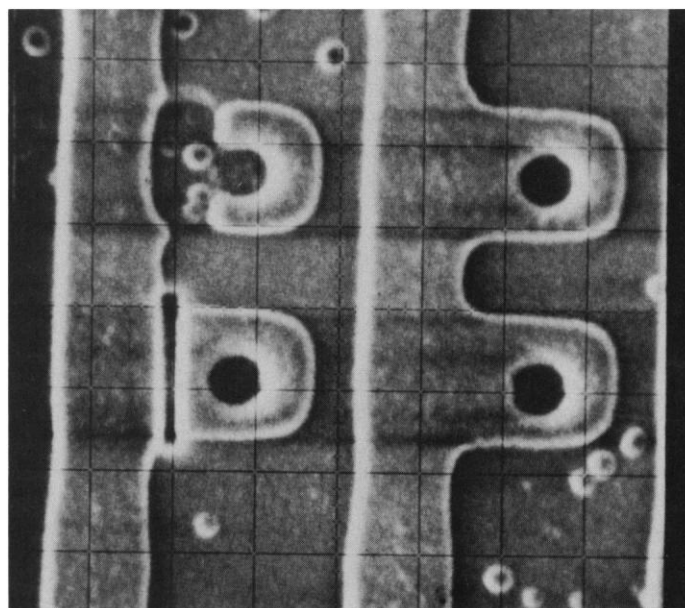
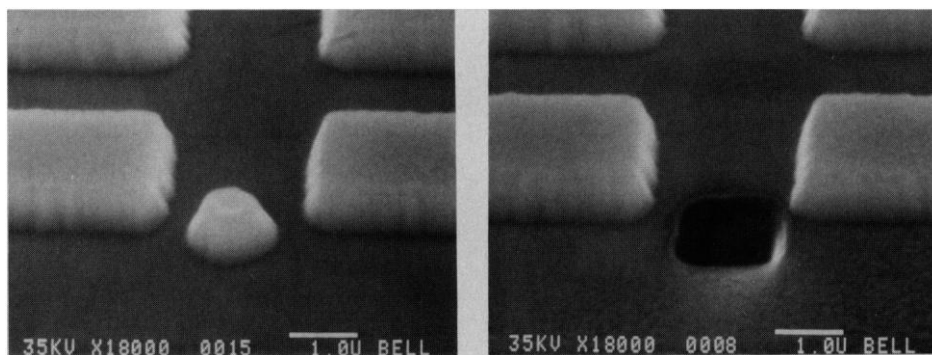


Fig. 7. An ion image showing four bits of the ROM memory in a microcomputer chip. The bit on the upper left was programmed with a laser; the bit on the lower left was programmed with a focused beam of gallium ions.

Fig. 8. A scanning electron micrograph showing a defect in an x-ray lithographic mask before (left) and after (right) ion beam repair. The conical metal defect was removed by bombardment with a focused Ga beam.



with the laser. The link on the lower left was cut by sputtering the aluminum conductor with a 20-keV focused beam of gallium ions. Approximately three aluminum atoms are removed per incident ion and this corresponds to the removal of $1 \mu\text{m}^3$ of aluminum every few seconds. In general, sputter yields range from 1 to 20 atoms per ion depending upon the material, ion species, and energy. The ion beam process offers much finer spatial resolution than the laser process for two fundamental reasons. First, the ion beam is not limited by diffraction effects so it can be focused to much smaller dimensions than the laser beam. Second, sputtering is a nonthermal process so energy deposited by the ion beam does not diffuse away from the focused spot.

Defects in lithographic masks can also be repaired with focused ion beams. Figure 8 is an example showing the repair of an opaque defect in an x-ray lithographic mask (21). The defect consists of the extra conical metal bump shown in Fig. 8, left. It was removed by physical sputtering as shown in Fig. 8, right. Focused ion beams have also been used to remove material in more sophisticated ways. For example, by varying the dwell time of the ion beam as it raster scans a region of a mask, a three-dimensional structure shaped like a prism, lens, or diffraction grating can be created. A prism structure eroded into a glass substrate can block the passage of light through total internal reflection. Such micromachining methods are currently being used to repair clear defects in optical masks used in the manufacture of integrated circuits.

Focused ion beams can also be used for depositing material (22). The most common method is to surround the sample with a hydrocarbon or organometallic gas, and then irradiate with the ion beam. The energy deposited by the ion beam decomposes the gas on the surface of the sample, leaving behind a deposited film. Typically 1 to 100 atoms can be deposited per incident ion. Figure 9 shows an example of ion-assisted deposition to repair three clear defects (holes) in an optical test mask. The patches are approximately $0.2 \mu\text{m}$ thick and consist of a diamondlike carbon film containing approximately 25% gallium. The patches are optically opaque and can be aligned with existing features on the mask to a precision exceeding $0.1 \mu\text{m}$ as shown in Fig. 9, bottom. In addition to carbon, metals such as aluminum, tungsten, and gold have been deposited with focused ion beams. This is a promising approach for the repair of metal wiring errors in integrated circuits and clear defects in x-ray masks. As circuit dimensions shrink, the limited resolution of laser processes will pose increasing difficulty. Focused ion beams offer a viable alternative.

Molecular Beams

Many of the advances in semiconductor processing have centered on the ability to decrease the lateral size of the device. Improved lithographic techniques and beam-related processing have dramati-

cally decreased the characteristic feature size obtainable on a semiconductor surface to the submicrometer range. Further improvements in the device and circuit performance will also require the ability to define and modify the semiconductor properties as a function of depth within 0.01 to $2 \mu\text{m}$ of the wafer surface. This "in-depth" modification of the material, or vertical profile, typically defines the electrically active region of the device. Most of existing semiconductor technology relies on the formation of this active region through the near-surface modification of a highly perfect semiconductor single-crystal wafer. The processing techniques of ion-implantation and diffusion of dopant impurities have been used to form, both laterally defined and in depth, regions of controlled electrical characteristics.

Epitaxial growth techniques. An alternative approach fabricates these regions through the process of crystal growth. If a bulk-grown semiconductor wafer is used as a seed or crystal template, thin layers of deposited material can continue the substrate crystal structure through the process of epitaxial growth. The epitaxial growth process begins with the deposition of the growth nutrients on substrate surface. These deposited atoms migrate over the substrate surface and finally bond to an appropriate crystallographic site. The deposited atom will continue the atomic arrangement of the substrate, typically growing in a layer-by-layer fashion. Abrupt changes in the composition of the deposited atoms can create very sharp interfaces between layers of deposited materials. The co-deposition of dopant impurities can alter the electrical properties of the growing crystal.

As device structures become smaller in both lateral and vertical dimensions, the use of thinner, more controlled layers becomes required. Recently new low-temperature processing techniques have been developed to meet these requirements. Low processing temperatures minimize the thermal redistribution of dopants and interdiffusion at interfaces. The epitaxial growth techniques of molecular beam epitaxy (MBE) and vapor phase epitaxy (VPE) have provided a new measure of control in the epitaxial formation of device structures. Namely, the composition of the film can be controllably altered in depth on an atomic level, as opposed to a control on the order of hundreds of atomic layers with ion implantation. These techniques, and the unique structures that result from their application, have allowed the device physicist and process engineer to "bandgap engineer" the electronic structure of a device, tailoring the composition and electrical profile to utilize particular physical effects.

Both VPE and the vacuum deposition of electronic materials have been in use for over 40 years, yet new forms of these epitaxial techniques have been developed within the last decade. Although both silicon and the compound semiconductors, such as GaAs, (Al,Ga)As, and InP, have benefited from these techniques, the field of GaAs related devices and materials has been the focus of the most active research and development. The MBE technique requires an

ultrahigh vacuum chamber (23). In the case of GaAs/(Al,Ga)As growth, beams of Ga, Al and As, which form an elemental thermal evaporation source, impinge on the surface of a heated substrate as schematically shown in Fig. 10. The composition of the growing layer is determined by the relative fluxes of these molecular beams at the hot substrate surface, whereas the layer thickness is controlled by shuttering the source cells. Similarly, shuttered cells of dopant elements such as Si and Be can place the electrically active impurities to a high precision within the growing layer. The MBE growth of Si has also been developed, albeit at a slower pace (24). Slow growth rates ($\approx 1 \mu\text{m}/\text{hour}$) and the beam nature of the MBE process limit the throughput of this growth system. Growth from the vapor phase permits the deposition of material simultaneously over many wafers. The technique of metal-organic vapor phase epitaxy (MOVPE) has been used to deposit thin-layered structures of the compound semiconductors (25). The MOVPE system consists of a panel of gas sources and a reactor. The gas panel determines the gas composition in the reactor through the careful metering of the source materials in a carrier gas. High-speed valves serve the function of the MBE shutters by rapidly switching the growth gases into and out of the

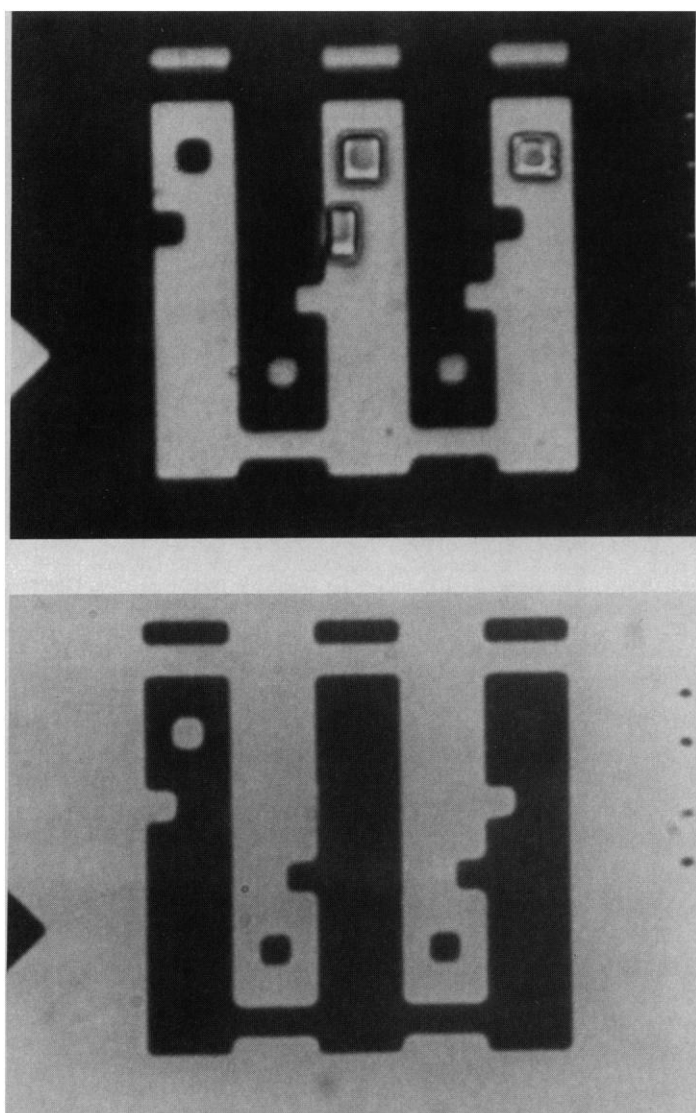


Fig. 9. (Top) An optical micrograph taken in reflected light showing three carbon patches deposited on an optical test mask with a focused ion beam. (Bottom) A transmitted light micrograph showing that the patches are optically opaque and suitable for the repair of clear defects in photomasks.

reactor. The reactor has a heated stage where the substrate resides and the deposition occurs. The process gases flow over the hot surface and chemical reactions near or at the growth surface result in the deposition of the epitaxial material.

Other less developed epitaxial growth techniques have appeared in the research literature. The replacement of the elemental sources in the molecular beam epitaxy system with gas beam sources is a promising combination of the MBE and MOVPE techniques. The use of chemical beam sources increases the versatility of the MBE system. Silicon epitaxial technology has also seen recent advances. Through the application of high-vacuum technology to Si VPE, epitaxial growth of Si can be achieved at substantially lower growth temperatures than previously employed (26). A variety of photon- and plasma-assisted epitaxial growth processes have also appeared at the research stage. These techniques supply additional energy for the decomposition of source gases and atomic motion on the surface during growth.

Although the capabilities of these new epitaxial deposition techniques have been impressive, these processes have not yet been used to any significant extent in the manufacturing of commercial digital circuits. Several reasons are: (i) methods such as ion implantation that have less depth control have been adequate and well developed and (ii) these new epitaxial growth techniques lack a high degree of uniformity and reproducibility in the deposition process. Vapor deposition systems are often difficult to characterize and model. Many of the chemical reactions important in the process are either unknown or poorly understood. These problems have motivated the search for new epitaxial processes that provide improved uniformity. Among the newest approaches, the process of atomic layer epitaxy (ALE) is one of the most promising (27). The ALE process consists of the deposition of a single monolayer of epitaxial material per growth cycle. This technique exhibits a self-limiting growth mechanism that insures the complete formation of one and only one monolayer of growth over the entire wafer per growth cycle. As digital microelectronics progresses into the submicrometer region with increased performance, these epitaxial methods will become preferred for many applications.

Ultrathin-layer structures. The ability to grow thin layers of epitaxial materials has led to new phenomena that have a substantial commercial impact, namely the fabrication of solid-state lasers. By combining or stacking thin layers of different chemical composition, the local electronic structure is correspondingly modified. Both barriers to current flow and local carrier confinement regions, or wells, can

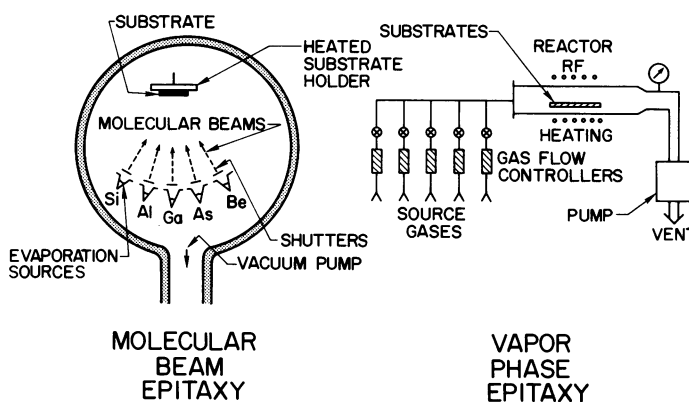


Fig. 10. Both molecular beam epitaxy (MBE) and vapor phase epitaxy (VPE) have been used to create thin-layer structures. MBE utilizes an ultrahigh vacuum system where atoms are supplied to the growing film in the form of molecular beams. The VPE growth system is a flowing gas reactor. Elements that are chemically entrained in the gas stream react to yield a solid deposit.

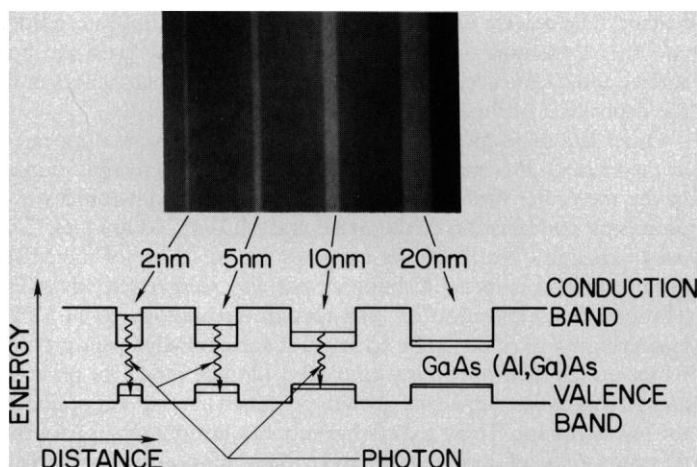


Fig. 11. Ultrathin layers of semiconductor material forming a single-crystal structure are routinely fabricated by MBE and VPE. Thin layers of the small-bandgap GaAs grown by MOVPE are cladded by layers, ≈ 40 nm thick, of the higher bandgap $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$, to form quantum wells. The electronic structure of the quantum well is modified from the structure found in thick layers. These layers form a potential well somewhat described by the classic quantum mechanics problem of a particle in a one-dimension potential well.

be formed by the appropriate growth of high or low bandgap materials. Currently the most important use of this thin-layer technology is the growth and study of quantum wells. These structures consist of a thin, typically 2- to 30-nm layer of a low bandgap material (for example, GaAs) sandwiched between higher bandgap material, $(\text{Al,Ga})\text{As}$, as seen in Fig. 11. Electrons and holes confined to the well exhibit new, sharp quantized energy states that can be used to create a laser. Quantum well structures have found a ready commercial application in the manufacturing of highly efficient solid-state lasers where the wavelength of emission can be tuned through the choice of the well width.

Other emerging applications of these technologies encompass almost all major digital device structures including bipolar and field effect transistors. The vapor-phase deposition of insulators, such as SiO_2 , metals, and metal silicides, continues to dominate key aspects of semiconductor chip and package fabrication.

Summary

Beam-controlled processing will affect all areas of semiconductor and microelectronic fabrication and packaging. The dramatic expan-

sion in the microelectronics industry has been the result, in part, of the development of higher levels of integration and circuit density. Smaller devices are required to maintain this progress. New lithography techniques utilizing photon, electron, or ion beams have led to the shrinking of the lateral feature size of a transistor to the submicrometer regime. Vertical device dimensions can be reduced even further to well below $0.1 \mu\text{m}$ through the use of epitaxial techniques. The advantages in fabrication afforded by these beam technologies will certainly justify the increased complexity and difficulties in their development. Meeting the challenges of these technologies will also open the door to new important physical phenomena useful in the next generation of information-processing machines.

REFERENCES AND NOTES

1. J. S. Wilczynski, *J. Vac. Sci. Technol.* **B5**, 288 (1987).
2. G. Blonder, G. S. Higzshi, C. G. Fleming, *Appl. Phys. Lett.* **50**, 766 (1987).
3. J. Chang, J. J. Donelon, P. Grier, J. E. Hurst, M. M. Oprysko, W. Shih, R. J. vonGutfield, unpublished results.
4. P. Chaudhari *et al.*, *Phys. Rev. Lett.* **60**, 1653 (1988).
5. A. N. Broers and T. H. P. Chang, in *Microcircuit Engineering*, H. Ahmed and W. C. Nixon, Eds. (Cambridge Univ. Press, London, 1980), pp. 1-73.
6. G. R. Brewer and J. P. Ballantyne, *Electron Beam Technology in Microelectronic Fabrication* (Academic Press, New York, 1980).
7. T. H. P. Chang *et al.*, *IBM J. Res. Dev.*, in press.
8. R. E. Howard and D. E. Prober, in *VLSI Electronics: Microstructure Science*, N. G. Einspruch (Academic Press, New York, 1982).
9. G. A. Sai-Halasz *et al.*, *IEEE International Electron Device Meeting, Technical Digest* (Institute of Electrical and Electronic Engineers, Piscataway, NJ, 1987), pp. 397-400.
10. O. C. Wells, A. Boyd, E. Lifschin, A. Rezanowich, *Scanning Electron Microscopy* (McGraw-Hill, New York, 1974).
11. L. Reimer, *Transmission Electron Microscopy* (Springer-Verlag, Berlin, 1984).
12. S. J. Jeng, T. S. Kuan, T. C. Chen, M. Jost, unpublished results.
13. H. Lichte, *Ultramicroscopy* **20**, 293 (1986).
14. A. Tonomur, *J. Appl. Phys.* **61**, 4297 (1987).
15. G. Binnig and H. Rohrer, *IBM J. Res. Dev.* **30**, 355 (1986).
16. R. M. Feenstra, J. A. Stroscio, J. Tersoff, A. P. Fein, *Phys. Rev. Lett.* **58**, 1192 (1987).
17. R. G. Wilson and G. R. Brewer, *Ion Beams with Applications to Ion Implantation* (Wiley, New York, 1973).
18. R. L. Seliger, J. W. Ward, V. Wang, R. L. Kubena, *Appl. Phys. Lett.* **34**, 310 (1979).
19. A. Wagner, *Nucl. Instr. Meth.* **218**, 355 (1983).
20. L. R. Harriott and A. Wagner, *J. Vac. Sci. Technol.* **4**, 181 (1986).
21. D. K. Atwood, G. J. Fisanick, W. A. Johnson, A. Wagner, *Soc. Photo. Opt. Instrum. Eng.* **471**, 127 (1984).
22. K. Gamou, N. Takakura, N. Samoto, R. Shimizu, S. Namba, *Jpn. J. Appl. Phys.* **23**, L293 (1984).
23. A. Y. Cho and J. R. Arthur, *Prog. Solid-State Chem.* **10**, 157 (1978).
24. S. Iyer, in *Silicon Epitaxy*, B. J. Balaga, Ed. (Academic Press, New York, 1986), pp. 91-175.
25. T. F. Kuech, *Mater. Sci. Rep.* **2**, 1 (1987).
26. B. S. Meyerson, *Appl. Phys. Lett.* **48**, 797 (1986).
27. C. H. L. Goodman and M. V. Pessa, *J. Appl. Phys.* **60**, R65 (1986).