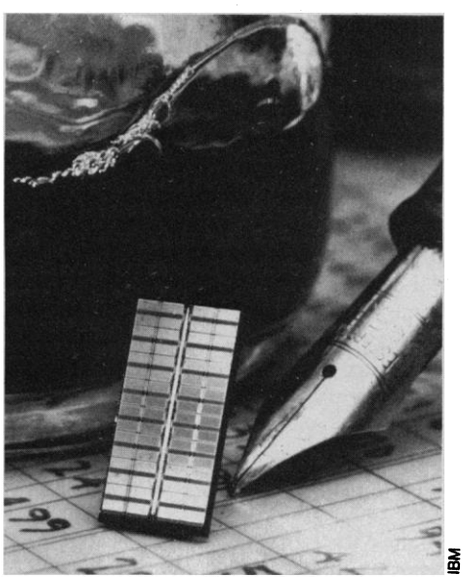
A 16-Megabit Memory Chip from Japan

Researchers from Nippon Telegraph and Telephone are the first to unveil an experimental 16-Mb dynamic random-access memory chip, although it is still some years away from commercial production

Just as dynamic random-access memory (DRAM) chips storing 1 million binary bits of information begin to enter the market in large numbers, researchers from Nippon Telegraph and Telephone's (NTT) Atsugi Electrical Communications Laboratories near Tokyo have leaped ahead two generations with the introduction of a DRAM with 16 times that storage capacity.

The announcement was made at the International Solid-State Circuits Conference in late February in New York, where five other Japanese companies and IBM also discussed 4-megabit (4-Mb) chips. Three other firms introduced experimental 4-Mb DRAMs at last year's conference. None of these advanced DRAMs are yet ready for production, but they indicate the types of microcircuit technologies future commercial versions will feature.

The Japanese domination of the session devoted to advanced DRAMs suggests their continued control of this segment of the integrated circuit industry. Japanese firms last year reportedly made 65% of the DRAMs sold in the United States, where the chip was invented, and held 80% of the world market. Because DRAMs are a high-volume product where new technology often appears first, leadership in their manufacture is often taken as a marker of overall position in a highly competitive business.



IBM

4-Mb DRAM. *The chip measures 6.35 millimeters by 12.3 millimeters. The 4,194,304 memory cells are in the rectangular arrays, while control circuitry runs between the arrays.*

Concern in the United States over loss of leadership is at a peak right now. Last week, the Semiconductor Industry Association, which represents American integrated circuit makers, announced an agreement to establish a joint research and development consortium to be called Sematech for Semiconductor Manufacturing Technology Institute. Although funding arrangements for the venture are yet to be worked out, most proposals call for substantial federal contributions to an annual budget that could be in the neighborhood of $300 million. Earlier this year, the Pentagon's Defense Science Board released a report calling for more than $1 billion of federal spending over 5 years on microelectronics, much of it focused on DRAMs.

A November report from Brookhaven National Laboratory outlined a specific plan for the development of the advanced technology needed for future generations of DRAMs. The result of a series of workshops with participation by Brookhaven, industry, and academic researchers, the plan highlights one role that U.S. national laboratories can play in aiding industry. In particular, it focuses on the use of synchrotron radiation for the x-ray lithography that could imprint circuit patterns with minimum feature sizes of 0.25 micrometer. Cost would be $395 million to be spent over 6 years.

All of the experimental DRAMs at the solid-state circuits conference had minimum features of 0.8 micrometer or less. The NTT 16-Mb and IBM 4-Mb chips were among the smallest at 0.7 micrometer. The NTT researchers used a scanning electron beam (direct writing) to achieve these dimensions, where the IBM group relied on a more conventional advanced optical lithography process. Direct writing is generally considered to be too expensive for high-volume commercial chips because it is a serial process and hence slow. It is one thing to make a few experimental chips and quite another to have a commercially feasible manufacturing process. IBM has made a big point of emphasizing that its DRAM was made on the same production line the company uses for volume production of the 1-Mb memories now in some of its computers.

Making small features is not the only trick to be mastered as the race to store ever more information on a DRAM chip continues apace. Tsuneo Mano, representing a group of ten NTT researchers at the solid-state circuits conference, and Richard Parent, speaking for 13 co-workers at IBM's General Technology Division in Essex Junction, Vermont, outlined sometimes convergent and othertimes divergent solutions to some of the technological issues.

Both groups took a now fairly common tack in confronting the problem of how to store a usefully large electric charge in an ever smaller area of space on a chip. The absence or presence of stored charge in a miniature capacitor represents the binary 0 and 1, but too small a charge cannot be reliably sensed. The solution is to construct a vertical or trench capacitor that does not take up much surface area. In this way, the NTT researchers were able to construct a memory cell, comprising the capacitor and an access transistor that allows the cell to be written into and read from, that occupies only 4.9 square micrometers.

IBM, which uses conventional horizontal or planar capacitors in its commercial 1-Mb DRAMs, also shifted to the newer trench capacitor technology in its 4-Mb chip. The resulting 10.5–square micrometer cell thereby increased the packing density of memory cells by a factor of 3 over the previous-generation chip. The NEC Corporation in Japan reportedly is already incorporating trench capacitors in its 1-Mb products, presumably thereby getting an early start and a leg up in this new technology.

Having a sufficiently large storage capacitor is not enough to guarantee a measurable signal in very large memories. The NTT group also had to design a new array structure that allowed signals to reach the sensing circuits without being degraded.

A second important problem is the yield or the percentage of defect-free chips. In a high-volume, low-cost product such as a DRAM, low yields are especially disastrous. As the structure of a memory cell becomes more complex in larger DRAMs and the

fabrication processes become concomitantly more complicated, yields are decreased by defects in the cells.

The now traditional means of dealing with low yields in DRAMs is to incorporate extra rows or columns of so-called redundant memory cells. If a defective cell is found in one of the normal rows or columns, it can be disconnected and replaced by a redundant cell. IBM has stayed with this approach in its 4-Mb DRAM. The chip includes 96,000 redundant memory cells. It is interesting that the state-of-the-art DRAM at the start of the 1980s had a total of 64,000 cells.

As memory size grows, redundancy becomes less practical, according to the NTT way of thinking. The alternative is the use of error-checking and error-correcting circuitry. Such circuitry can also test for and fix errors due to electric charge generated in memory cells when ionizing alpha particles pass through the chip, a significant problem when the storage capacitors are small. The downside of error-correcting circuitry is that it slows down the operation of the memory.

Three years ago, NTT researchers introduced a then experimental 1-Mb DRAM with such circuitry but there was a substantial 20-nanosecond "access penalty," enough to prevent its use in commercial memory chips. This year the NTT group redesigned the error-correcting circuitry and reduced the access penalty to 5 nanoseconds. The space occupied by the circuitry is about 10% of the total chip area.

To address a third problem, both NTT and IBM departed from the industry-standard 5-volt power supply for their DRAMs, lowering the operating voltage to 3.3 volts. The lower voltage is necessary to reduce the electric fields in the tiny structures making up the transistors and other devices on the chip, thereby preventing the degradation of device performance by high-field effects.

A crucial specification of any memory device is the access time or time to retrieve a bit of information from a memory cell. IBM's 4-Mb chip is quite fast for a DRAM with an access time of 65 nanoseconds, which compares favorably with the 80-nanosecond access time in the company's most advanced 1-Mb memory. Although perhaps not so meaningful from a computer point of view, some idea of the speed comes from the realization that this corresponds to retrieving in less than a quarter of a second the 400 pages of double-spaced typewritten text that the chip can store. The NTT 16-Mb chip operates with a quite respectable 80-nanosecond access time. The fastest DRAM at the conference was a 1-Mb chip with a 35-nanosecond access time from the Hitachi Central Research Laboratory in Tokyo. ■ **ARTHUR L. ROBINSON**

The Surprising Genetics of Bottlenecked Flies

The great majority of theoretical models have led researchers to expect a genetic impoverishment when a population is founded from a small number of individuals; new experimental results appear to confound these expectations

"You have to be crazy to do this sort of thing," says Edwin Bryant of the University of Houston. "It is incredibly laborious." Bryant is referring to a series of quantitative genetics experiments that he and his colleagues Steven McCommas and Lisa Combs have just reported, in which they measured the effects of passing houseflies through what geneticists call population bottlenecks. "I didn't think anyone would ever do this experimentally, because it is so tedious," observes Charles Goodnight, a theoretician at the University of Illinois, "but I'm delighted with the results."

"I think what happened with theoretical analyses of bottlenecks is what often happens with mathematical representations of biology."

The genetic effect that Bryant and his colleagues saw in populations of flies that had bred from 1, 4, and 16 male-female pairs in three separate experiments was an increase in variance, not a decrease as most mathematical models of bottlenecks would imply. In other words, there was more variability in some of the flies' physical characteristics—such as wing size and shape—in the post-bottleneck population than in the ancestral population, whereas the general expectation is that there would have been less. "Yes, at first sight it seems counterintuitive," comments Brian Charlesworth, a theoretician at the University of Chicago. "The results are clearly important, but I'm not yet fully sure what the implications are."

Goodnight is delighted with the Houston researchers' data because shortly after they were published he reported a theoretical model that essentially points in the same direction. "We've come to similar conclusions, but from completely different directions," says Goodnight, "and that's got to be encouraging."

Charlesworth's uncertainty about the implications of these new results is not because bottlenecks occupy an obscure backwater of quantitative genetics research. They don't. Since the 1950s bottlenecks have been part of an intense debate among geneticists, a debate that touches both on the mechanisms of the origin of new species and on conservation biology. An understanding of bottlenecks is therefore undoubtedly important. Charlesworth's uncertainty derives from the immense complexity of genetic processes that apparently operate through bottlenecks, a complexity that he and other theoreticians have attempted to address with several elegant but competing mathematical models.

"This uncertainty is not going to be resolved quickly," says Alan Templeton, a geneticist at Washington University who has played a key role in recent exchanges in the long debate. "But Bryant's results are important because we are finally getting the kind of information we need in order to evaluate these alternative models."

The potential genetic consequence of a bottleneck can be envisaged by thinking about one highly variable gene locus in some kind of hypothetical population. "Suppose you have 200 alleles at that locus within the population," explains Bryant, "and then you take two individuals, a male and a female, and begin a new population from them. The maximum number of alleles at that locus that can get through the bottleneck is four, which at first sight is a tremendous loss of variability."

The loss is tremendous, of course, but most of the 200 different alleles will be extremely rare in the original population and will therefore contribute only minimally to variance of the trait—such as wing dimensions in Bryant's experiments—influenced by this gene locus. "So, although a drop from 200 alleles to four is a sharp decrease in absolute genetic variability at the locus, it is a much smaller reduction in