Transistors Head for the Trenches

Space on the surface of a random access memory chip is limited; vertical transistors on trench walls permit denser packing

THE elements of integrated circuits are laid out horizontally on the surface of a semiconductor chip. While miniaturization proceeds apace, some limits are in sight, and electrical engineers are increasingly looking at exploiting the third dimension, depth, in order to squeeze more transistors into a given surface area.

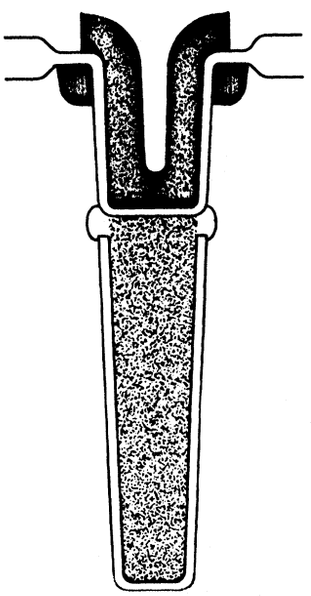
While the idea of vertical integration is not new, at the International Electron Devices Meeting in early December, Hideo Sunami of Hitachi Ltd.'s Central Research Laboratory in Tokyo explained why it may be necessary in dynamic random-access memory (DRAM) circuits by the early 1990's.* New technology often appears first in DRAM's, which are the mainstay of the microelectronics business.

At the same meeting, a group from the Nippon Telegraph and Telephone Electrical Communication Laboratories in Atsugi showed how to combine the notion of vertical transistors with the recently fashionable idea of trenches, while another group from Texas Instruments in Dallas reported on a complete vertical memory cell.

In his presentation leading off a session on advanced DRAM technologies, Sunami reviewed the effects on memory cell structure as the storage capacity of a chip evolved from the 4096 (4K) bits of the early 1970's to the present level of 1-megabit. Each generation has four times the storage capacity of its predecessor. The 4K DRAM was the first generation in which each memory cell comprised only a capacitor and a single transistor. Stored charge on the capacitor represents the information content of the cell. The transistor acts as a switch (pass gate) that connects the capacitor to other circuits for the reading and writing operations.

Sunami noted for successive generations of DRAM's an exponential decline in cell area, which is in the neighborhood of 30 square micrometers for the 1-megabit chips that will soon be commercially available. The decreasing area becomes a problem because the capacitor must be able to store a large enough charge (at least 300 femtocoulombs) to represent reliably the information content of the memory cell, and the charge storage capacity is proportional to the area.

Engineers struggling with this problem have devised so-called trench capacitors. A coating of electrically insulating material on the surface of a trench a few micrometers deep in a silicon substrate serves as the dielectric, while the electrically conducting trench walls and trench filler material serve as the plates of the capacitor. The trench is actually shaped like a rectangular well with vertical walls. In this way, the capacitor area can be larger than that occupied on the chip surface by the memory cell.



Trench memory cell

White stripe delineating the trench is silicon dioxide insulator. Silicon outside and polycrystalline inside the lower trench are the capacitor plates. Dark and light bulbs outside the top and bottom of the upper trench are the transistor source and drain electrodes. Silicon outside the upper trench is the channel, while polycrystalline silicon inside is the gate electrode.

Assuming that future DRAM generations will continue to appear every 3 years, Sunami projected that the 4-megabit chip would arrive in 1989 with a cell size of 13 square micrometers, the 16-megabit chip in 1992 with a 5-square-micrometer cell, and the 64-megabit chip in 1995 at only 2-square micrometers per cell. To achieve these small dimensions, the pass-gate transistor would have to be placed over the capacitor rather than beside it, as at present. Eventually, the transistor itself would have to be oriented vertically, concluded the Japanese engineer.

In a session on novel device technology, Shigeru Nakajima, Kenji Miura, Toshifume Somatani, and Eisuke Arai of NTT's Atsugi laboratory presented what they called a T-MOS transistor. The T stands for trench. The MOS technology dominates in densely packed memory chips and takes its name from the transistor structure in which a metal gate electrode is electrically insulated from the active semiconductor by a thin layer of oxide. A voltage on the gate electrode turns the transistor current on or off. When the transistor is on, current flows between source and drain electrodes in a thin channel beneath the insulating oxide.

Recall that, by adding the appropriate impurity atoms (dopants), silicon can be either *n*-type in which electrical current is carried by electrons or *p*-type in which the current is borne by electron vacancies or holes. An *n*-channel MOS transistor consists of *n*-type source and drain regions separated by a *p*-type channel. In operation, application of a positive voltage to the gate generates electrons in the channel, making it also *n*-type, so that there is a continuous path for electrons between the source and drain, which turns on the transistor.

To make a vertical *n*-channel MOS transistor, the NTT engineers carved out a square trench 1.4 micrometers wide and either 0.8 micrometer or 1.3 micrometers deep in the surface of a *p*-type silicon substrate. Subsequent processing steps filled in the trench as follows. A 150-angstrom-thick layer of silicon dioxide covered the trench walls, which played the role of the channel. Next, a layer of electrically conducting polycrystalline silicon served as the gate electrode. Regions of heavily *n*-type silicon underneath the trench and beside it at the top comprised the drain and source. Finally, after another layer of insulating oxide, the

*Institute of Electrical and Electronics Engineers, International Electron Devices Meeting, Washington, DC, 1–4 December 1985.

The Return of the Vacuum Tube

Anybody who has ever replaced a vacuum tube in an old television or radio knows why tubes are not seen much anymore: they are big; they get hot; and they cost a lot of money. However, suppose that tubes could be made as small and as inexpensively as transistors in semiconductor integrated circuits. Would the vacuum tube be set for a return?

Quite possibly yes, argued Richard Greene of the Naval Research Laboratory at the International Electron Devices Meeting in December. In his presentation, coauthored with Henry Gray and George Campisi, also of NRL, Greene did not forecast the end of solid-state electronics. But for certain applications requiring high speed, immunity to radiation in space-based or nuclear environments, or operation at an elevated temperature, he said that vacuum-tube integrated circuits could have distinct advantages. Ironically, it is the microfabrication technology developed for semiconductors that makes resurrection of vacuum tubes conceivable.

Consider the vacuum-tube equivalent of a transistor, the triode. Electrons are emitted from the cathode and fly toward the anode or plate, which is positive relative to the cathode. In between lies the grid, which is negative relative to the cathode. The grid voltage determines whether electrons make it to the anode. If they do, the triode is on; if not, it is off.

The speed of a triode switch is ultimately limited by the electron transit time between the cathode and anode, which depends on the distance between them and on the electron velocity. Electrons in a vacuum are not slowed by collisions as in a semiconductor. If the anode is 100 volts more positive than the cathode, a typical value for vacuum tubes, the electron velocity reaches 6×10^8 centimeters per second, 60 times the maximum in silicon. The transit time in a miniaturized device 1 micrometer long would be less than a picosecond, hence the possibility of ultrahigh-speed triode switches. As for immunity to radiation damage and operation at high temperature, vacuum tubes have natural advantages over semiconductors. Vacuum tubes operate best at high temperature and there is no electrically active structure to damage.

The fastest semiconductor transistor switches in only 5.8 picoseconds and there are ways to enhance resistance to radiation and to keep devices cool. Nonetheless,as Greene reviewed, there are substantial efforts under way to make vacuum-tube integrated circuits and take advantage of their special properties. Greene mentioned space missions, real-time control of nuclear reactors and jet engines, monitoring geothermal wells, and "various military applications" as the kinds of places one would consider the new vacuum-tube technology.

Researchers led by Byron McCormick at the Los Alamos National Laboratory have made small-scale integrated circuits, such as a flip-flop, comprising several triodes. Materials for the cathode, grid, and anode are deposited on a sapphire substrate and patterned as in semiconductor integrated-circuit manufacture. The distinguishing feature of the Los Alamos devices is the cathode, which works by thermionically emitting electrons; that is, a combination of applied voltage and high temperature (800 C) kicks the electrons out of the material. Unfortunately, the cathode must be relatively large, inhibiting miniaturization and limiting switching times to about 1 nanosecond, when the technology is perfected.

A more ambitious approach that is farther from fruition lies with the use of field-emitter cathodes in which an intense electric field draws electrons from the tip of a sharp metal point about 0.05 micrometer in diameter. Field emitters require quite high anode voltages, up to 500 volts, but they are also compatible with overall device dimensions of about 1 micrometer, opening the way to ultrahigh-speed operation. A group headed by Charles Spindt at SRI International and the NRL researchers independently are looking into this option. The SRI group has made arrays of up to 10,000 field emitters on substrates 1 millimeter in diameter.

Overall, Greene compared the performance of vacuum-tube integrated circuits against a list of eight desirable attributes for microelectronics devices, including speed, size, power consumption, device and circuit cost, electrical properties, suitability for digital electronics, reliability, and environmental ruggedness. He concluded that much more work is necessary before it would be possible to predict when vacuum tubes will return in their miniaturized form. ■ **A.L.R.**

center of the trench was filled with additional polycrystalline silicon as a guide electrode to connect the drain to the surface.

All in all, the vertical transistor occupied about half the space of a conventional horizontal device. A particular advantage of the NTT design is that all three electrodes can be connected individually and from the top of the chip by metal or other conducting material to other devices, in contrast to an earlier version of vertically integrated transistors in which the substrate served as a common drain for all the transistors.

The next step is to fabricate an entire circuit on the sidewalls of a trench. According to a presentation by William Richardson during the advanced DRAM technologies session, this is just what a group of 13 engineers from Texas Instruments did by combining the notions of trench capacitors and vertical transistors to make a DRAM memory cell in three dimensions. The horizontal area of the rectangular memory cell was only 9 square micrometers.

Richardson also reported that the Texas Instruments group has used the vertical memory cell in the fabrication of a 4-megabit DRAM despite the fact that, except for the vertical structure, fabrication processes were generically the same as those now used in 1-megabit DRAM's. For example, the cell had minimum feature sizes of 1 micrometer, while other advanced DRAM concepts presented at the meeting relied on submicrometer dimensions.

In essence, the Texas Instruments group simply stacked a simplified version of NTT's vertical transistor atop a trench capacitor. Total depth of the rectangular 1.3 by 1.5 square micrometer trench was a hefty 8 micrometers, the top 2 micrometers of which were devoted to the pass-gate transistor. Although the two groups worked entirely independently, their respective transistors behave quite similarly. Richardson characterized them to *Science* as "good transistors" with performance comparable to conventional devices.

The capacitor part of the trench was embedded in electrically conducting, heavily *p*-type silicon material, which served as one capacitor plate. *N*-type polycrystalline silicon filler inside the trench acted as the second plate. In a DRAM memory cell, the source electrode of the pass-gate transistor connects directly to one of the capacitor plates, in this case the polycrystalline silicon trench filler. Since the connection between the transistor source and one capacitor plate is made internally, there is no need to provide for access to the source from the surface; that is, no guide electrode is necessary, as in the NTT T-MOS device. ■

ARTHUR L. ROBINSON