Although the RNA components of the *E. coli* and *B. subtilis* enzymes are demonstrably different—a gene probe from *E. coli* does not hybridize with the *B. subtilis* genome—each can cleave the natural transfer RNA substrates of the other. Differences in primary sequence of the RNA molecules—both of which measure around 370 nucleotides long—does not necessarily translate to differences in secondary and tertiary structure, however. Pace is especially interested in comparing secondary structure arrangements in the RNA from several organisms to see which aspects are conserved: these are likely to be the functional parts. He expects to have the primary sequence of the *B. subtilis* RNA within weeks and a second one soon thereafter. Both Pace and Altman plan to modify the RNA's—by insertions, deletions, and specific mutations—as a way of dissecting the functionally operative domains of the molecules.

In addition to cleaving a tail section from transfer RNA precursors, ribonuclease P in *E. coli* is also responsible for a similar processing reaction on an enigmatic molecule called 4.5*S* RNA. In this reaction only the ribonuclease P RNA from *E. coli* will work in vitro, not that from *B. subtilis*, and only then when it is combined with a protein component, which can be from either organism. The catalytic activity must be a little different in this case, as well as there being a clear species specificity with respect to the RNA component of the enzyme.

RNA molecules are highly flexible entities, especially when compared with the relatively rigid strands of DNA, and have a greater facility than proteins for action over large distances. So, far from being the dumb slaves of the all mighty DNA, RNA molecules have great functional potential.

This latest discovery with ribonuclease P will undoubtedly spur the systematic search for further examples of RNA as catalyst, of which there are many potential candidates. In addition to the well-established occurrences of protein and RNA combinations—for instance, in the ribosome, several classes of ribonucleoprotein particles in the nucleus and cytoplasm, and the recently discovered signal recognition particle—in which the RNA might possibly be playing more than a passive structural role, there are scores of small RNA molecules in all cells for which no function has yet been identified.

Furthermore, there are at least two cases of enzyme activity that apparently require the presence of an RNA molecule. One, reported last October by Max Birnstiel's group at Zurich University, Switzerland, implicates a 60 nucleotide RNA in the processing of a histone messenger RNA in a sea urchin species. Another, worked on by a Russian group, involves the modification of the carbohydrate amylose by an RNA-containing enzyme. If this latter case were to be confirmed as truly catalytic RNA, it would be the first example of an RNA catalyst effecting a chemical modification in a non-RNA substrate.

For those interested in the origin of life, the existence of RNA catalysts offers an intriguing glimpse of a former, more primitive age when the full range of metabolic and genetic machinery had yet to evolve. If, as now seems certain, RNA molecules can perform a range of catalytic functions in addition to being carriers of information, the old origins conundrum of "protein before DNA or DNA before protein?" is mercifully eschewed.—ROGER LEWIN

One Billion Transistors on a Chip?

The annual rate of increase in numbers of transistors on a chip is slowing as theoretical limits are neared, but there may be a billion by the year 2000

It could happen by the turn of the century, according to James Meindl, director of Stanford University's Center for Integrated Systems. Meindl's forecast came in the opening session of the 3-day International Electron Devices Meeting, held in Washington, D.C., early in December. For comparison, the most densely packed integrated circuits at present cram about 600,000 transistors onto a silicon chip about 6 millimeters on a side. Moreover, these integrated-circuit chips, random access memories that store 262,144 binary bits of information (so-called 256K RAM's), will not be commercially available for another year or two.

Projection of the future course of semiconductors has become a liturgical requirement of integrated circuit meetings since Gordon Moore of the Intel Corporation formulated "Moore's law" in the mid-1970's. Moore observed that the number of transistors on a chip had been roughly doubling each year since Texas Instruments and Fairchild Semiconductor independently developed the integrated circuit in 1959. From 1973 to the present, the rate of growth has been slightly lower, the number of transistors per chip increasing by a factor of 4 every 3 years. A continuation of this trend would find integrated circuits of over 10 billion transistors by the year 2000.

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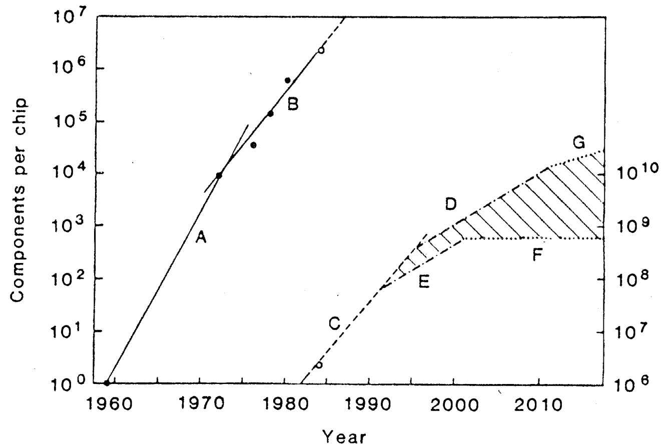
Meindl's message, then, is that further moderation of the growth curve is in store. Depending on certain assumptions pertaining to the fabrication technology, the number of transistors per chip may climb to a number ranging from "only" several hundred million to about 1 billion in the next 16 years. The reason for the anticipated decline in rate is that engineers are approaching a number of theoretical and practical limits on the minimum size of transistors. Their situation is like that of a football team that finds it harder to advance the ball as it nears its opponent's goal line because there is less room for maneuvering.

Meindl calls this future era ULSI, for ultralarge-scale integration, as opposed to the current VLSI or very-large-scale-integration epoch. The upcoming generation of 256K RAM's have minimum feature sizes ranging from 1.3 to 2.5 micrometers. The minimum feature size is usually defined as the average of the width of the electrical conductors that connect transistors and the spacing be-



Chip future

Transistors per chip doubled yearly in segment A but the rate dropped in segment B to a doubling every year and a half. Segments C, D, E, F, and G are projections. E and F assume a 0.5 micrometer minimum feature size, whereas D and G assume a 0.25 micrometer limit. [Source: J. D. Meindl, Stanford University]

tween the conductors. ULSI circuits will reach minimum feature sizes of 0.25 micrometer by the end of the century, said Meindl, and possibly even smaller later on.

To examine theoretically the consequences of reducing the size of transistors, engineers start with existing device and circuit designs and simply reduce all the physical dimensions by a fixed factor S, the scaling factor. As for the operating voltages, there are two principal choices. One can scale them by the same factor S in order to maintain a constant electric field as transistor size goes down, or one can keep the voltage constant. Constant voltage is easier to implement because the standard industry power supplies can be kept. However, the heat per unit area of the chip produced by the current through the transistors rises as S^3 and eventually could be enough to damage the chip.

The alternative of a constant field solves the heat problem but ultimately runs into trouble in the form of fundamental limits due to the basic laws of physics. For example, thermodynamics dictates that there is always a certain amount of noise in electrical devices. The signal in a useful device must exceed the noise by a reasonable factor (a factor of 4 in Meindl's examples). This sets a limit on the minimum useful voltage.

Engineers rate the performance of transistors by the time delay suffered by a signal as it passes through the device and by the power expended in the process. The best transistors have the smallest time delay–power dissipation product. Meindl reported some of his findings in this form, but they can be converted to device dimensions, since speed scales with size. Applying constant electric field scaling means that today's 5-volt operating levels would be reduced to 0.5 volt at room temperature. Scaling 2-micrometer minimum feature sizes by the same factor results in 0.2-micrometer features. Even smaller dimensions would result from lowering the operating temperature.

Thermodynamics represents a fundamental limit on semiconductor size and performance. Meindl considered a hierarchy of limits, ranging from fundamental to circuit-specific. The next one relates to the material itself. Each semiconductor has a maximum electric field it can withstand before the material breaks down. The minimum length of semiconductor is therefore the applied voltage divided by the breakdown field. For silicon with 1 volt applied, this length is about 0.03 micrometer. Electrons traveling at their maximum velocity in silicon would take 0.4 picosecond to travel this distance, corresponding to the minimum time delay for a silicon device.

As it happens, no real transistor begins to approach the performance suggested as ultimately possible by this limit. At the next level of the hierarchy, however, the transistor structure itself imposes bounds on device speed that are within hailing distance. Meindl treated the case of metal-oxide-semiconductor (MOS) transistors. Current in an MOS transistor flows between a part called the source and another part called the drain when the device is in the "on" state. Current cannot flow when the transistor is "off." An applied "gate" voltage controls whether the transistor is on or off.

However, if the source and drain are too close together, current can "punch through" between the source and drain even in the off state. The minimum source-drain separation or "channel length" and the maximum charge carrier velocity set a minimum time delay of 4 picoseconds, about a factor of 10 larger than that due to the material itself for the case of silicon MOS transistors. The shortest allowable channel lengths range from about 0.4 to 0.2 micrometer, depending on the circuit the MOS transistor is used in, according to a model developed by J. R. Pfiester of Stanford.

For comparison with the state of the art in the laboratory, consider the findings of Ping Ko and several co-workers from Bell Laboratories, who reported at the electron device meeting that they achieved a time delay as low as 33 picoseconds in simple test circuits. The effective channel length in their transistors under these conditions was 0.5 micrometer. They said that this is the smallest delay per effective channel length yet reported for silicon MOS devices.

One reason the Bell Labs team did not do better is that real transistors have a capacitance. The outcome is an RC time constant that limits the speed. The Bell Labs researchers reduced the unwanted or parasitic capacitance to a new low but could not reduce it altogether.

Circuits, which are the next level in the hierarchy of limits above devices, comprise more than transistors. In particular, resistors have to be scaled. Although this might seem a trivial task compared to scaling transistors, it happens that the most popular resistor material, polycrystalline silicon, cannot be used conveniently in lengths shorter than about 1 micrometer and still behave as an ideal resistor that obeys Ohm's law.

Finally, the conductors that connect the circuit components impose their own limitations. As circuit dimensions are scaled down, the RC time constant due to the resistance and capacitance associated with the conductors remains unchanged. Eventually, during scaling, this delay time could exceed the decreasing transistor delay time and further reduction in size does not improve performance.

In making his projections for progress in miniaturizing integrated circuits, Meindl combined these and related theoretical limitations—in particular the minimum MOS transistor channel length—with historical trends, which he called practical limitations. Over the last three decades, the size of transistor features has decreased at a characteristic rate, while the size of the chip itself has increased continually. The ability of circuit designers to devise configurations that pack more transistors of a given size into the same area seems to be leveling off. All three factors contribute to the total number of transistors per chip.

Meindl's projections bracket a range of chip densities corresponding to minimum MOS transistor feature sizes from 0.5 to 0.25 micrometer. The smaller number leads to about 1 billion transistors per chip by the year 2000 (see figure).—**Arthur L. Robinson**