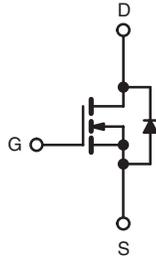
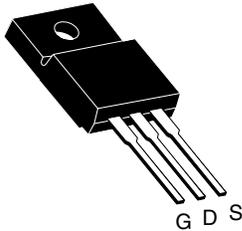




Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	600
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V 0.75
Q <sub>g</sub> (Max.) (nC)	49
Q <sub>gs</sub> (nC)	13
Q <sub>gd</sub> (nC)	20
Configuration	Single

TO-220 FULLPAK



N-Channel MOSFET

FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC



RoHS\* COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)

TYPICAL SMPS TOPOLOGIES

- Single Transistor Forward
- Active Clamped Forward

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB6N60APbF
	SiHFIB6N60A-E3
SnPb	IRFIB6N60A
	SiHFIB6N60A

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	600	V
Gate-Source Voltage	V <sub>GS</sub>	± 30	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	5.5
		T <sub>C</sub> = 100 °C	3.5
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	37	
Linear Derating Factor		0.48	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	290	mJ
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>	9.2	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	6.0	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	60
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10
			1.1

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T<sub>J</sub> = 25 °C, L = 6.8 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 9.2 A (see fig. 12).
- I<sub>SD</sub> ≤ 9.2 A, dI/dt ≤ 50 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

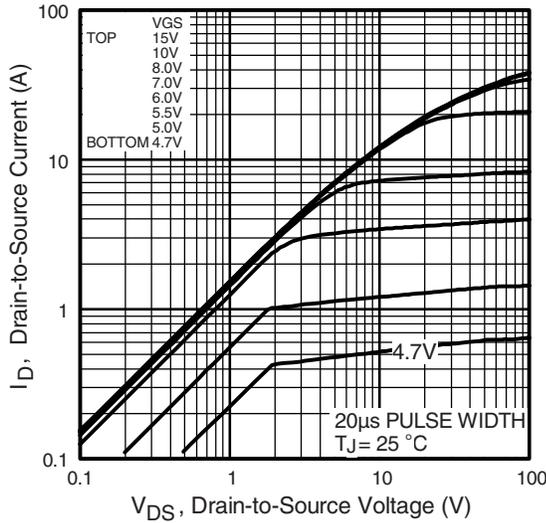
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	660	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}^b$	-	-	0.75	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 5.5\text{ A}$	5.5	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	1400	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	180	-	
Reverse Transfer Capacitance	$C_{rss}$		-	7.1	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1957	-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	49	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	96	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 9.2\text{ A}, V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	49	nC
Gate-Source Charge	$Q_{gs}$		-	-	13	
Gate-Drain Charge	$Q_{gd}$		-	-	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 9.2\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 35.5\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	13	-	ns
Rise Time	$t_r$		-	25	-	
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	
Fall Time	$t_f$		-	22	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	37	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	530	800	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.0	4.4	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

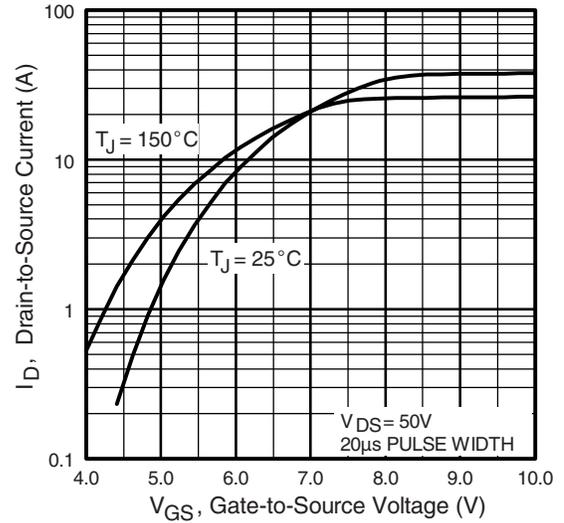
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .
- $t = 60\text{ s}, f = 60\text{ Hz}$ .

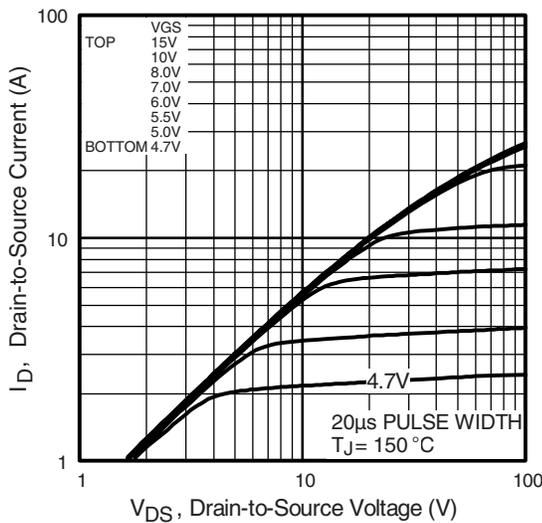
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



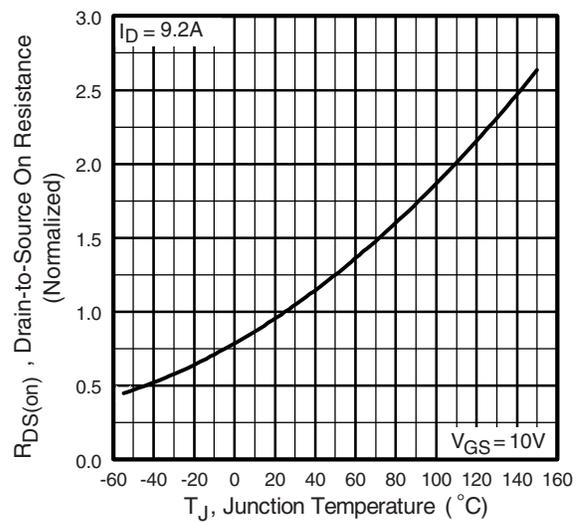
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

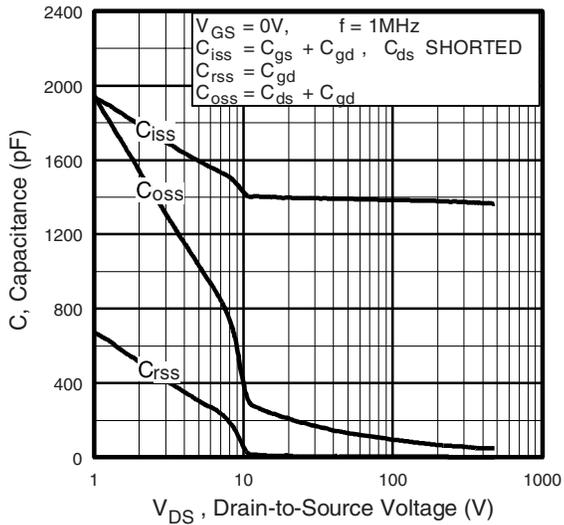


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

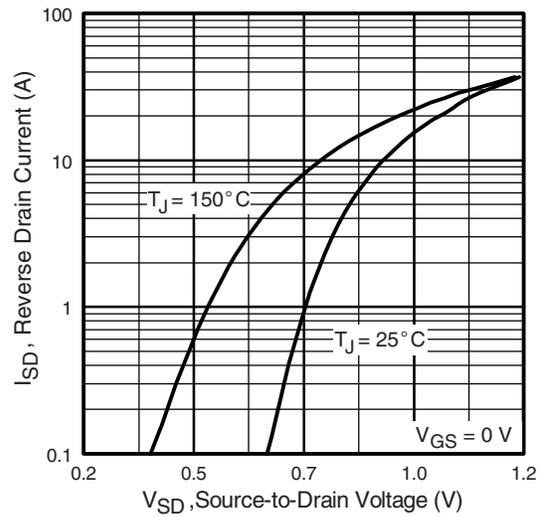


Fig. 7 - Typical Source-Drain Diode Forward Voltage

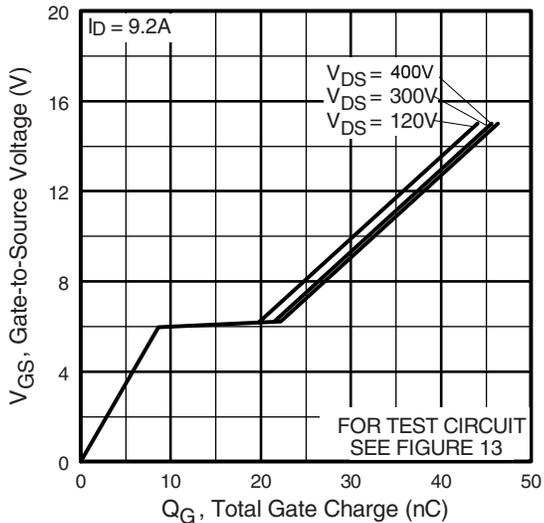


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

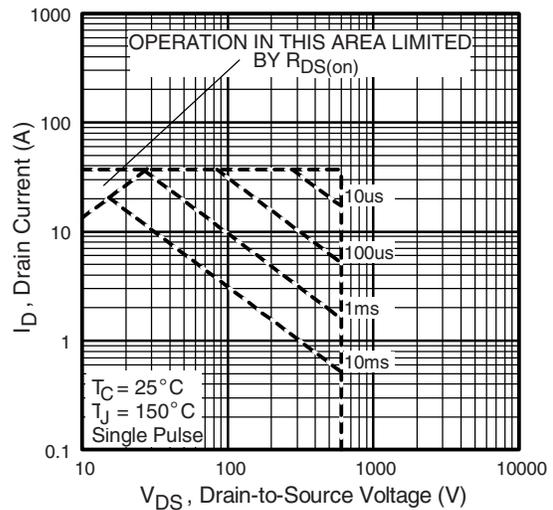


Fig. 8 - Maximum Safe Operating Area

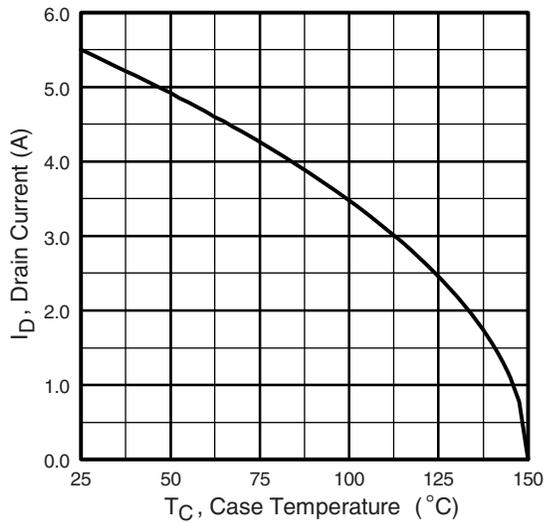


Fig. 9 - Maximum Drain Current vs. Case Temperature

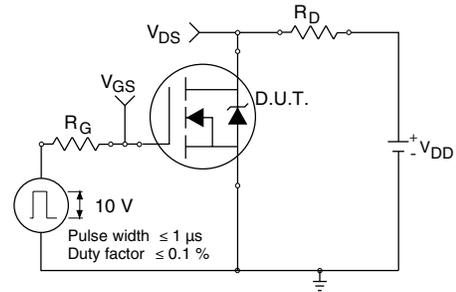


Fig. 10a - Switching Time Test Circuit

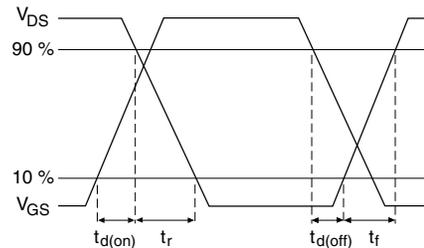


Fig. 10b - Switching Time Waveforms

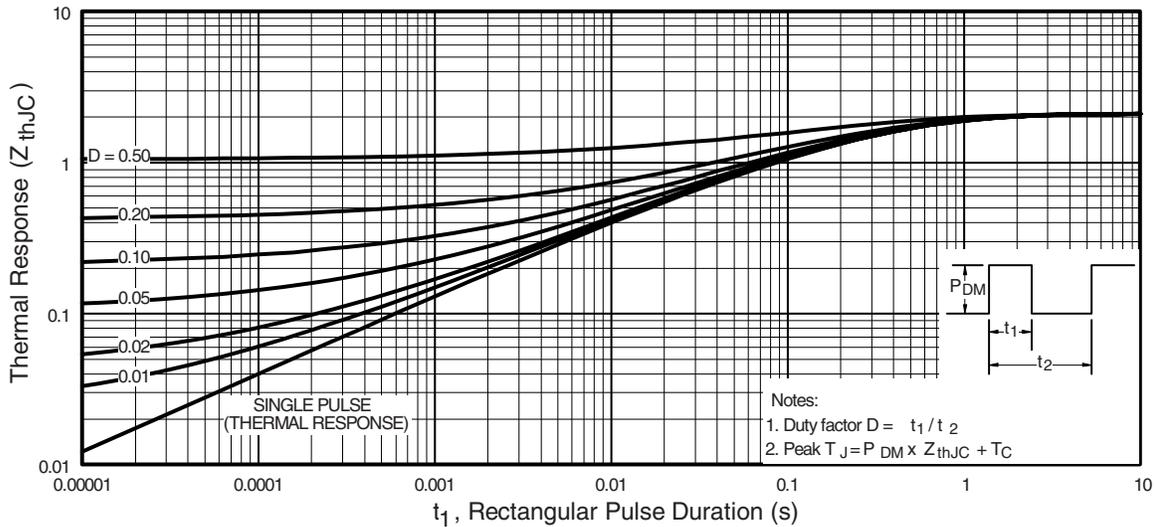


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

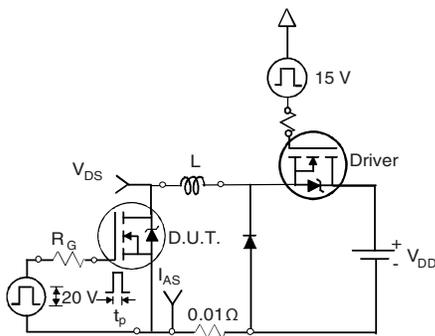


Fig. 12a - Unclamped Inductive Test Circuit

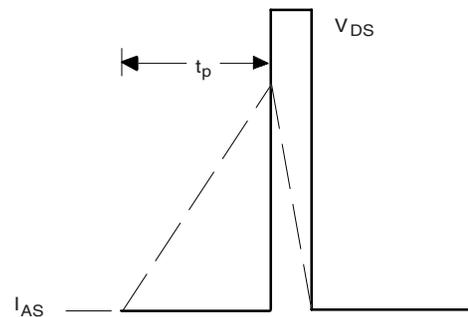
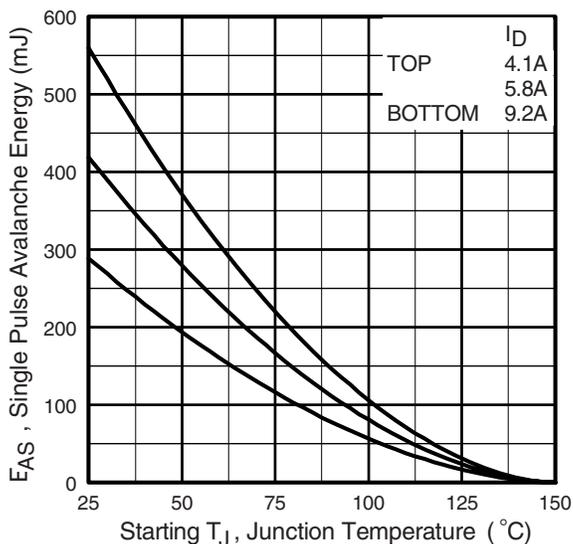
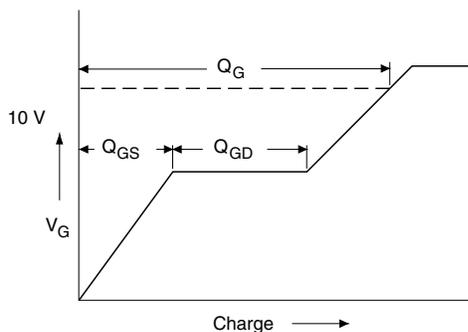


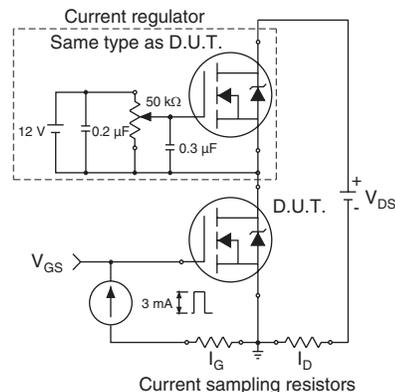
Fig. 12b - Unclamped Inductive Waveforms



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

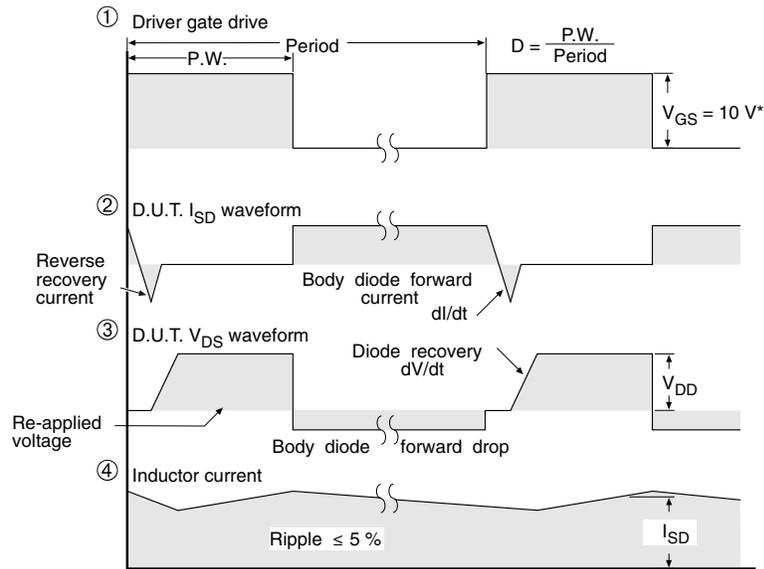
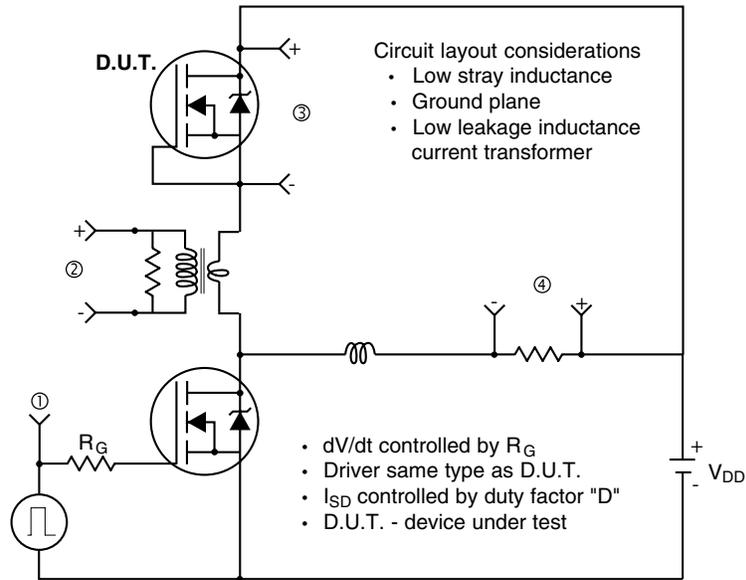


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

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