ISO724x High-Speed, Quad-Channel Digital Isolators

1 Features

- 25 and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns Maximum
  - Low Pulse-Width Distortion (PWD); 2 ns Maximum
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Selectable Default Output (ISO7240CF)
- > 25-Year Life at Rated Working Voltage (See Application Note SLLA197 and Figure 16)
- 4-kV ESD Protection
- Operates With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (See Application Report SLLA181)
- –40°C to 125°C Operating Temperature Range
- Safety and Regulatory Approvals:
  - VDE 4000 V_{PK} Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 2.5 kV_{RMS} Isulation for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A and IEC 60950-1 End Equipment Standard

2 Applications

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7240x, ISO7241x, and ISO7242x devices are quad-channel digital isolators with multiple channel configurations and output-enable functions. These devices have logic-input and logic-output buffers separated by Texas Instrument's silicon-dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices help block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

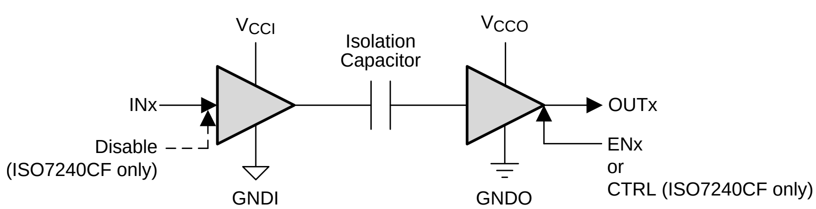
The ISO7240x family of devices has all four channels in the same direction. The ISO7241x family of devices has three channels in the same direction and one channel in the opposition direction. The ISO7242x family of devices has two channels in each direction.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7240CF	SOIC (16)	10.30 mm × 7.50 mm
ISO7240C		
ISO7240M		
ISO7241C		
ISO7241M		
ISO7242C		
ISO7242M		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (September 2015) to Revision S — **Page**

- Changed the HBM value from ±4 V to ±4000 V and the CDM value from ±1 V to ±1000 V in the *ESD Ratings* table ... 9
- Moved the device power dissipation parameter from the *Thermal Information* table to the *Power Dissipation Characteristics* table ... 13

Changes from Revision Q (January 2015) to Revision R — **Page**

- Changed *Features* From: "Basic Isolation per DIN EN 60747-5-5 (VDE 0884-5) & DIN EN 61010-1" To:"Basic Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" ... 1
- Changed V_{CC1} To V_{CCI}, V_{CC2} To V_{CCO}, GND1 To GNDI, and GND2 To GNDO, and added Notes 1 and 2 to the *Simplified Schematic* ... 1
- Changed V_{OH} MIN values From: V_{CC} - 0.8 To: V_{CCO} - 0.8 and V_{CC} - 0.1 To: V_{CCO} - 0.1 in the *Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V(1) Operation* ... 10
- Changed V_{OH} Test Condition ISO7240 To: 3.3-V side and the MIN value From: V_{CC} - 0.4 To V_{CCO} -0.4 in the *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* ... 11
- Changed V_{OH} Test Condition ISO724x (5-V side) To: 5-V side and the MIN value From: V_{CC} - 0.8 To: V_{CCO} - 0.8 in the *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* ... 11
- Changed V_{OH}, Test Condition I_{OH} = -20 µA MIN value From: V_{CC} - 0.1 To V_{CCO} - 0.1 in the *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* ... 11
- Changed V_{OH} Test Condition ISO7240 To: 3.3-V side and the MIN value From: V_{CC} - 0.4 To V_{CCO} -0.4 in the *Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation* ... 12
- Changed V_{OH} Test Condition ISO724x (5-V side) To: 5-V side and the MIN value From: V_{CC} - 0.8 To: V_{CCO} - 0.8 in the *Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation* ... 12

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- Changed V_{OH}, Test Condition I_{OH} = -20 µA MIN value From: V_{CC} - 0.1 To V_{CCO} - 0.1 in the *Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation* 12
- Changed V_{OH} MIN values From: V_{CC} - 0.4 To: V_{CCO} - 0.4 and V_{CC} - 0.1 To: V_{CCO} - 0.1 in the *Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation* 13
- Changed V_{CC1} To: V_{CCI} and V_{CC2} To: V_{CCO} in Figure 13 22
- Changed section title From: *DIN EN 60747-5-5 Insulation Characteristics* To: *DIN V VDE V 0884-10 (VDE V 0884-10):2006-1 Insulation Characteristics*(1) 24
- Changed R_S Test Conditions From: V_{IO} = 500 V at T_S To: V_{IO} = 500 V at T_S = 150°C in the *DIN V VDE V 0884-10 (VDE V 0884-10):2006-1 Insulation Characteristics*(2) table........ 24
- Changed the CTI Test Conditions From: IEC 60112/VDE 0303 Part 1 To: DIN EN 60112 (VDE 0303-11); IEC 60112 in the *Package Characteristics* table 24
- Deleted C_I - Input capacitance to ground from the *Package Characteristics* table 24
- Changed title From: *IEC Safety Limiting Values* To: *Safety Limiting Values* 25
- Changed Figure 17 title From: *Thermal Derating Curve per DIN EN 60747-5-5* To: *Thermal Derating Curve per VDE* 25
- Changed "DIN EN 60747-5-5 & DIN EN 61010-1" To: DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07 in the *Regulatory Information* table........ 26

(1) Climatic Classification 40/125/21

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- Changed the V_I MAX value in the *Absolute Maximum Ratings* table From: 6 V To: V_{CC} + 0.5 V........ 9
- Added Note 3 to the *Absolute Maximum Ratings* table........ 9
- Moved T_{STG} - Storage From the *ESD Ratings* table to the *Absolute Maximum Ratings* table 9
- Changed the *Handling Rating* table to the *ESD Ratings* table. 9
- Added one row to Table 4. Values: X, PD, X, X, X, Undetermined 26
- Added one row to Table 3. Values: X, PD, X, X, Undetermined 26
- Changed Figure 18 labels From: "ISO7240CF Input" To: "ISO7240CF Input, Disable" and From: "Enable" To: "Enable, Control" 27

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- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed ISO7241C minimum supply from 2.8 V to 3.15 V........ 9

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- Added the *Safety Limiting Values* section........ 25

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- Changed Feature From: Operates 3.3-V or 5-V Supplies To: Operates With 2.8-V (ISO7241C), 3.3-V or 5-V Supplies..... 1
- Added device options to V_{CC} in the RECOMMENDED OPERATING CONDITIONS table 9
- Changed Table Note (1)........ 9
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} and V_{CC2} at 5-V *Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V(1) Operation* table 10
- Changed Table Note (1)........ 10
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 5-V, V_{CC2} at 3.3-V *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* table 11

- Changed Table Note (1) 11
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- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} and V_{CC2} at 3.3 V table 13
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- Added ELECTRICAL and Switching CHARACTERISTICS tables forV_{CC1} and V_{CC2} at 2.8V (ISO722xC-only).......... 13
- Changed Figure 6 From V_{CC1} Failsafe Threshold To: V_{CC} Undervoltage Threshold.......... 18
- Changed the CTI MIN value From: ≥175 V To:≥400 V 24
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- Changed Figure 9, Figure 11, and Figure 12 20
- Changed the CSA File Number From: 1698195 To: 220991 26

Changes from Revision K (Decemberl 2009) to Revision L **Page**

- Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table.......... 24
- Added the IEC 60664-1 RATINGS TABLE 24
- Added CTI - Tracking resistance (comparative tracking index to the *Package Characteristics* table.......... 24

Changes from Revision J (April 2009) to Revision K **Page**

- Changed the Input circuit in the DEVICE I/O SCHEMATICS illustration 1
- Added Note 1 to LI01), and changed the MIN value From: 8.34 To 8 mm in the *Package Characteristics* table 24
- Added Note 1 to LI02), and changed the MIN value From: 8.1 To 8 mm in the *Package Characteristics* table 24

Changes from Revision I (December 2008) to Revision J **Page**

- Changed I_{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA 10
- Changed I_{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA 11

Changes from Revision G (July 2008) to Revision H **Page**

- Added Device number ISO7240CF. 1
- Added Features Bullet: Selectable Failsafe Output (ISO7240CF) 1
- Changed description paragraph 4 text. 7
- Changed V_I in the *Absolute Maximum Ratings* table From: Voltage at IN, OUT, EN To: Voltage at IN, OUT, EN, DISABLE, CTRL 9
- Added t_{wake}, Wake time from input disable.......... 14
- Added t_{wake}, Wake time from input disable.......... 15
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- Changed the *Package Characteristics* table, line , $L_{(IO1)}$ MIN value from7.7mm to 8.34mm.......... 24

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Changes from Revision E (May 2008) to Revision F **Page**

- Deleted ISO724xA devices. See SLLS905 for the ISO7240A, ISO7241A, and ISO7242A. 1
- Changed Title From: QUAD DIGITAL ISOLATORS To: HIGH SPEED QUAD DIGITAL ISOLATORS 1
- Changed Feature Low Jitter Content - From: 1, 25, and 150-Mbps Signaling Rate Options To: 25, and 150-Mbps Signaling Rate Options 1
- Added $t_{sk(pp)}$ footnote. 14
- Added $t_{sk(o)}$ footnote. 14
- Added $t_{sk(pp)}$ footnote. 17
- Added $t_{sk(o)}$ footnote. 17

Changes from Revision D (April 2008) to Revision E **Page**

- Added Table Note (1): For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. 9
- Added Table Note (1): For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V 11
- Added Table Note (1): For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V 12
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- Added $t_{sk(pp)}$ Part-to-part skew 14
- Added $t_{sk(pp)}$ Part-to-part skew 15
- Added $t_{sk(pp)}$ Part-to-part skew 16
- Added $t_{sk(pp)}$ Part-to-part skew 17
- Changed Typical ISO724x Application Circuit Figure 19 28

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- Deleted Min = 4.5 V and max = 5.5 V for Supply Voltage of the ROC Table. 9
- Changed V_{CC} Supply Voltage in the ROC Table From: 3.6 To: 5.5 9

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- Changed V_{CC} Supply Voltage in the ROC Table From: 3.45 To: 3.6 9

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- Changed V_{CC} Supply Voltage in the ROC Table From: 3.6 To: 3.45 9
- Changed V_{CC} Supply Voltage in the ROC Table From: 3 To: 3.15 9
- Changed TBDs to actual values. 10
- Changed C_I - typ value From: 1 To: 2 in the *Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V(1) Operation* 10
- Changed C_I - typ value From: 1 To: 2 in the *Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation* 11
- Changed C_I - typ value From: 1 To: 2 in the *Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation* 12
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- Changed Figure 1, Figure 2, and Figure 4. Added Figure 3. 18
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5 Description (Continued)

The devices with the C suffix (C option) have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The devices with the M suffix (M option) have CMOS $V_{CC}/2$ input thresholds and do not have the input noise filter or the additional propagation delay.

The ISO7240CF device has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe output is a logic high when a logic high is placed on the CTRL pin or it is left unconnected. If a logic low signal is applied to the CTRL pin, the failsafe output becomes a logic-low output state. The input disable function of the ISO7240CF device prevents data from being passed across the isolation barrier to the output. When the inputs are disabled or V_{CC1} is powered down, the outputs are set by the CTRL pin.

These devices can be powered from 3.3-V or 5-V supplies on either side, in any combination. The signal input pins are 5-V tolerant regardless of the voltage supply level that is used.

These devices are characterized for operation over the ambient temperature range of –40°C to +125°C.

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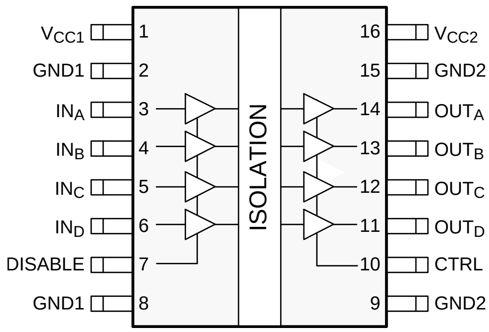
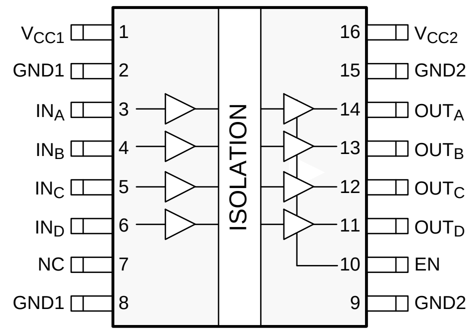
6 Pin Configurations and Functions

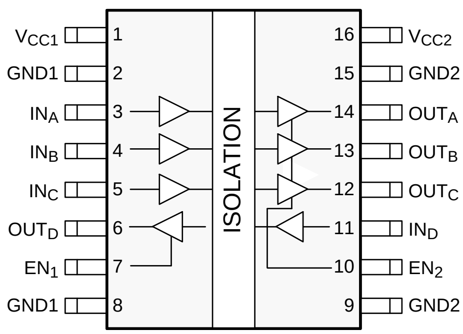
ISO7240CF DW Package
16-Pin SOIC
Top View



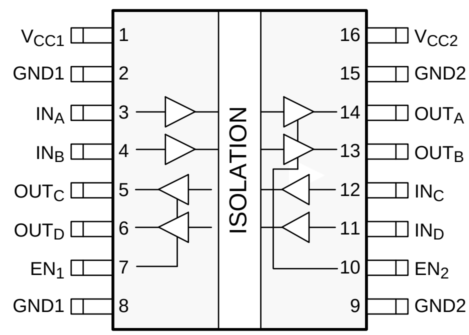
ISO7240C and ISO7240M DW Package
16-Pin SOIC
Top View



ISO7241C and ISO7241M DW Package
16-Pin SOIC
Top View



ISO7242C and ISO7242M DW Package
16-Pin SOIC
Top View



Pin Functions

PIN					I/O	DESCRIPTION3
NAME	NO.					
	ISO7240CF	ISO7240C ISO7240M	ISO7241C ISO7241M	ISO7242C ISO7242M		
CTRL	10	—	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V_{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	10	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN_1	—	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN_1 is high or open and disabled when EN_1 is low.
EN_2	—	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN_2 is high or open and disabled when EN_2 is low.
GND1	2, 8	2, 8	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	9, 15	9, 15	—	Ground connection for V_{CC2}
IN_A	3	3	3	3	I	Input, channel A
IN_B	4	4	4	4	I	Input, channel B
IN_C	5	5	5	12	I	Input, channel C
IN_D	6	6	11	11	I	Input, channel D
NC	—	7	—	—	—	No Connect pins are floating with no internal connection
OUT_A	14	14	14	14	O	Output, channel A
OUT_B	13	13	13	13	O	Output, channel B
OUT_C	12	12	12	5	O	Output, channel C
OUT_D	11	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	16	—	Power supply, V_{CC2}

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7 Specifications

7.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT, EN, DISABLE, CTRL	–0.5	V_{CC} + 0.5 (3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM), per ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (1), V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width	ISO724xC	40			ns
		ISO724xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO724xC	0	30 (2)	25	Mbps
		ISO724xM	0	200 (2)	150	
V_{IH}	High-level input voltage (IN)	ISO724xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	V
V_{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	ISO724xC	2		5.5	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)		0		0.8	V
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
(2) Typical value at room temperature and well-regulated power supply.

7.4 Thermal Information

THERMAL METRIC(1)			ISO724xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K board	168	°C/W
		High-K board	77.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter		41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V(1) Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		1	3	mA
		25 Mbps	12.5-MHz input-clock signal			7	10.5	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps	12.5-MHz input-clock signal			12	18	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps	12.5-MHz input-clock signal			15	24	
I_{CC2}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		15	22	mA
		25 Mbps	12.5-MHz input-clock signal			17	25	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps	12.5-MHz input-clock signal			18	28	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps	12.5-MHz input-clock signal			15	24	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel				0		µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 9			V_{CCO} – 0.8			V
		I_{OH} = –20 µA, See Figure 9			V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 9					0.4	V
		I_{OL} = 20 µA, See Figure 9					0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current	IN at V_{CCI}					10	µA
I_{IL}	Low-level input current	IN at 0 V			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)				2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 13			25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.

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7.6 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

See (1). Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		1	3	mA
		25 Mbps	12.5-MHz input-clock signal			7	10.5	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps	12.5-MHz input-clock signal			12	18	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps	12.5-MHz input-clock signal			15	24	
I_{CC2}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		9.5	15	mA
		25 Mbps	12.5-MHz input-clock signal			10.5	17	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
		25 Mbps	12.5-MHz input-clock signal			11.5	18	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA
		25 Mbps	12.5-MHz input-clock signal			9	14	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel				0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 9		3.3-V side	V_{CCO} – 0.4			V
				5-V side	V_{CCO} – 0.8			
		I_{OH} = –20 μA, See Figure 9			V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 9					0.4	V
		I_{OL} = 20 μA, See Figure 9					0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current	IN at V_{CCI}					10	μA
I_{IL}	Low-level input current	IN at 0 V			–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)				2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 13			25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.7 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

See [(1)]. Over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		0.5	1	mA
		25 Mbps	12.5-MHz input-clock signal			3	5	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		25 Mbps	12.5-MHz input-clock signal			6.5	11	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA
		25 Mbps	12.5-MHz input-clock signal			9	14	
I_{CC2}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		15	22	mA
		25 Mbps	12.5-MHz input-clock signal			17	25	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps	12.5-MHz input-clock signal			18	28	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps	12.5-MHz input-clock signal			15	24	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 9	3.3-V side	V_{CCO} – 0.4			V
				5-V side	V_{CCO} – 0.8			
			I_{OH} = –20 μA, See Figure 9		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 9				0.4	V
			I_{OL} = 20 μA, See Figure 9				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at V_{CCI}				10	μA
I_{IL}	Low-level input current		IN at 0 V		–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 13		25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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7.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

See (1). Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		0.5	1	mA
		25 Mbps	12.5 MHz Input Clock Signal			3	5	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		25 Mbps	12.5 MHz Input Clock Signal			6.5	11	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps	12.5 MHz Input Clock Signal			9	14	
I_{CC2}	ISO7240C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN at 3 V		9.5	15	mA
		25 Mbps	12.5 MHz Input Clock Signal			10.5	17	
	ISO7241C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
		25 Mbps	12.5 MHz Input Clock Signal			11.5	18	
	ISO7242C/M	Quiescent	$V_I = V_{CC}$ or 0 V	All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps	12.5 MHz Input Clock Signal			9	14	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, single channel			0		μA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 9		V_{CCO} – 0.4			V
			I_{OH} = –20 μA, See Figure 9		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 9				0.4	V
			I_{OL} = 20 μA, See Figure 9				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at V_{CCI}				10	μA
I_{IL}	Low-level input current		IN at 0 V		–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 13		25	50		kV/μs

(1) For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.9 Power Dissipation Characteristics

$V_{CC1} = V_{CC2}$ = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation				220	mW

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7.10 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 9	18		42	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} – t_{PLH}\rvert$	ISO724xC	See Figure 9			2.5	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 9	10		23	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} – t_{PLH}\rvert$	ISO724xM	See Figure 9		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				8	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xM			0	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				2	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 9		2		ns
t_f	Output signal fall time		See Figure 9		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 10		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 10		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 11		12		μs
t_{wake}	Wake time from input disable		See Figure 12		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 14		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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7.11 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 9	20		50	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} – t_{PLH} \rvert$					3	
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM		12		29	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} – t_{PLH} \rvert$				1	2	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
		ISO724xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				3	ns
		ISO724xM			0	1	
t_r	Output signal rise time		See Figure 9		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 11		18		μs
t_{wake}	Wake time from input disable		See Figure 12		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 14		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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7.12 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 9	22		51	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xC	See Figure 9			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 9	12		30	ns
PWD	Pulse-width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO724xM	See Figure 9		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 9		2		ns
t_f	Output signal fall time		See Figure 9		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 10		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 10		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 11		12		μs
t_{wake}	Wake time from input disable		See Figure 12		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 14		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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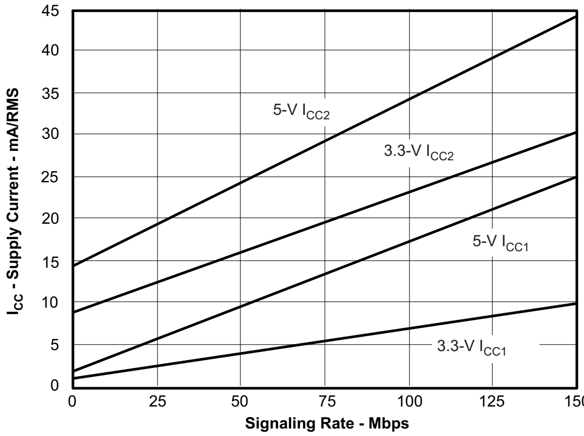
7.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 9	25		56	ns
PWD	Pulse-width distortion $\|t_{PHL} – t_{PLH}\|$ (1)	ISO724xC	See Figure 9			4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 9	12		34	ns
PWD	Pulse-width distortion $\|t_{PHL} – t_{PLH}\|$ (1)	ISO724xM	See Figure 9		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xC				3.5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 9		2		ns
t_f	Output signal fall time		See Figure 9		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 10		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 10		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 10		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 11		18		μs
t_{wake}	Wake time from input disable		See Figure 12		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 14		1		ns

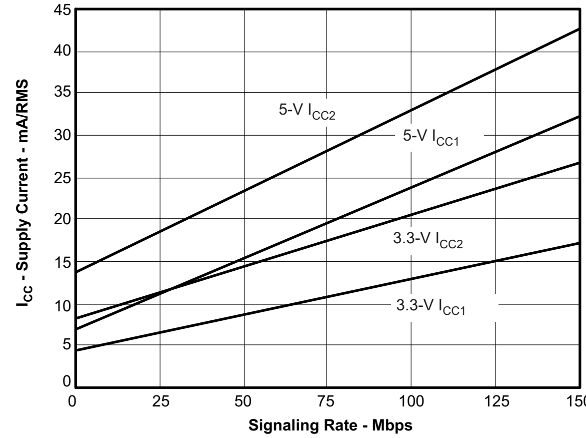
(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.14 Typical Characteristics



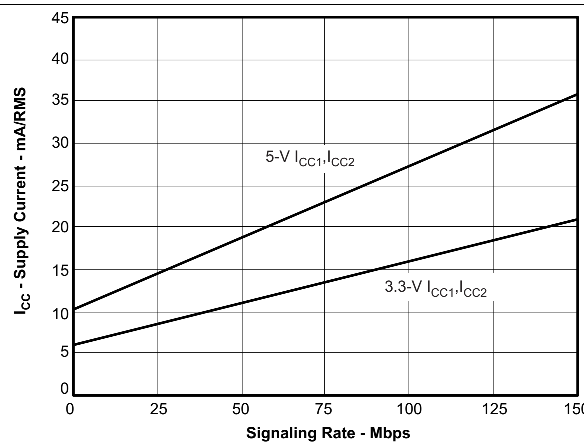
T_A = 25°C   Load = 15 pF   All Channels

Figure 1. ISO7240C/M RMS Supply Current vs Signaling Rate



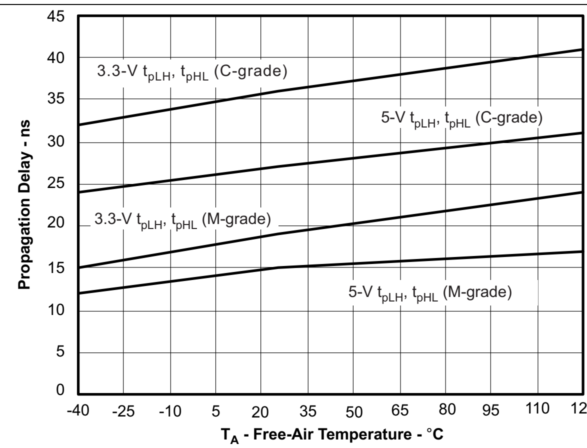
T_A = 25°C   Load = 15 pF   All Channels

Figure 2. ISO7241C/M RMS Supply Current vs Signaling Rate



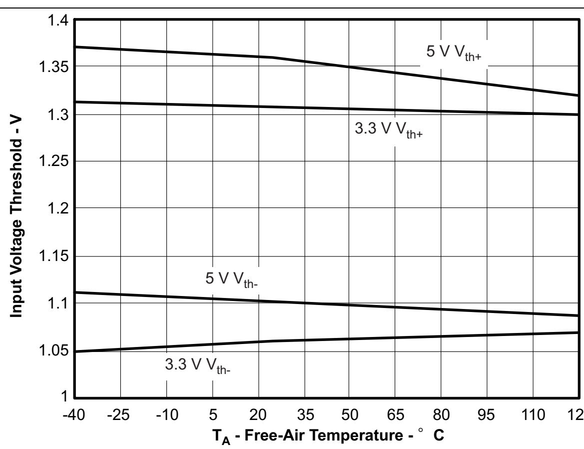
T_A = 25°C   Load = 15 pF   All Channels

Figure 3. ISO7242C/M RMS Supply Current vs Signaling Rate



T_A = 25°C   Load = 15 pF   All Channels

Figure 4. Propagation Delay vs Free-Air Temperature



Air Flow at 7 cf/m   Low_K Board

Figure 5. Input Voltage Threshold vs Free-Air Temperature

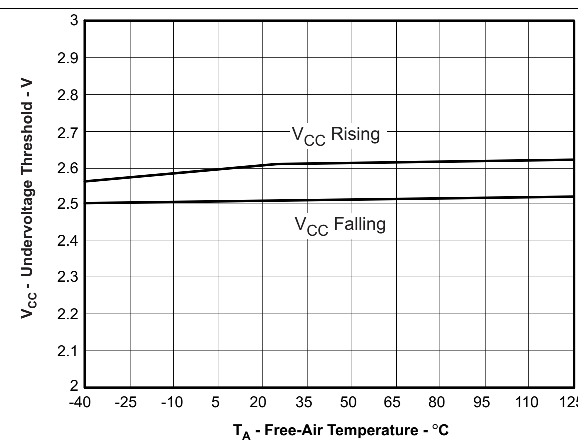


Figure 6. V_{CC} Undervoltage Threshold vs Free-Air Temperature

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Typical Characteristics (continued)

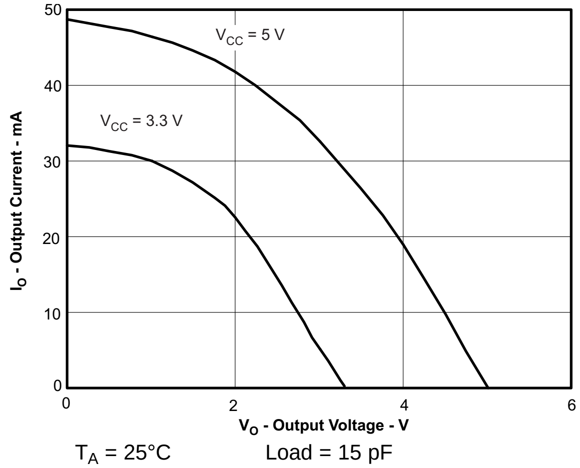


Figure 7. High-Level Output Current vs High-Level Output Voltage

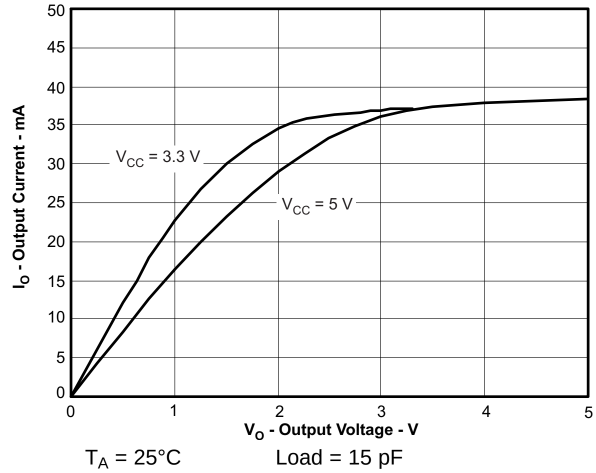
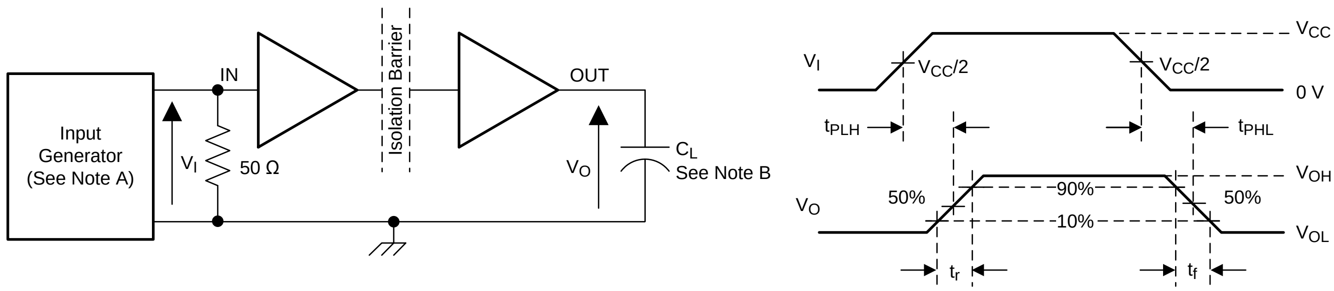


Figure 8. Low-Level Output Current vs Low-Level Output Voltage

8 Parameter Measurement Information



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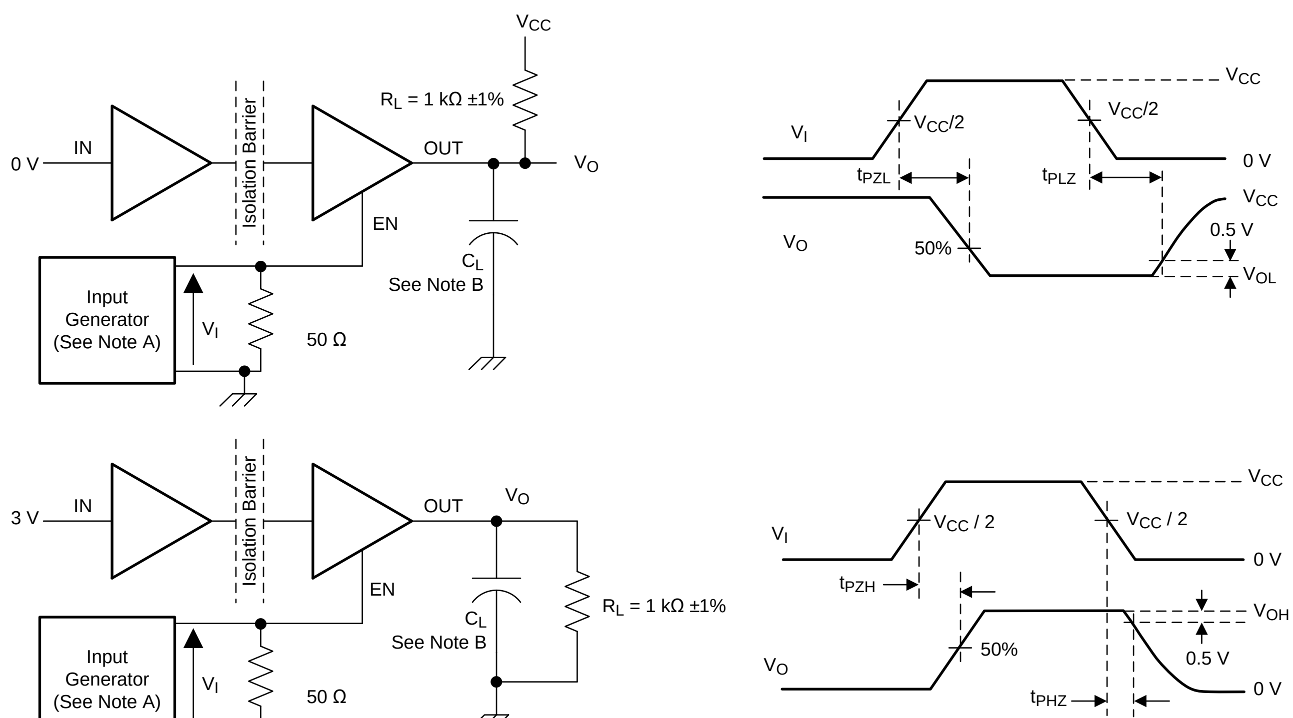
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Switching Characteristic Test Circuit and Voltage Waveforms



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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Enable or Disable Propagation-Delay Time Test Circuit and Waveform

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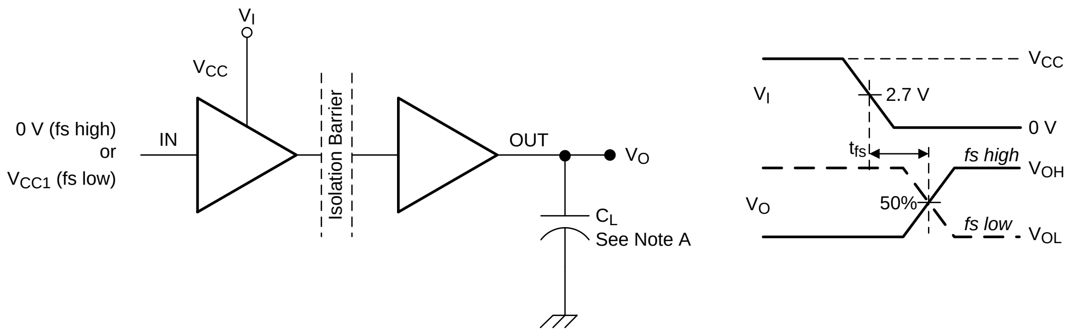
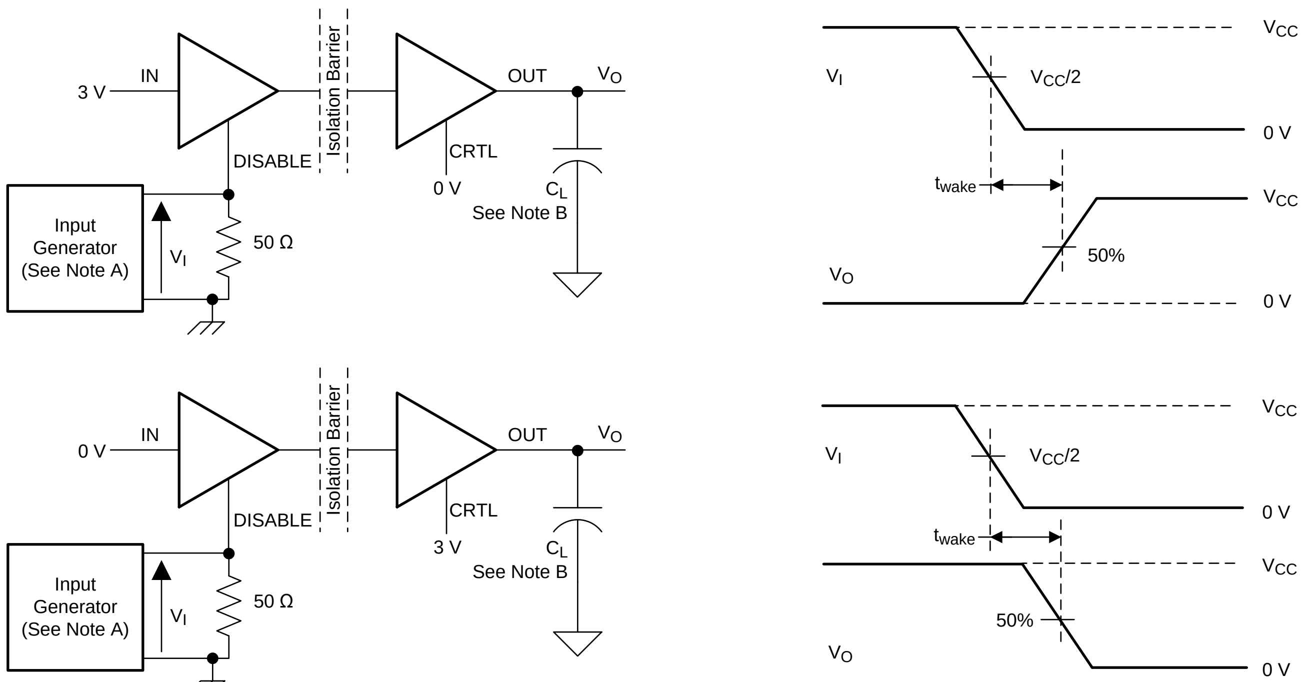
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Failsafe Delay Time Test Circuit and Voltage Waveforms



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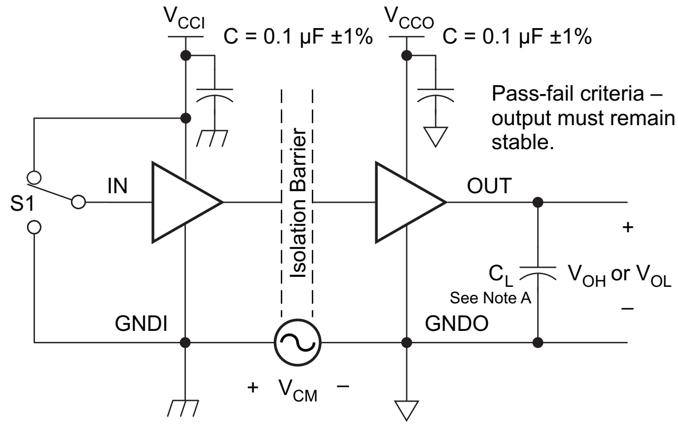
NOTE: The test that yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Wake Time From Input Disable Test Circuit and Voltage Waveforms

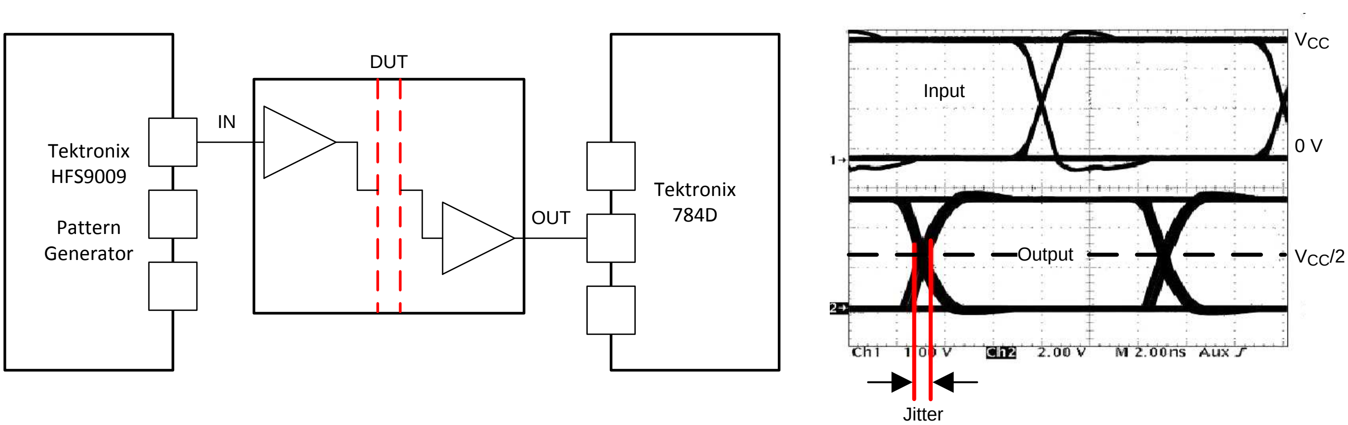
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

Figure 13. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 14. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

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9 Detailed Description

9.1 Overview

The isolator in Figure 15 is based on a capacitive isolation-barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop the output of which feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, as in the case of a low-frequency signal, the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is required to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

9.2 Functional Block Diagram

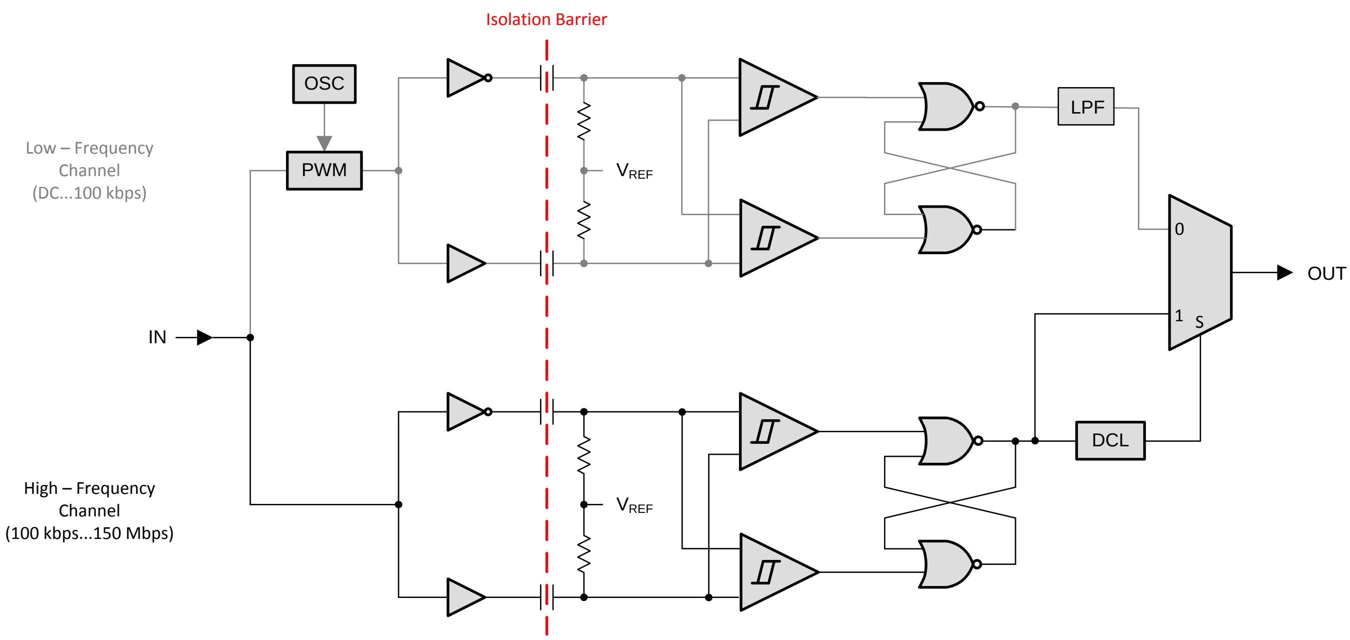

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Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

9.3 Feature Description

The ISO724xx family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. Table 1 lists these device features.

Table 1. Device Features

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240C	25 Mbps	~1.5 V (TTL)	4/0
ISO7240CF	25 Mbps	~1.5 V (TTL)	
ISO7240M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7241C	25 Mbps	~1.5 V (TTL)	3/1
ISO7241M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7242C	25 Mbps	~1.5 V (TTL)	2/2
ISO7242M	150 Mbps	V_{CC}/ 2 (CMOS)	

9.3.1 DIN V VDE V 0884-10 (VDE V 0884-10):2006-1 Insulation Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
V_{IORM}	Maximum working insulation voltage		560	V_{PK}
V_{PR}	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	V_{PK}
		Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V_{PK}
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	t = 60 s	4000	V_{PK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 2. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group 1	Material group	II
Installation classification	Rated mains voltage ≤150 V_{RMS}	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-III

9.3.2 Package Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)(1)	Shortest pin-to-pin distance through air	8			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest pin-to-pin distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$> 10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	$V_I = 0.4 \sin(4E6\pi t)$		2		pF

(1) Per JEDEC package dimensions

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9.3.3 Life Expectancy versus Working Voltage

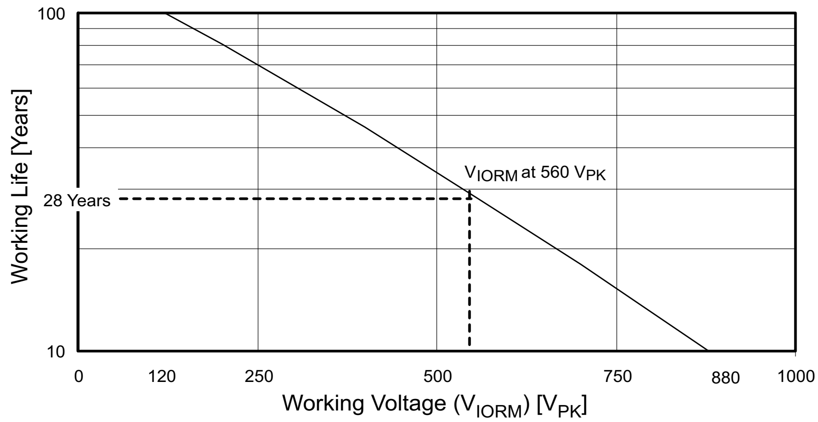

Figure 16. Time-Dependant Dielectric Breakdown Testing Results

9.3.4 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-16	θ_{JA} = 168°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			156	mA
			θ_{JA} = 168°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			239	
T_S	Maximum case temperature	SOIC-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

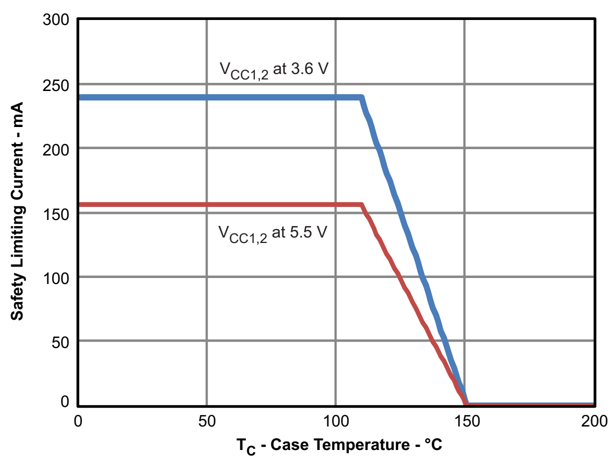

Figure 17. SOIC-16 Θ_{JC} Thermal Derating Curve per VDE

9.3.5 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07	Approved under CSA Component Acceptance Notice 5A	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 560 V_{PK}	Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 395 V_{RMS} maximum working voltage, 4000 V_{PK} maximum isolation rating	Single protection, 2500 V_{RMS} (1)
Certificate Number: 40016131	Master Contract Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

9.4 Device Functional Modes

Table 3 lists the ISO724xx functional modes. Table 4 lists the ISO7240CF functional modes.

Table 3. Device Function Table ISO724x(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

Table 4. ISO7240CF Functions Table(1)

V_{CC1}	V_{CC2}	DATA INPUT (IN)	DISABLE INPUT (DISABLE)	FAILSAFE CONTROL (CTRL)	DATA OUTPUT (OUT)
PU	PU	H	L or Open	X	H
PU	PU	L	L or Open	X	L
X	PU	X	H	H or Open	H
X	PU	X	H	L	L
PD	PU	X	X	H or Open	H
PD	PU	X	X	L	L
X	PD	X	X	X	Undetermined

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance; Open = Not Connected

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9.4.1 Device I/O Schematics

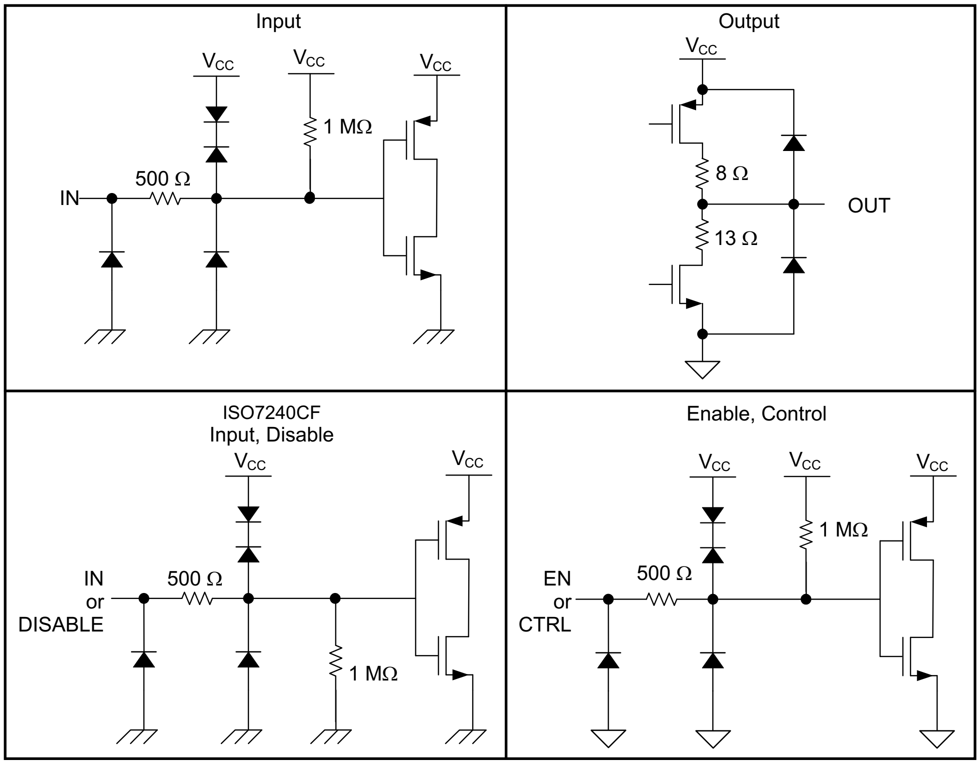

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Figure 18. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO724xx family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

10.2.1 Isolated Data Acquisition System for Process Control

The ISO724xx family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in Figure 19.

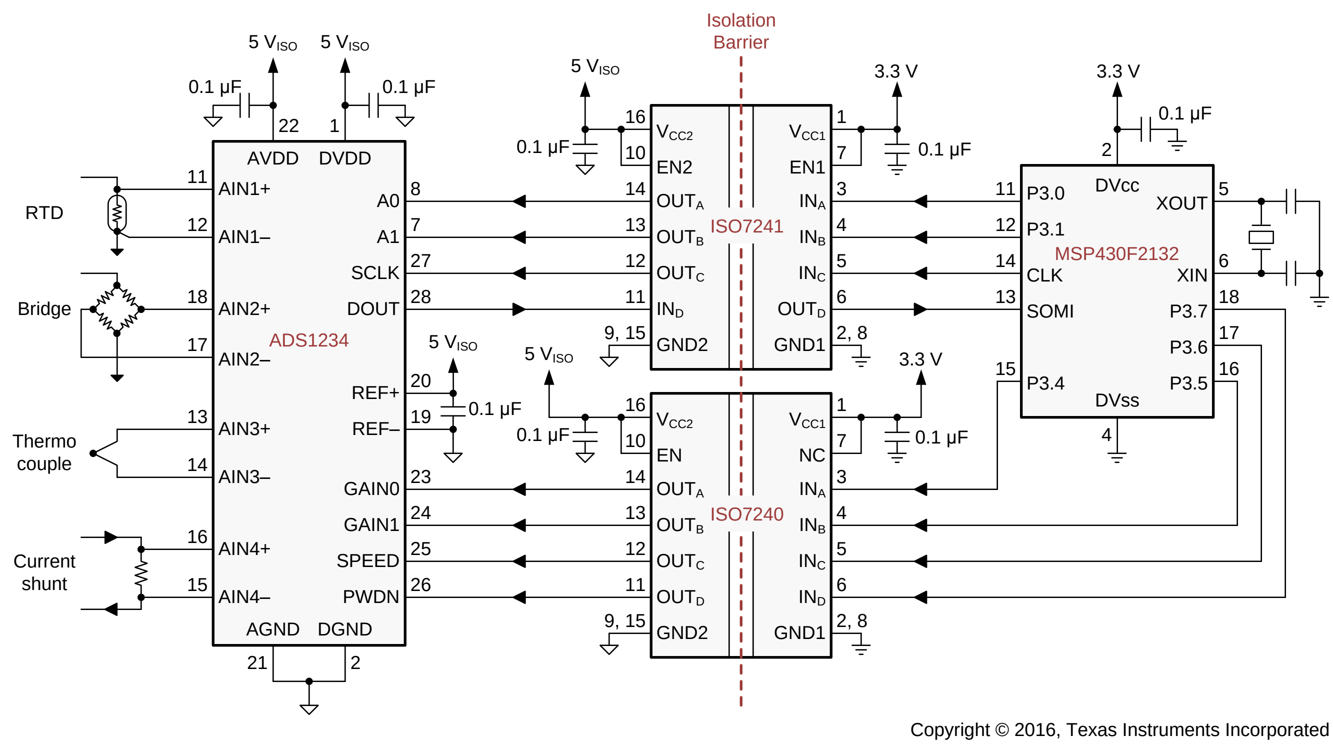

Figure 19. Isolated Data Acquisition System for Process Control

10.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x family of devices only require two external bypass capacitors to operate.

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Typical Application (continued)

10.2.1.2 Detailed Design Procedure

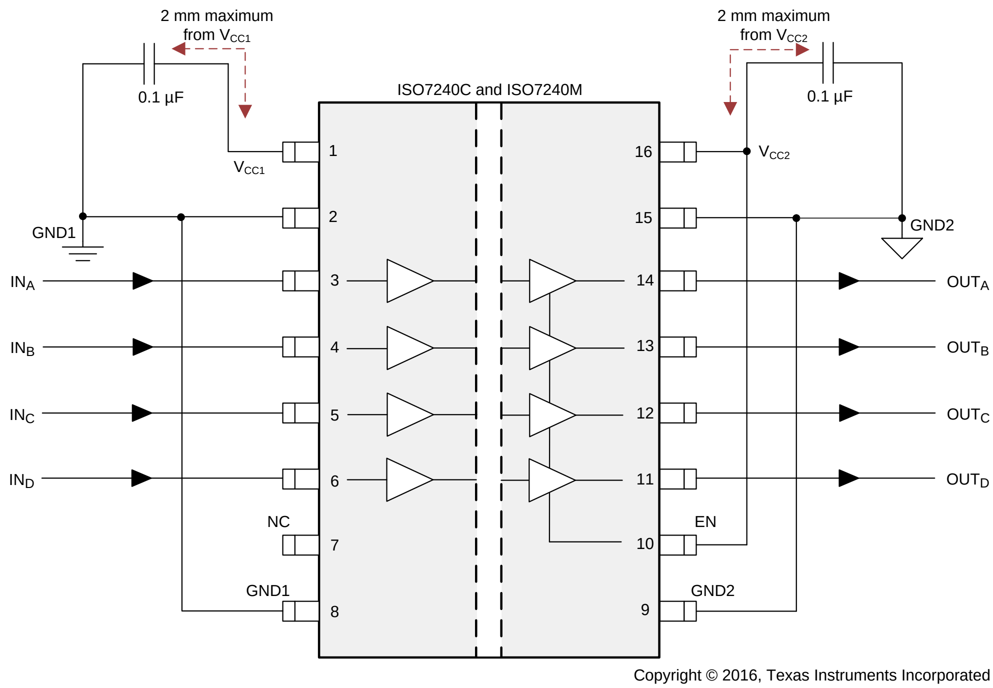

Figure 20. ISO7240x Typical Circuit Hook-Up

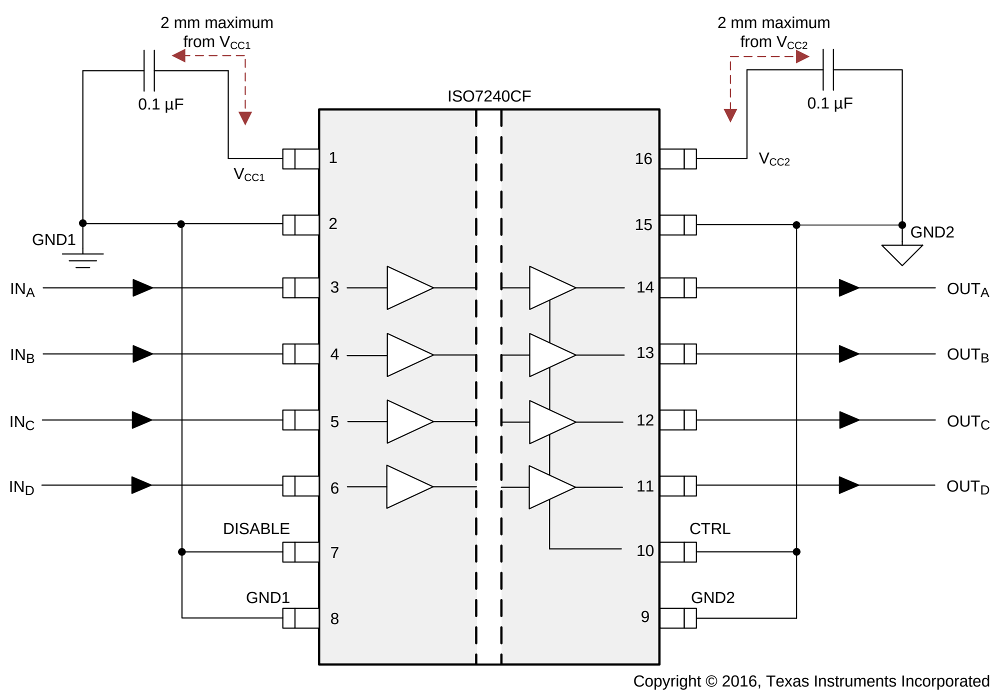

Figure 21. ISO7240CF Typical Circuit Hook-Up

Typical Application (continued)

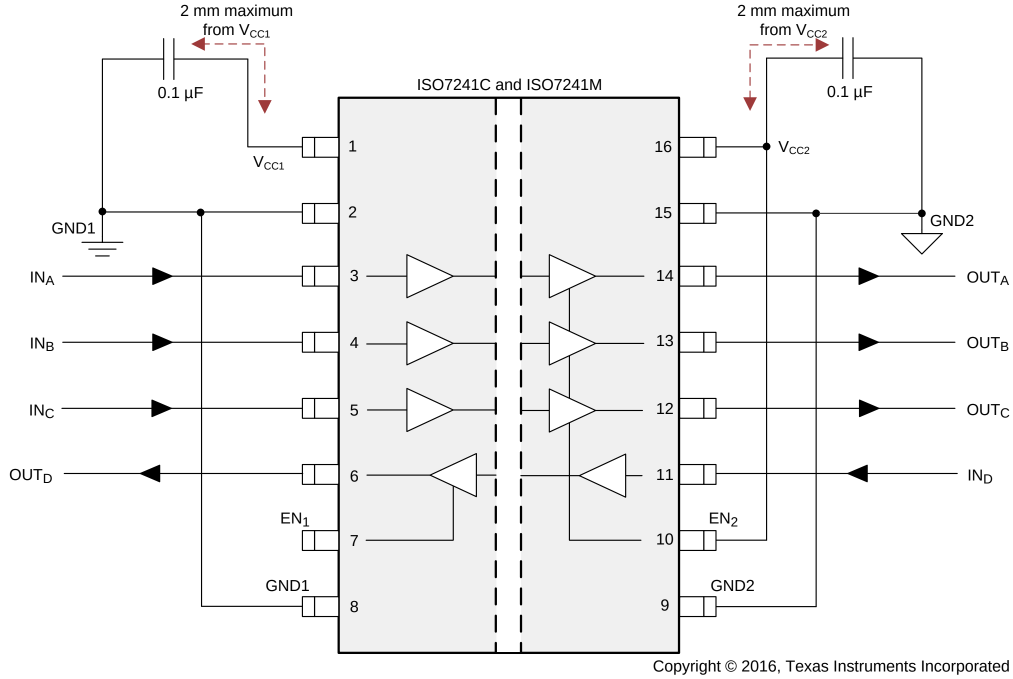

Figure 22. ISO7241x Typical Circuit Hook-Up

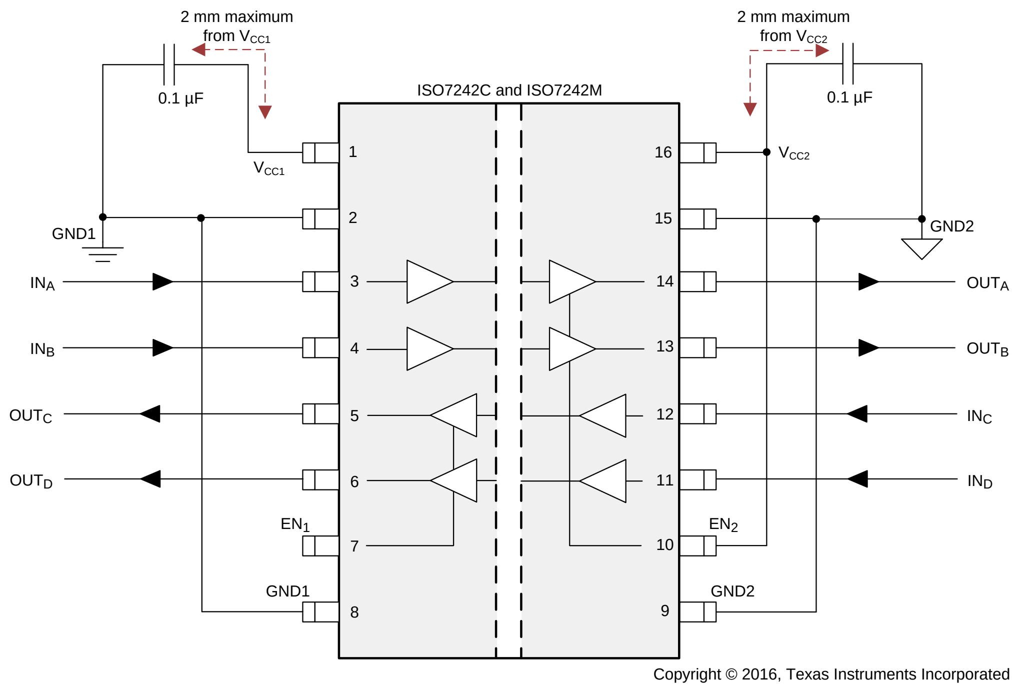

Figure 23. ISO7242x Typical Circuit Hook-Up

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Typical Application (continued)

10.2.1.3 Application Curves

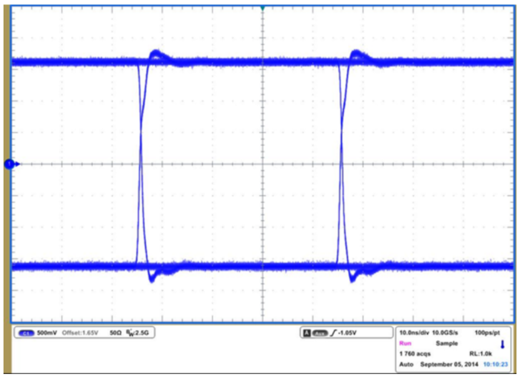

Figure 24. ISO7242M Eye Diagram at 25 Mbps, 3.3 V and 25°C

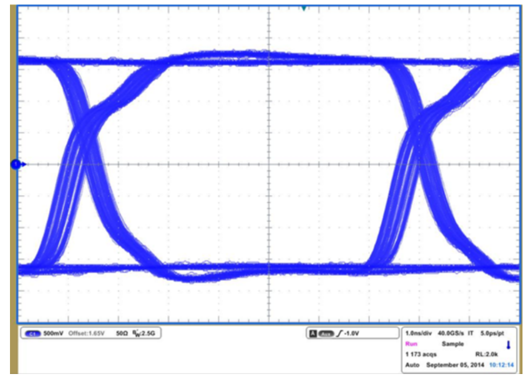

Figure 25. ISO7242M Eye Diagram at 150 Mbps, 3.3 V and 25°C

Typical Application (continued)

10.2.2 Isolated SPI Interface for an Analog Input Module with 16 Inputs

The ISO7241x family of devices and several other components from Texas Instruments can be used to create an isolated SPI interface for an input module with 16 inputs.

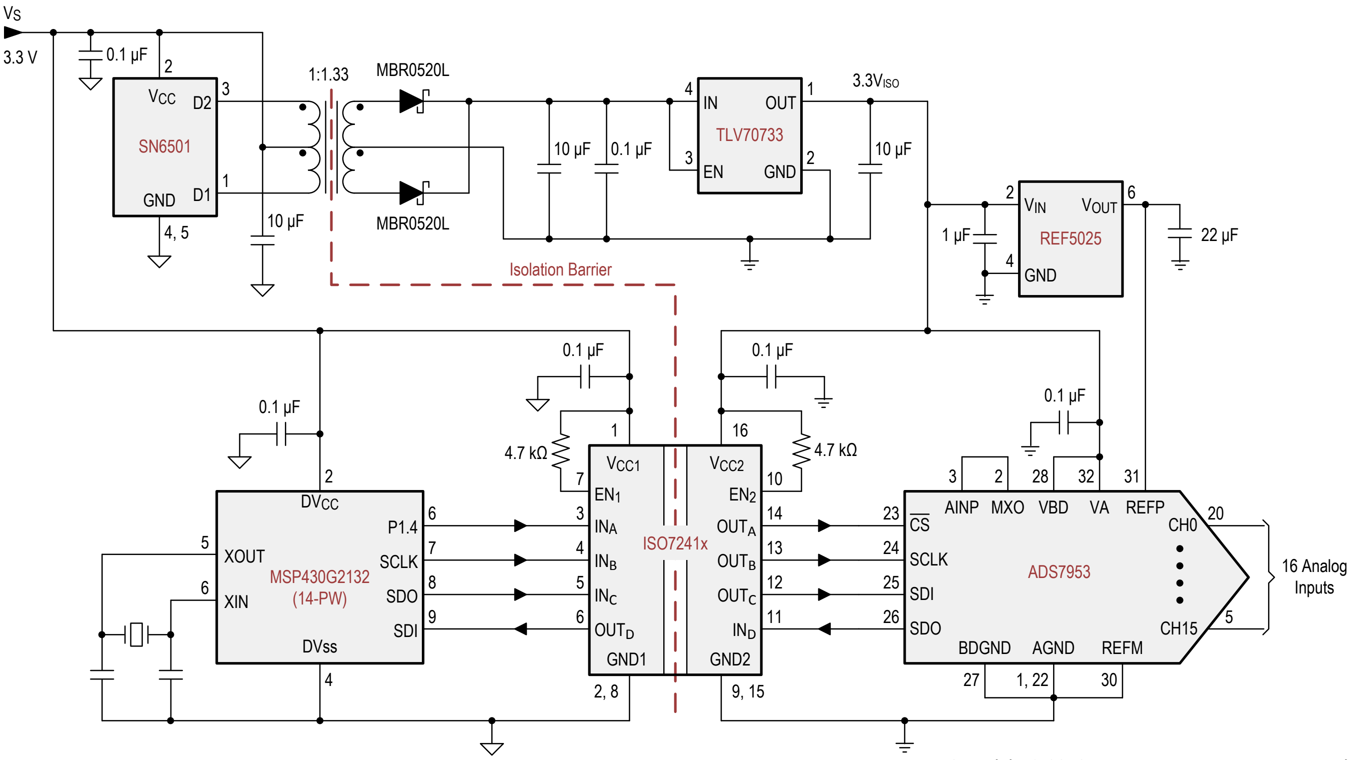

Figure 26. Isolated SPI Interface for an Analog Input Module With 16 Inputs

10.2.2.1 Design Requirements

See the *Design Requirements* in the *Isolated Data Acquisition System for Process Control* section.

10.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure* in the *Isolated Data Acquisition System for Process Control* section..

10.2.2.3 Application Curve

See the *Application Curves* in the *Isolated Data Acquisition System for Process Control* section..

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Typical Application (continued)

10.2.3 Isolated RS-232 Interface

Figure 27 shows a typical isolated RS-232 interface implementation.

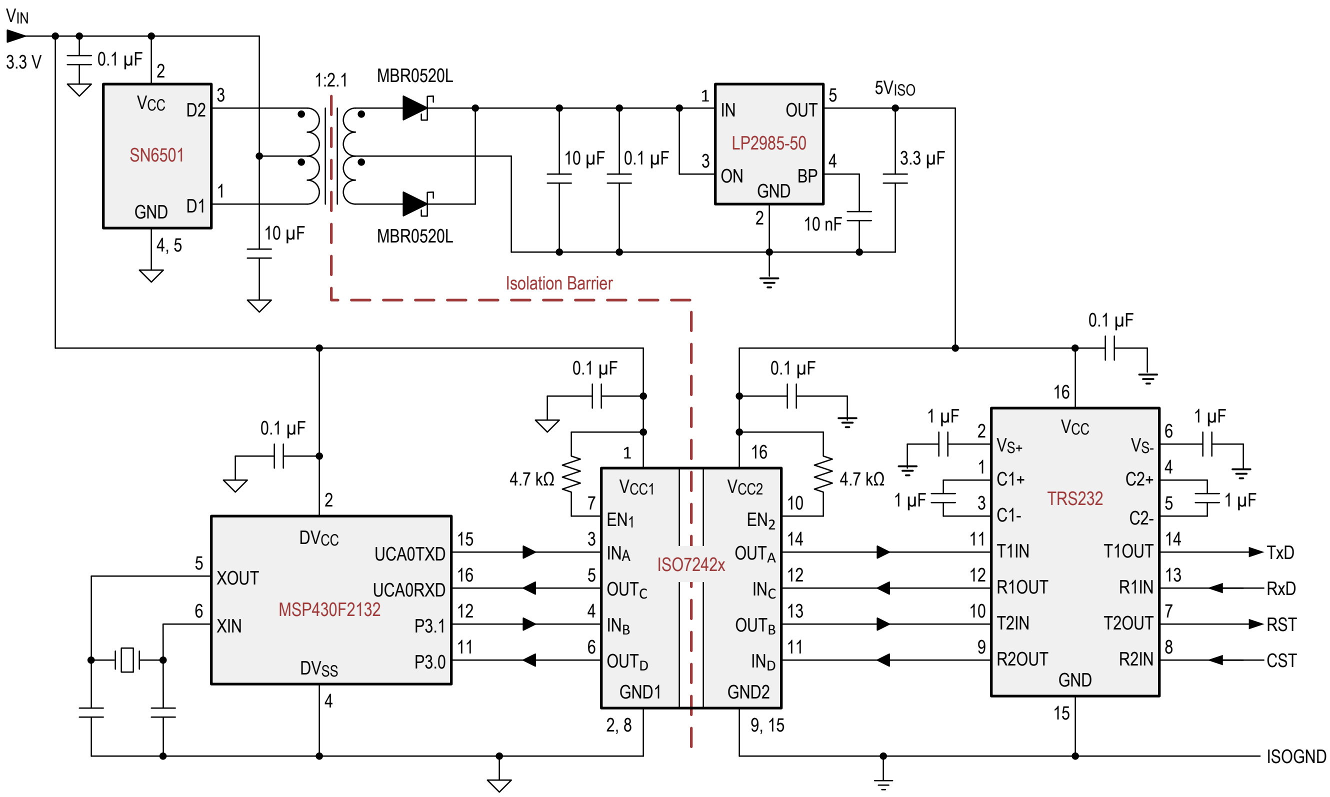

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Figure 27. Isolated RS-232 Interface

10.2.3.1 Design Requirements

See the *Design Requirements* in the *Isolated Data Acquisition System for Process Control* section.

10.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure* in the *Isolated Data Acquisition System for Process Control* section..

10.2.3.3 Application Curve

See the *Application Curves* in the *Isolated Data Acquisition System for Process Control* section..

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 28). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284).

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example

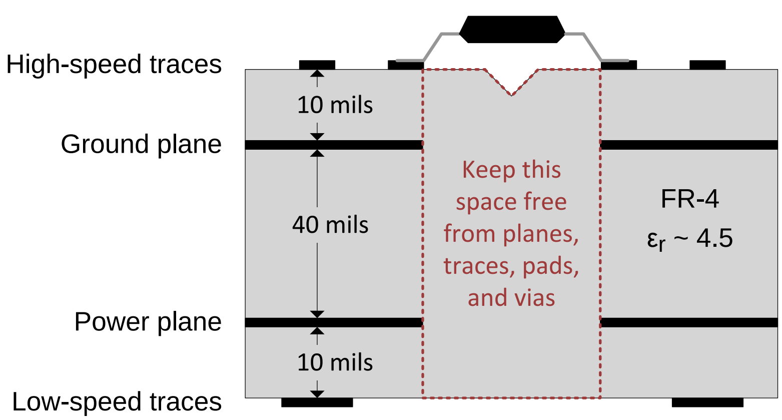

Figure 28. Recommended Layer Stack

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13 Device and Documentation Support

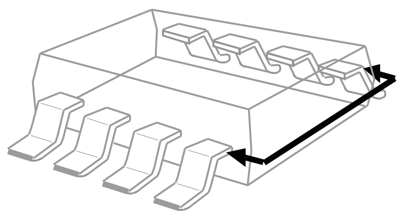
13.1 Device Support

13.1.1 Isolation Glossary

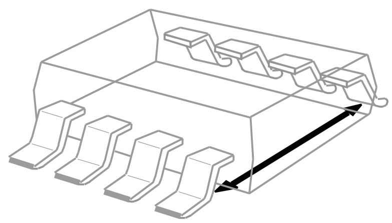
Primary Circuit A circuit that is directly connected to an external main supply for the power requirements of the device.

Secondary Circuit A circuit that has no direct connection to a primary circuit and derives power from a transformer, converter or equivalent isolation device, or from a battery.

Creepage The shortest distance between two conductive parts measured along the surface of a solid insulation. The shortest path is typically found around the end of the package body.



Clearance The shortest distance between two conductive parts measured through air.



Isolation Capacitance (C_{IO}) The total capacitance between the terminals on a first side of the isolation barrier connected together and the terminals on a second side of the isolation barrier connected together forming a two-terminal device.

Isolation Resistance (R_{IO}) The resistance between the terminals on a first side of the isolation barrier connected together and all the terminals on a second side of the isolation barrier connected together forming a two-terminal device.

Rated Isolation Voltages The maximum voltage between all input terminals (connected together) and all output terminals (connected together) respectively.

Maximum Rated Isolation Working Voltage (V_{IOWM}) An RMS or equivalent DC voltage assigned by the manufacturer, characterizing the specified long term withstand capability of the isolation.

Maximum Rated Repetitive Peak Isolation Voltage (V_{IORM}) A peak voltage assigned by the manufacturer, characterizing the specified withstand capability of isolation against repetitive peak voltages. It includes all repetitive transient voltages, but excludes all non-repetitive transient voltages.

Maximum Rated Transient Isolation Voltage (V_{IOTM}) A peak impulse voltage assigned by the manufacturer, characterizing the specified withstand capability of isolation against transient overvoltages.

Withstand Isolation Voltage (V_{ISO}) Maximum AC RMS isolation voltage for one minute.

Withstand Isolation Voltage (V_{ISO}) Maximum AC RMS isolation voltage for one minute.

Surge Isolation Voltage (V_{IOSM}) The highest instantaneous value of an isolation voltage pulse with short time duration and of specified wave shape.

Partial Discharge Localized electrical discharge which occurs in the insulation between all terminals of the first side and all terminals of the second side of the coupler.

Device Support (continued)

Comparative Tracking Index (CTI) CTI is an index used for electrical insulating materials that is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher the CTI value of the insulating material, the smaller the minimum creepage distance required.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Material Groups Materials are classified into four groups according to their CTI values. These values are determined in accordance with IEC 60112. The groups are as follows:

- Material group I: 600V ≤ CTI
- Material group II: 400V ≤ CTI < 600
- Material group II: 175V ≤ CTI < 400
- Material group II: 100V ≤ CTI < 175

13.1.1.1 Insulation

Functional insulation Insulation required for the correct operation of the equipment.

Basic insulation Insulation that provides basic protection against electric shock.

Supplementary insulation Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation Insulation comprising both basic and supplementary insulation.

Reinforced insulation A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

13.1.1.2 Pollution Degree

Pollution is any addition of foreign matter, solid, liquid, or gaseous that can result in a reduction of electric strength or surface resistivity of the insulation. There are four categories of pollution:

Pollution Degree 1 No pollution or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 Only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3 Conductive pollution occurs or dry non-conductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

13.1.1.3 Overvoltage Categories and Installation Classification

Overvoltage Categories define transient overvoltage conditions. There are four different levels as indicated in IEC 60664.

I: Signal level — Special protected equipment or parts of equipment, for example, circuit board inside a DVD player.

II: Local level — Portable equipment that is supplied from the wall outlet, for example, a DVD player

III: Distribution level — Equipment in fixed installation such as HVAC system, washers, dryers, and others.

IV: Primary supply level — Equipment for use at the origin of the installations such as overhead lines, cable systems, and others.

Lower level category is subject to smaller transients than the category above.

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- ADS1234 *24-Bit Analog-to-Digital Converter For Bridge Sensors*, SBAS350
- *ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs*, SLAS605
- *Digital Isolator Design Guide*, SLLA284
- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*, SLLA197
- *ISO72x Digital Isolator Magnetic-Field Immunity*, SLLA181
- LP2985-50
- MSP430F2132
- *MSP430G2x32, MSP430G2x02 Mixed Signal Microcontroller*, SLAS723
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*, SBOS410
- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*, SBVS153
- *TRS232*

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7240CF	Click here	Click here	Click here	Click here	Click here
ISO7240C	Click here	Click here	Click here	Click here	Click here
ISO7240M	Click here	Click here	Click here	Click here	Click here
ISO7241C	Click here	Click here	Click here	Click here	Click here
ISO7241M	Click here	Click here	Click here	Click here	Click here
ISO7242C	Click here	Click here	Click here	Click here	Click here
ISO7242M	Click here	Click here	Click here	Click here	Click here

13.4 Trademarks

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240C	Samples
ISO7240CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240C	Samples
ISO7240CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240C	Samples
ISO7240CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240C	Samples
ISO7240CFDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CF	Samples
ISO7240CFDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CF	Samples
ISO7240CFDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CF	Samples
ISO7240MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240M	Samples
ISO7240MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240M	Samples
ISO7240MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240M	Samples
ISO7240MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240M	Samples
ISO7241CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241C	Samples
ISO7241CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241C	Samples
ISO7241CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241C	Samples
ISO7241CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241C	Samples
ISO7241MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241M	Samples
ISO7241MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7241MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241M	Samples
ISO7241MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241M	Samples
ISO7242CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242C	Samples
ISO7242CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242C	Samples
ISO7242CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242C	Samples
ISO7242MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242M	Samples
ISO7242MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242M	Samples
ISO7242MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242M	Samples
ISO7242MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :

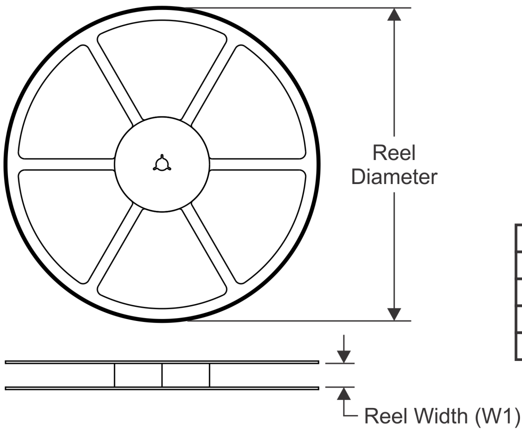
- Automotive: ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1

NOTE: Qualified Version Definitions:

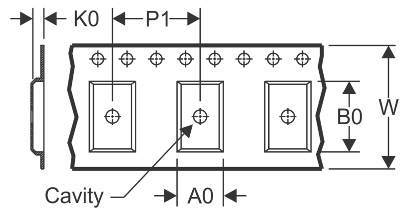
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

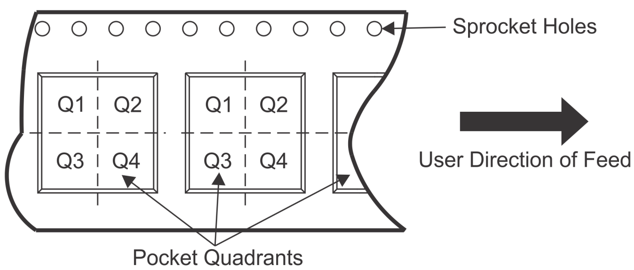


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

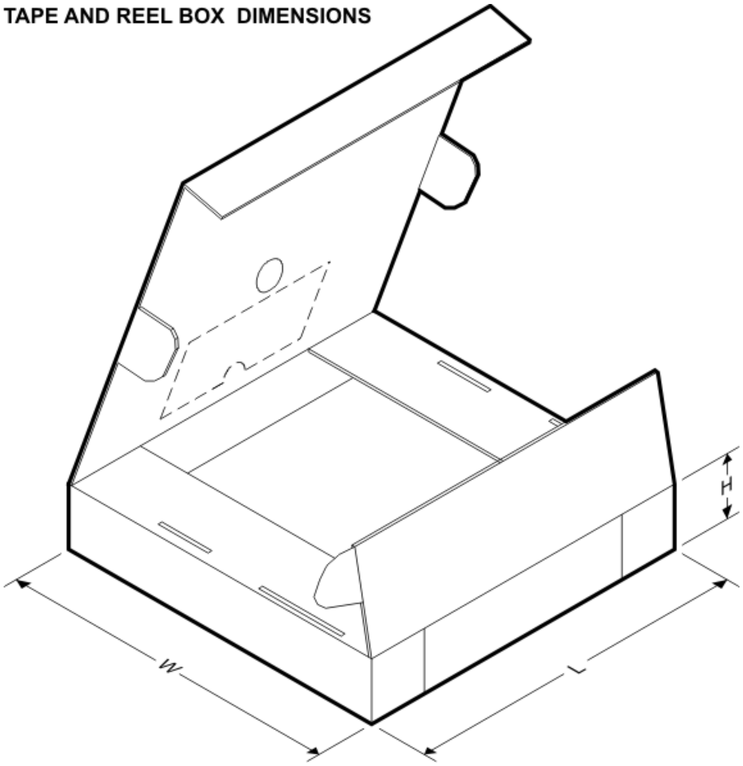
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240CFDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7240CFDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7240MDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7241CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7241MDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7242CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7242MDWR	SOIC	DW	16	2000	367.0	367.0	38.0

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