



P-Channel NexFET™ Power MOSFET

 Check for Samples: **CSD23201W10**

FEATURES

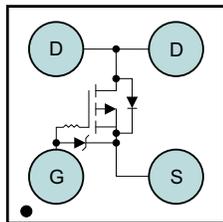
- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate ESD Protection – 3kV
- RoHS Compliant
- Halogen Free

APPLICATIONS

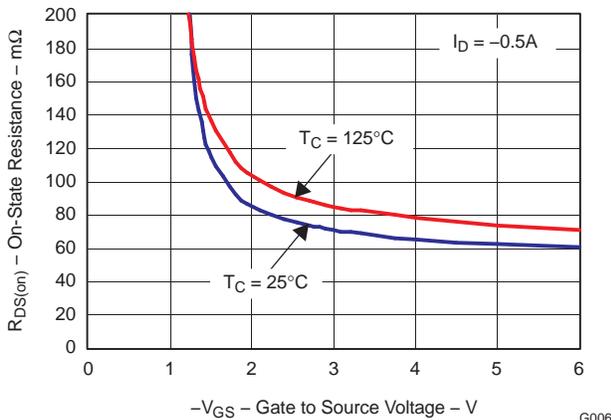
- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

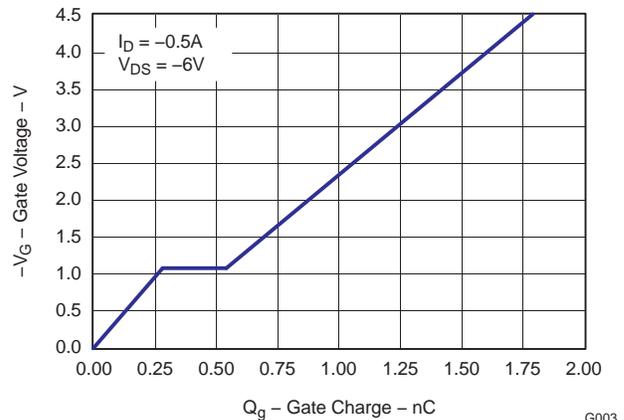
The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View


P0097-01

R_{DS(on)} vs V_{GS}


G006

Gate Charge


G003

PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	-12	V
Q _g	Gate Charge Total (4.5V)	1.8	nC
Q _{gd}	Gate Charge Gate to Drain	0.26	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -1.5V	110 mΩ
		V _{GS} = -2.5V	77 mΩ
		V _{GS} = -4.5V	66 mΩ
V _{GS(th)}	Threshold Voltage	-0.6	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD23201W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	-12	V
V _{GS}	Gate to Source Voltage	-6	V
I _D	Continuous Drain Current, T _C = 25°C ⁽¹⁾	-2.2	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	-8.8	A
I _G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current	-7	A
P _D	Power Dissipation ⁽¹⁾	1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) R_{θJA} = 100°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

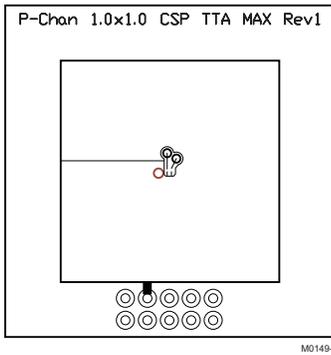
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = -250μA	-12			V
BV _{GSS}	Gate to Source Voltage;	V _{DS} = 0V, I _G = -250μA	-6.1		-7.2	V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = -9.6V			-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = -6V			-100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.6	-1.0	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -1.5V, I _D = -0.5A		110	138	mΩ
		V _{GS} = -2.5V, I _D = -0.5A		77	96	mΩ
		V _{GS} = -4.5V, I _D = -0.5A		66	82	mΩ
g _{fs}	Transconductance	V _{DS} = -6.0V, I _D = -0.5A		9		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = -6.0V, f = 1MHz		250	325	pF
C _{OSS}	Output Capacitance			125	155	pF
C _{RSS}	Reverse Transfer Capacitance			32	42	pF
Q _g	Gate Charge Total (-4.5V)			1.8	2.4	nC
Q _{gd}	Gate Charge Gate to Drain	V _{DS} = -6.0V, I _D = -0.5A		0.26		nC
Q _{gs}	Gate Charge Gate to Source			0.28		nC
Q _{g(th)}	Gate Charge at V _{th}			0.11		nC
Q _{OSS}	Output Charge	V _{DS} = -6.0V, V _{GS} = 0V		1.7		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = -6.0V, V _{GS} = -2.5V, I _D = -0.5A R _G = 20Ω		24		ns
t _r	Rise Time			19		ns
t _{d(off)}	Turn Off Delay Time			68		ns
t _f	Fall Time			29		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _S = -0.5A, V _{GS} = 0V	-0.77		-1.0	V
Q _{rr}	Reverse Recovery Charge	V _{dd} = -4.0V, I _F = -0.5A, di/dt = 100A/μs		2		nC
t _{rr}	Reverse Recovery Time	V _{dd} = -4.0V, I _F = -0.5A, di/dt = 100A/μs		9.5		ns

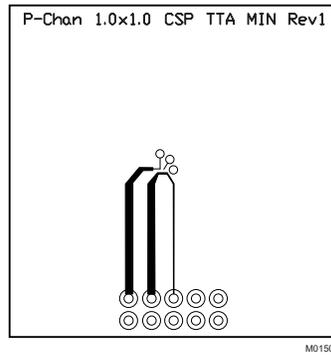
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Ambient (Minimum Cu area)			245	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient (1 in ² Cu area)			125	°C/W



Max $R_{\theta JA} = 125^{\circ}\text{C}/\text{W}$
when mounted on
1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 245^{\circ}\text{C}/\text{W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

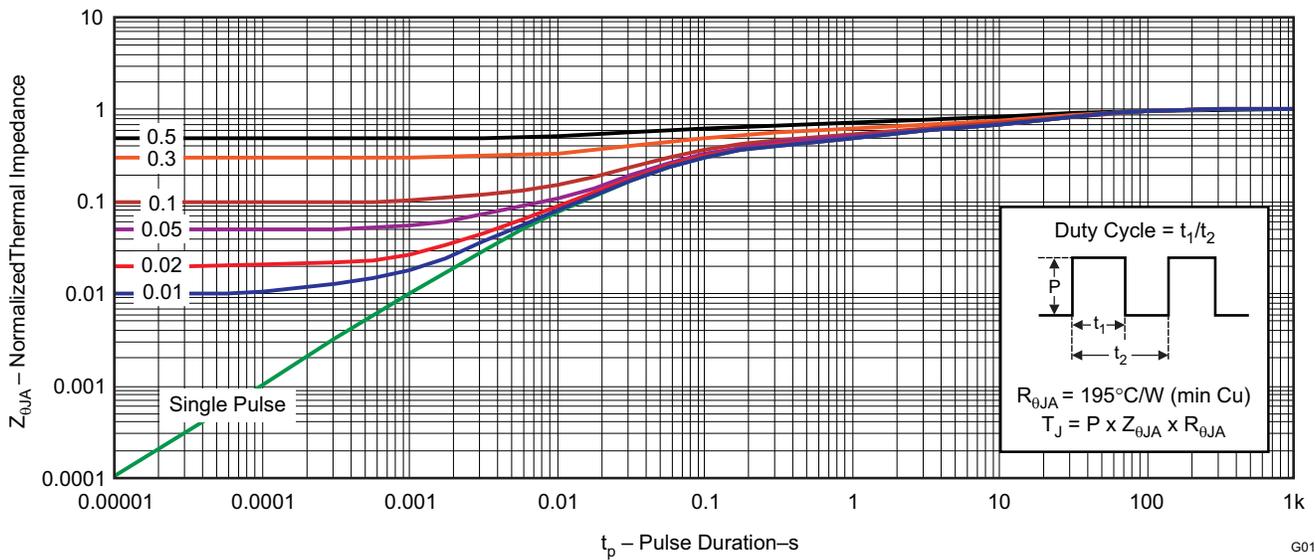


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

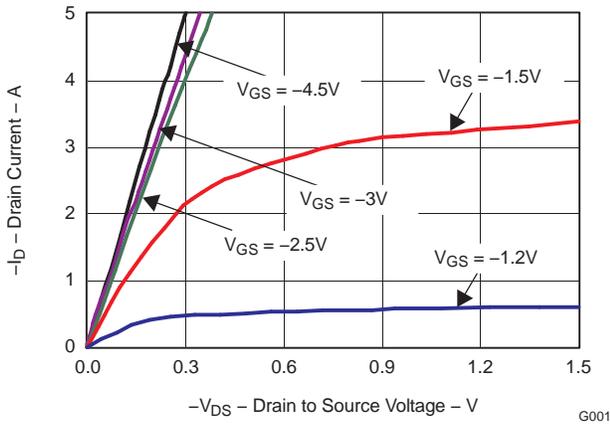


Figure 2. Saturation Characteristics

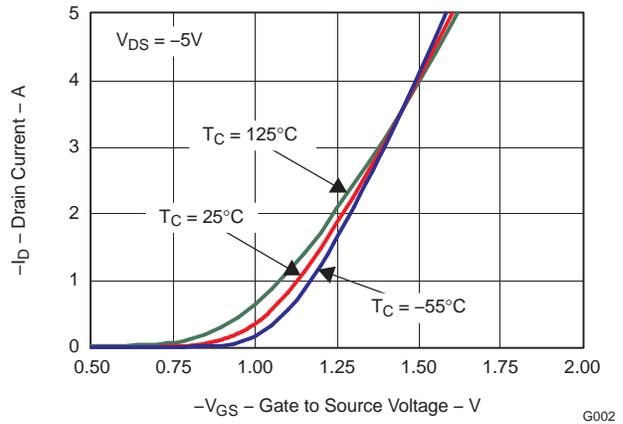


Figure 3. Transfer Characteristics

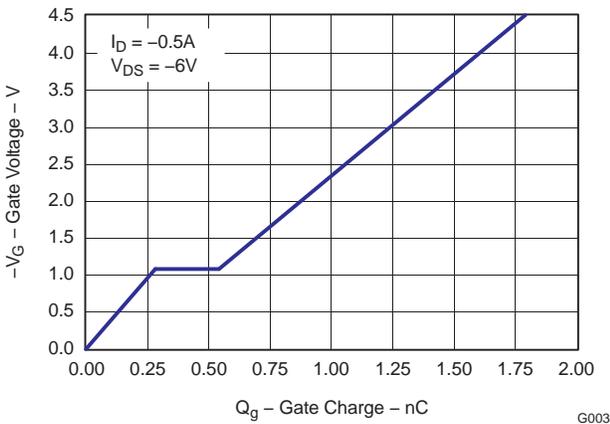


Figure 4. Gate Charge

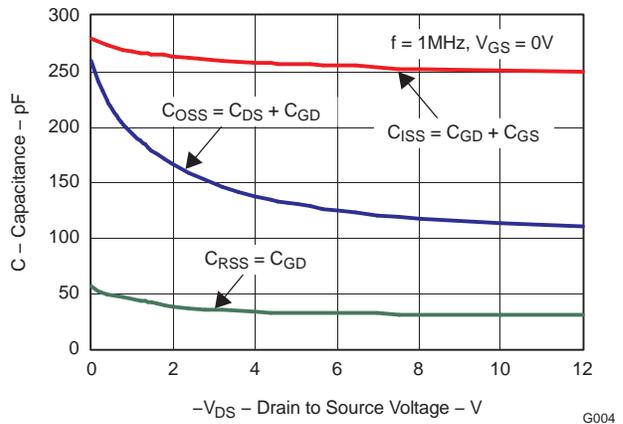


Figure 5. Capacitance

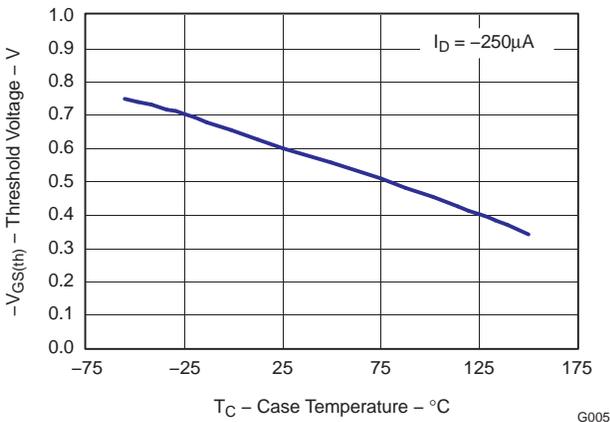


Figure 6. Threshold Voltage vs. Temperature

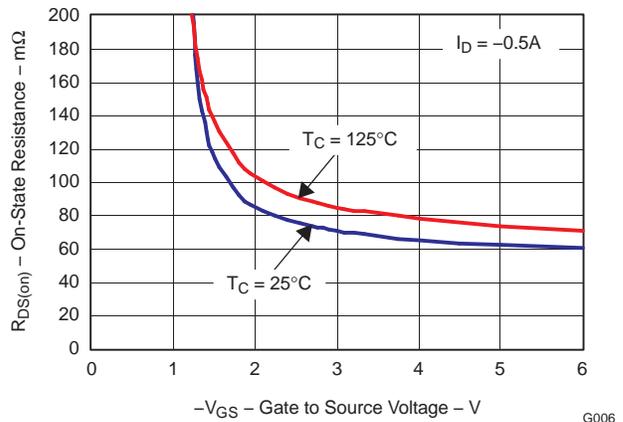


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

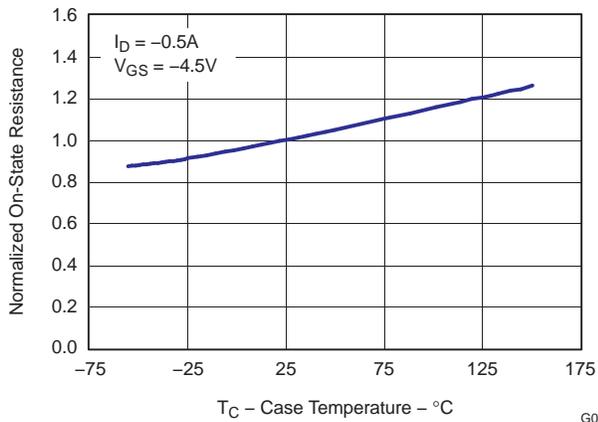


Figure 8. On Resistance vs. Temperature

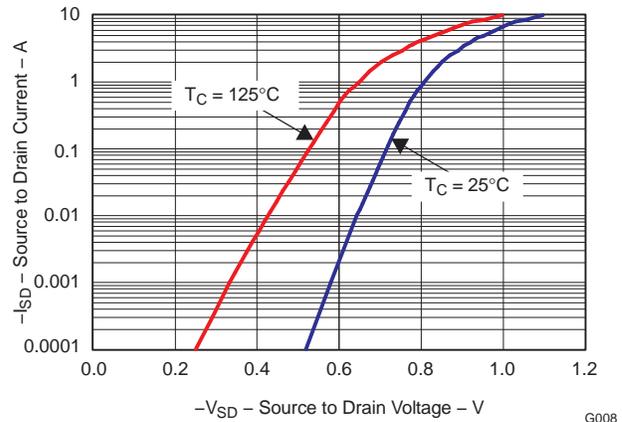


Figure 9. Typical Diode Forward Voltage

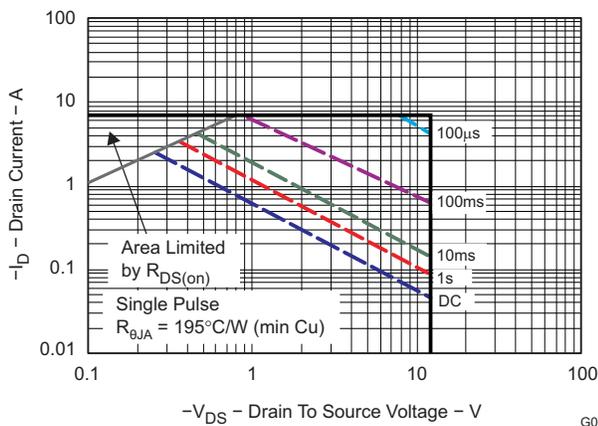


Figure 10. Maximum Safe Operating Area

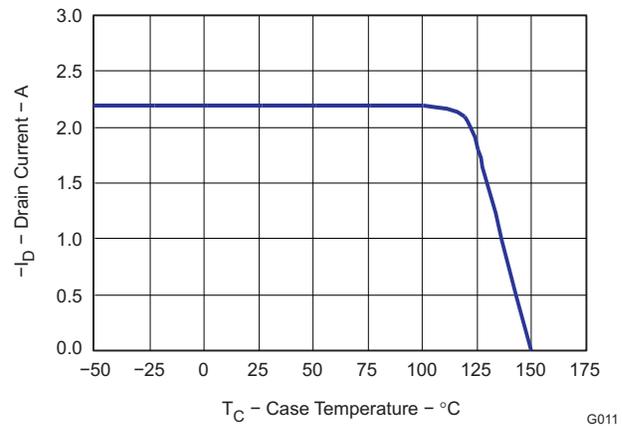
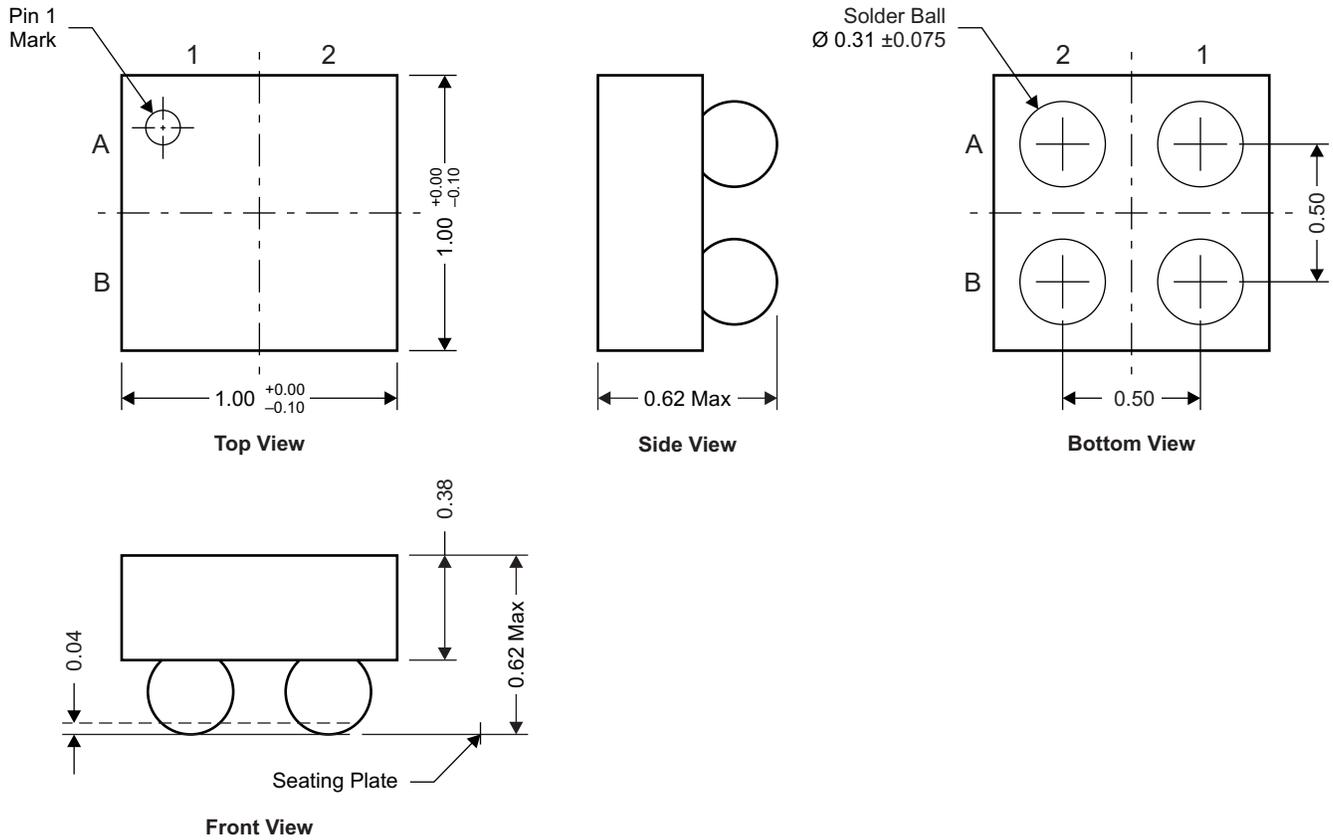


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD23201W10 Package Dimensions



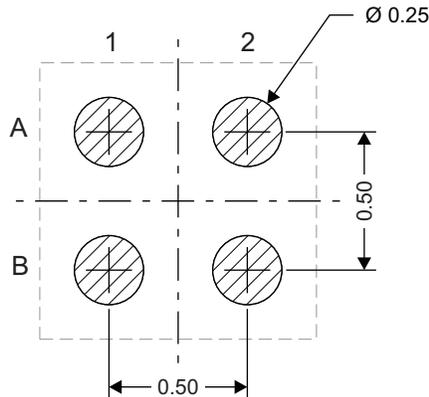
M0151-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

POSITION	DESIGNATION
B1	Source
A1	Gate
A2, B2	Drain

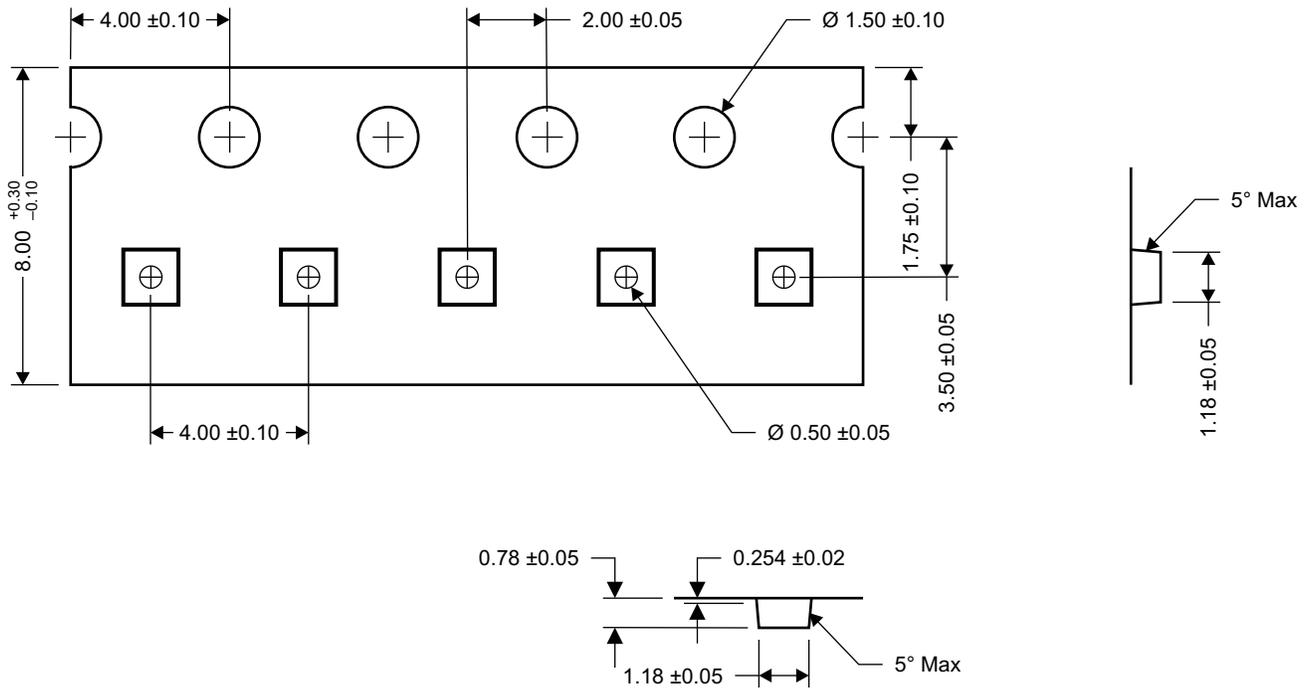
Land Pattern Recommendation



M0152-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0153-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
Deleted the Package Marking Information section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23201W10	OBSOLETE	DSBGA	YZB	4		TBD	Call TI	Call TI	-55 to 150		
HPA00788W10	OBSOLETE	DSBGA	YZB	4		TBD	Call TI	Call TI	-55 to 150		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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