

N-Channel NexFET™ Power MOSFET

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5mm x 6mm Plastic Package

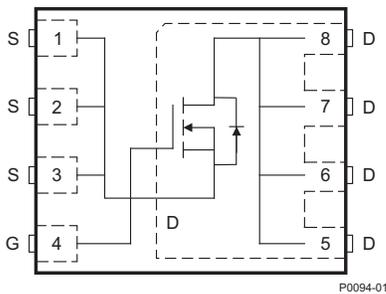
APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	21	nC
Q_{gd}	Gate Charge Gate to Drain	5.2	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	1.8 mΩ
		$V_{GS} = 10V$	1.3 mΩ
$V_{GS(th)}$	Threshold Voltage	1.5	V

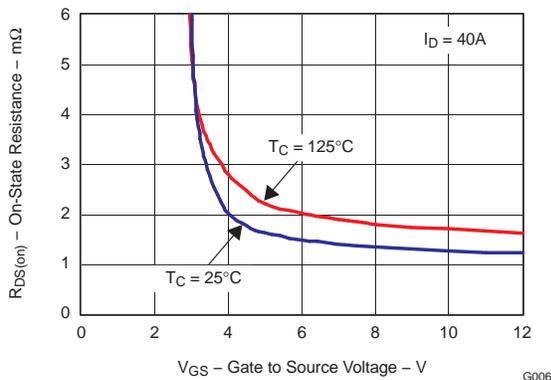
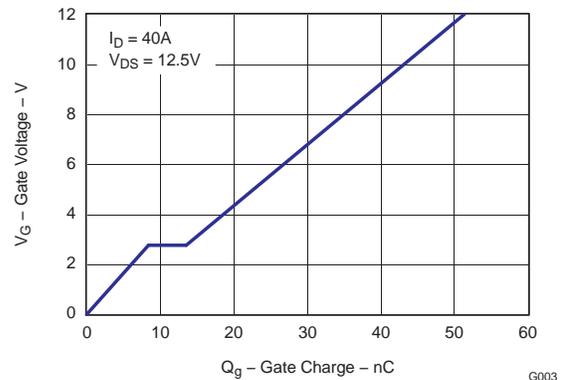
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16401Q5	SON 5 x 6 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / -12	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	38	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	240	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 100A, L = 0.1mH, R_G = 25\Omega$	500	mJ

- (1) $R_{\theta JA} = 40^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
 (2) Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(ON)}$ vs V_{GS}

Gate Charge


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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	25			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +16/-12V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.5	1.9	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 40A		1.8	2.3	mΩ
		V _{GS} = 10V, I _D = 40A		1.3	1.6	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 40A		168		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		3150	4100	pF
C _{OSS}	Output Capacitance			2530	3300	pF
C _{RSS}	Reverse Transfer Capacitance			175	230	pF
R _g	Series Gate Resistance			1.2	2.4	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _D = 40A		21	29	nC
Q _{gd}	Gate Charge Gate to Drain			5.2		nC
Q _{gs}	Gate Charge Gate to Source			8.3		nC
Q _{g(th)}	Gate Charge at V _{th}			4.8		nC
Q _{OSS}	Output Charge	V _{DS} = 15V, V _{GS} = 0V		55		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _D = 40A R _G = 2Ω		16.6		ns
t _r	Rise Time			30		ns
t _{d(off)}	Turn Off Delay Time			20		ns
t _f	Fall Time			12.7		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _S = 40A, V _{GS} = 0V		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 15V, I _F = 40A, di/dt = 300A/μs		72		nC
t _{rr}	Reverse Recovery Time	V _{DD} = 15V, I _F = 40A, di/dt = 300A/μs		45		ns

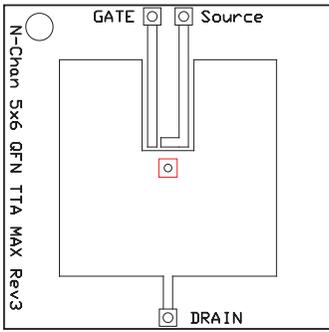
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.1	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	°C/W

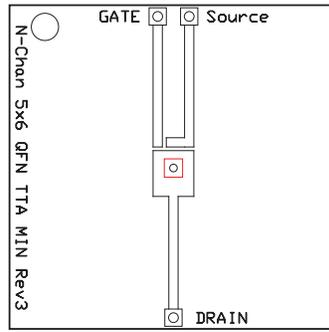
(1) R_{θJC} is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in .060 inch thick FR4 board. R_{θJC} is specified by design while R_{θJA} is determined by the user's board design.

(2) Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.



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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.

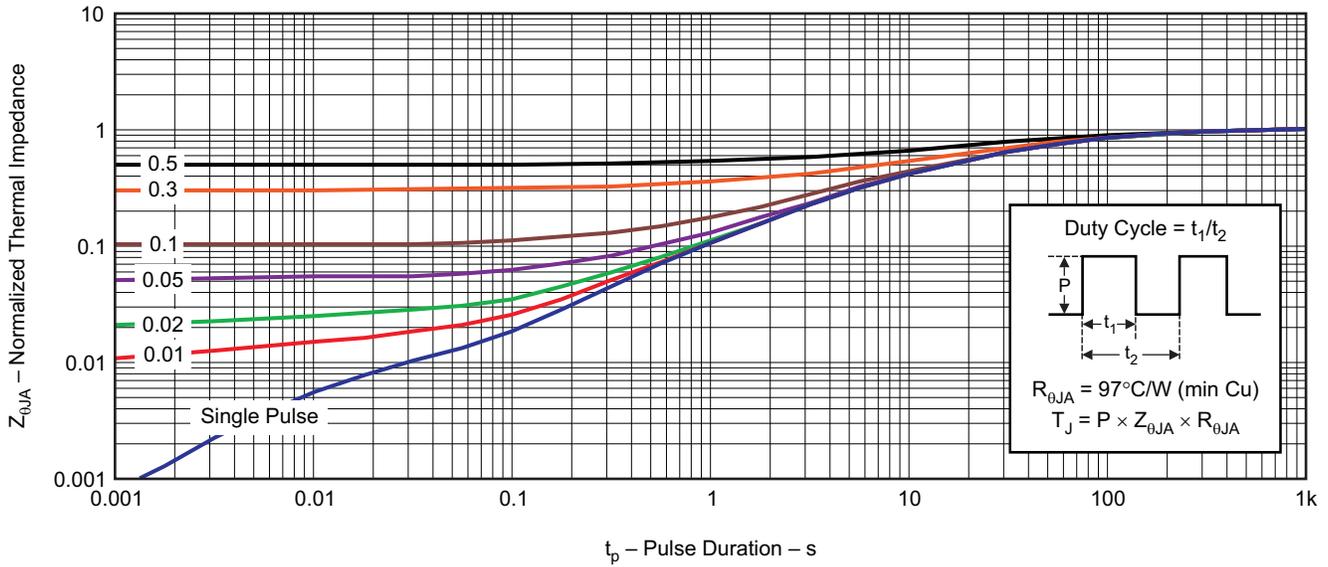


M0137-02

Max $R_{\theta JA} = 121^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

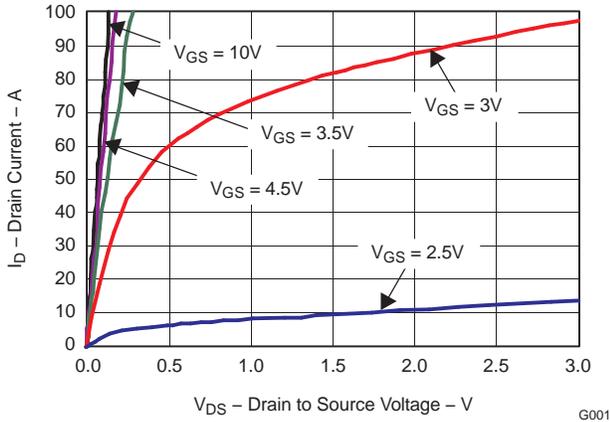


Figure 2. Saturation Characteristics

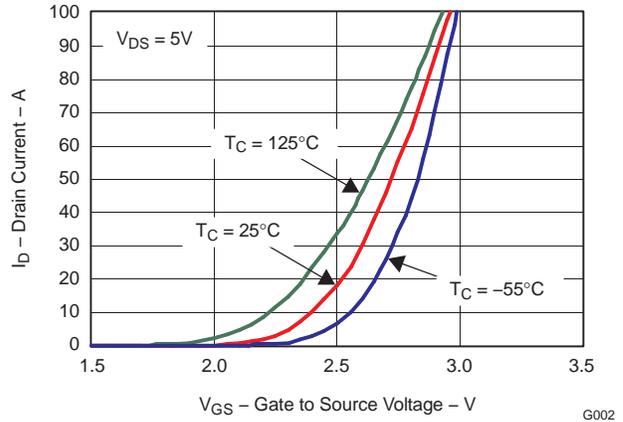


Figure 3. Transfer Characteristics

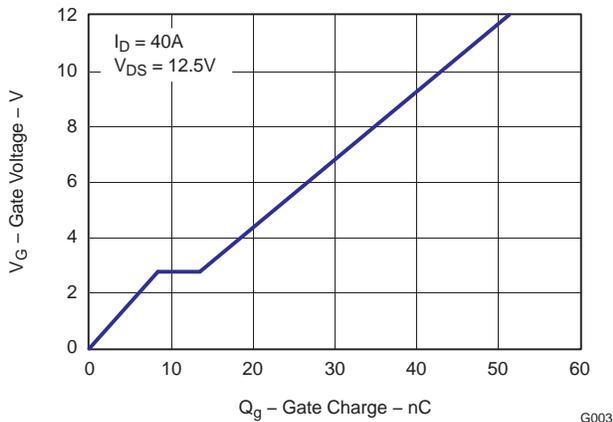


Figure 4. Gate Charge

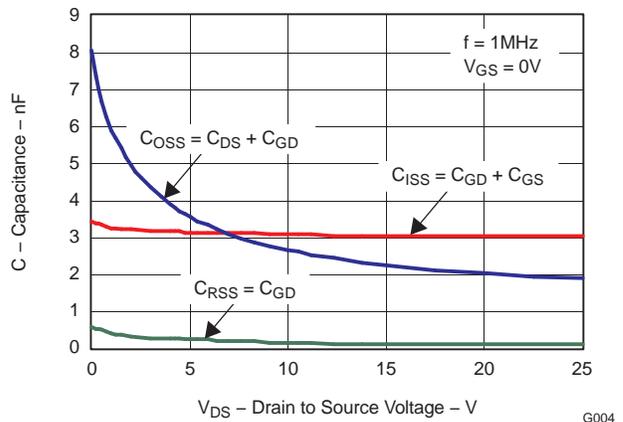


Figure 5. Capacitance

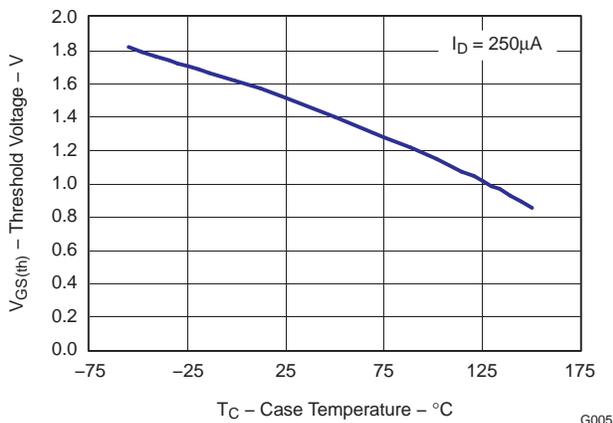


Figure 6. Threshold Voltage vs. Temperature

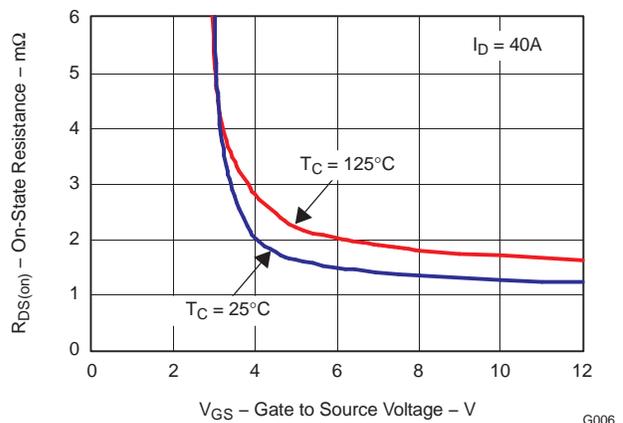


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

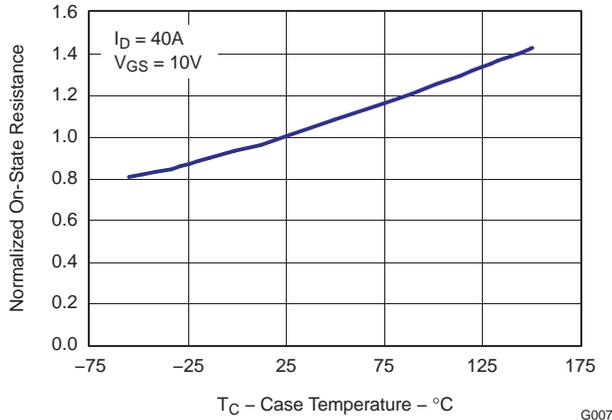


Figure 8. On Resistance vs. Temperature

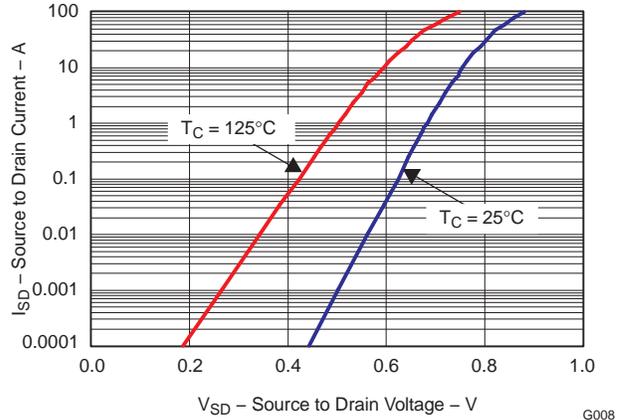


Figure 9. Typical Diode Forward Voltage

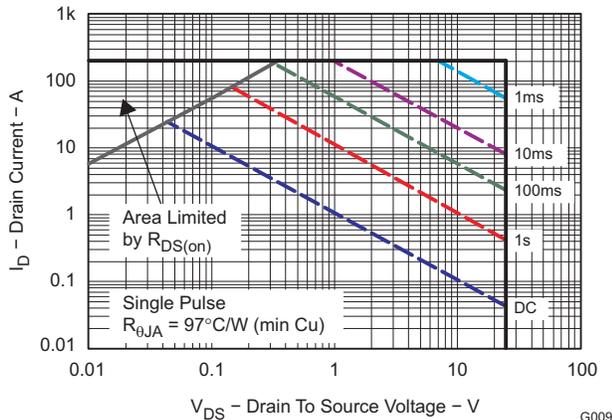


Figure 10. Maximum Safe Operating Area

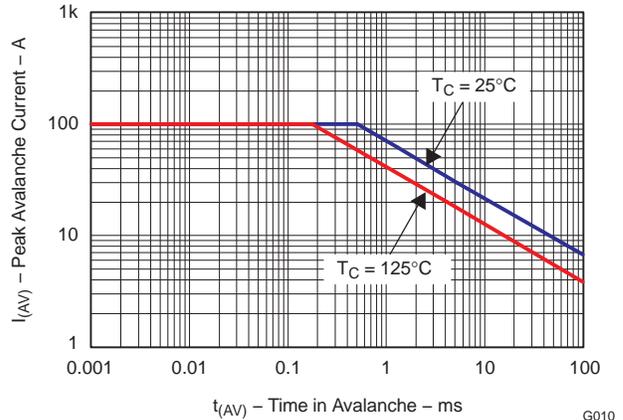


Figure 11. Single Pulse Unclamped Inductive Switching

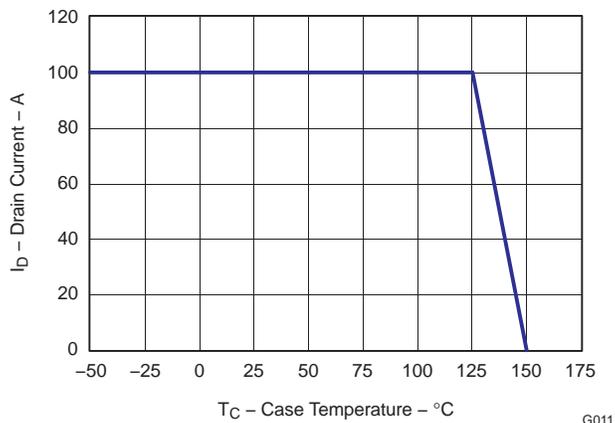
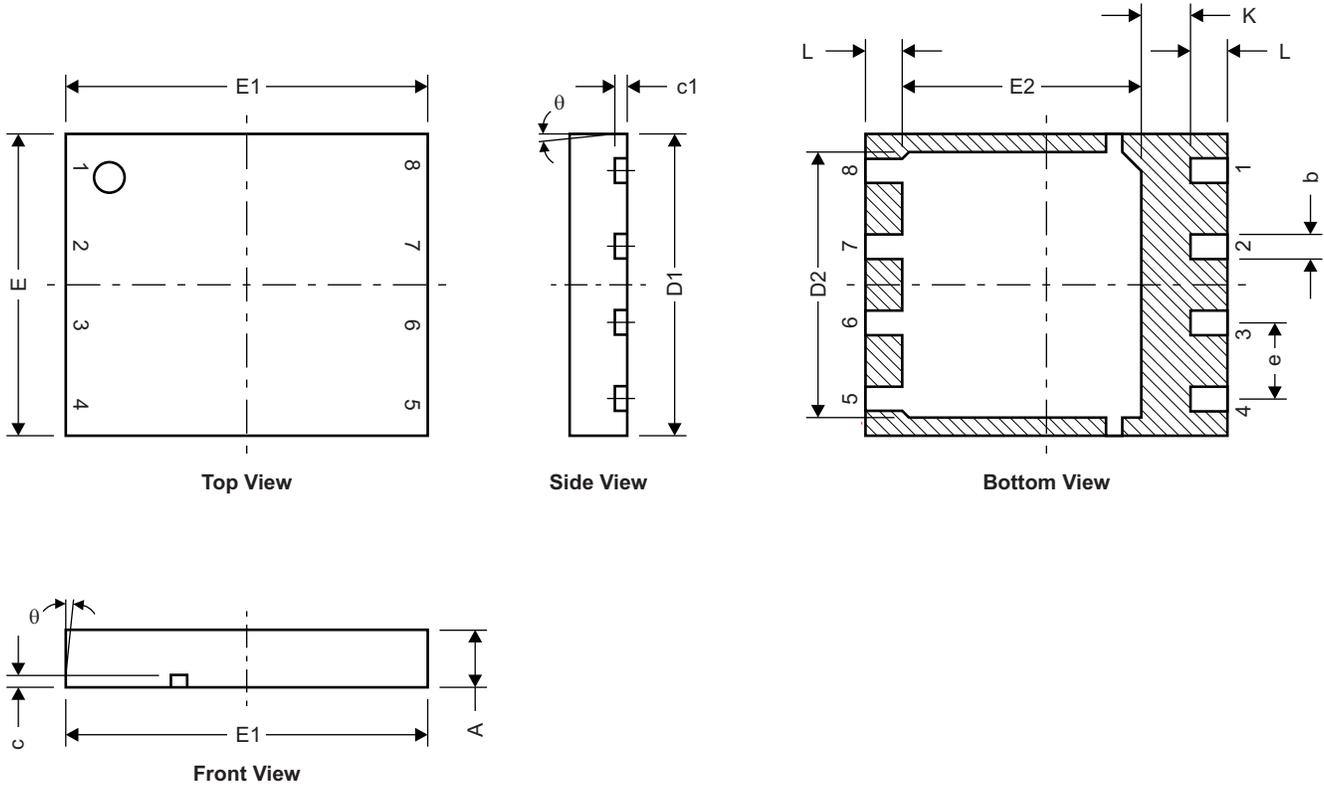


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5 Package Dimensions



M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			

Package Marking Information

Location

1st Line

CSD = Fixed Characters

NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year

WW = 2-digit Work Week

C = Country of Origin

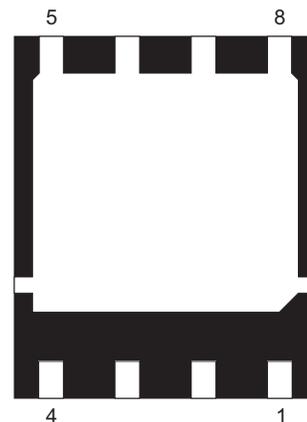
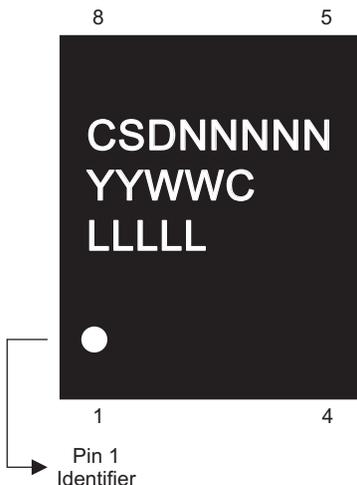
> Philippines = P

> Taiwan = T

> China = C

3rd Line

LLLL = Last 5 digits of the Wafer Lot #



M0141-01

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD16401Q5	ACTIVE	SON	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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