SONY

AC-DC Controller

CXA3811M

Description

The CXA3811M has optimum configuration to realize various power supply circuits easily and compactly by including Power-factor correction, resonant controller and various protection function in one package. (Applications: Power supply circuit, etc.)

Features

- ◆ Power-factor correction
  - Critical conduction mode, interleave PFC control
  - Supports W/W input
  - Start timer
  - Maximum frequency limit (During overcurrent detection)
  - Continuous overcurrent detection protection function
- ◆ Resonant controller
  - Timer-latch over current protection
  - Soft start function
  - Adjustment minimum frequency limit
  - Pulse over current load detection
- ◆ Common
  - Adjacent 2-pin short protection
  - Various protection functions including overvoltage and overcurrent
  - AC off detection
  - PFC-OK signal output

Structure

BiCMOS silicon monolithic IC

Package

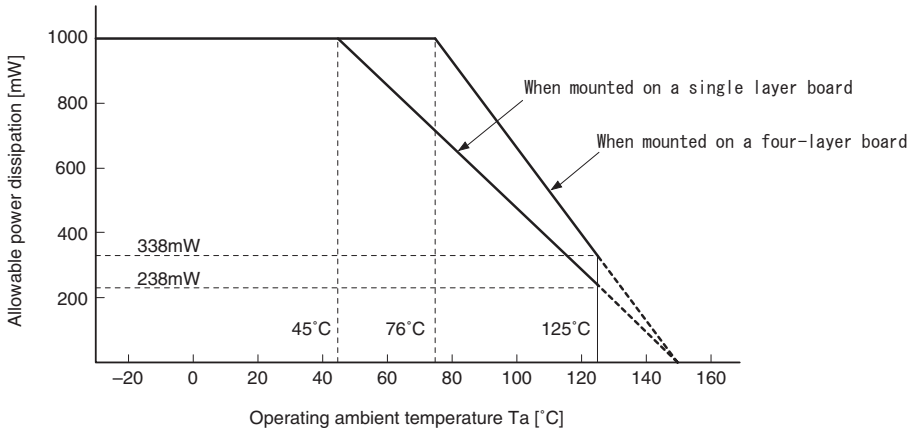
28-pin SOP

E10631A0Z

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Maximum supply voltage	VCC	24.0	V	VCC
Pin voltage which operates with VCC as power supply	VCCIN	–0.3 to VCC + 0.3	V	AC_DETIN, AC_DETOUT, AC_VRMS, B_OK, MODE1, MODE2
Driver output pin voltage	VOUT	–0.3 to VCC + 0.3	V	PFC_OUT1, PFC_OUT2, RM_OUTP, RM_OUTN
Power supply pin voltage for internal circuit	VREF	–0.3 to +7.0	V	VREF
Pin voltage which operates with VREF as power supply	VREFIN	–0.3 to +7.0	V	PFC_OVP, PFC_CS1, PFC_CS2, PFC_VAO, PFC_TONMAX, PFC_VSENSE, RM_OFFADJ, RM_RT, RM_SS, RM_CS1, RM_CS2, RM_FMIN
ZCD current	Izcd	±7	mA	PFC_ZCD1, PFC_ZCD2
Allowable power dissipation	P_D	*1	mW	(See the thermal derating curve.)
Operating ambient temperature range	Topt	–30 to +125	˚C	
Junction temperature	Tjmax	+150	˚C	
Storage temperature	Tstg	–55 to +150	˚C	

*1 Allowable power dissipation reduction characteristics

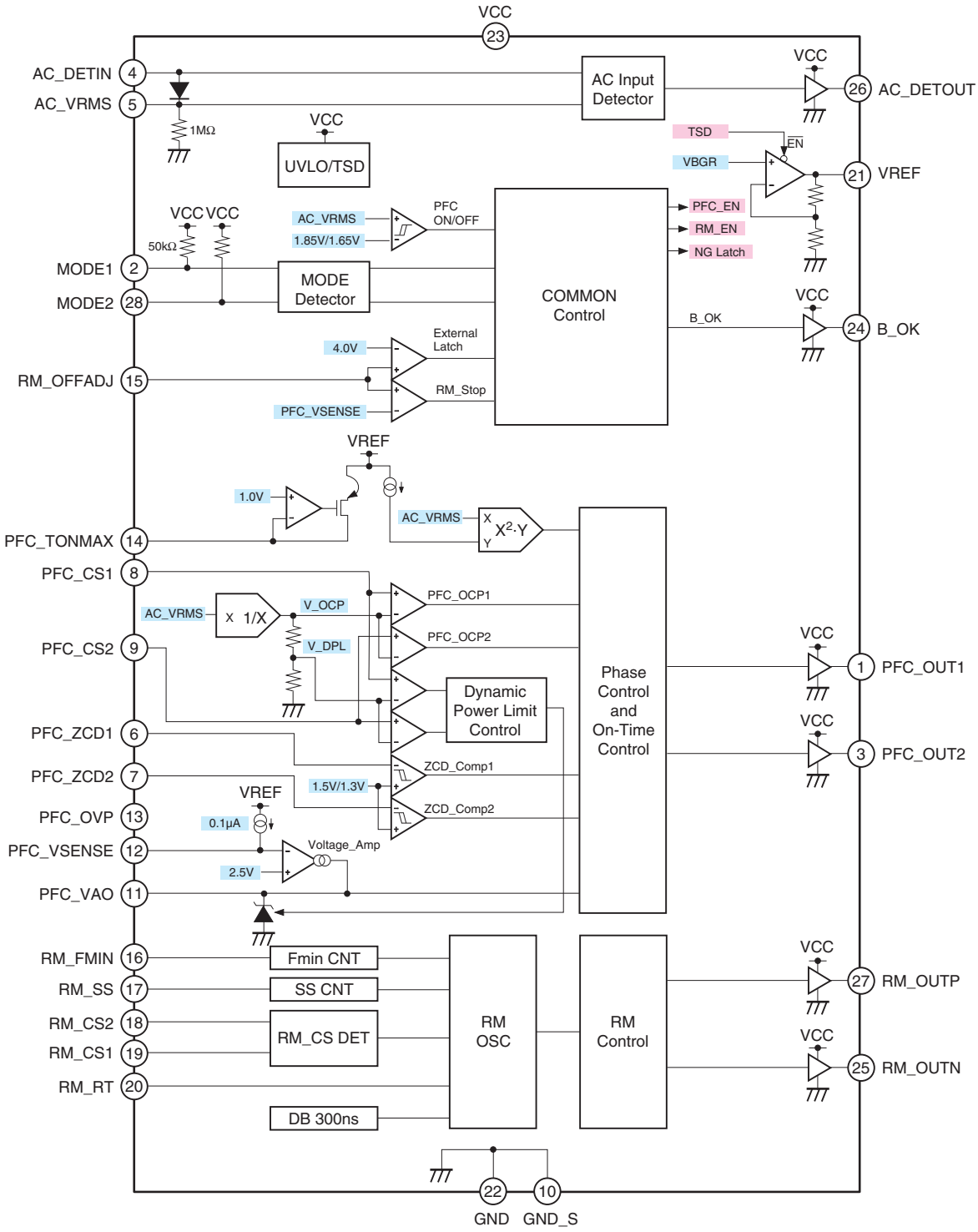


Glass fabric base epoxy board 76mm × 114mm t = 1.6mm

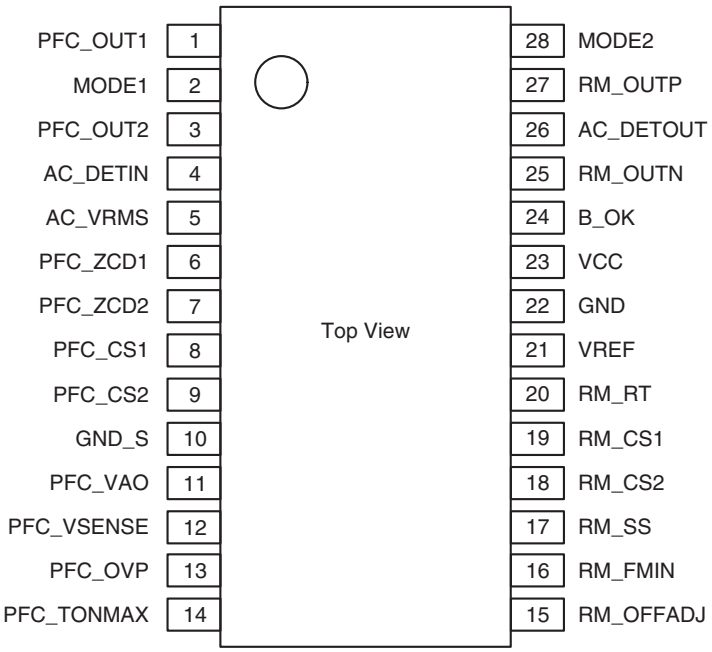
Recommended Operating Conditions

Item	Symbol	Rating	Unit	Remarks
Supply voltage . (VCC system)	VCC	12.0 to 18.0	V	
Operating ambient temperature range	Topt	–25 to +85	˚C	
Junction temperature	Tj	–25 to +125	˚C	

Block Diagram



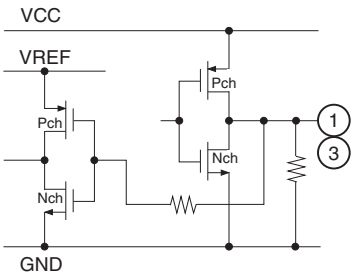
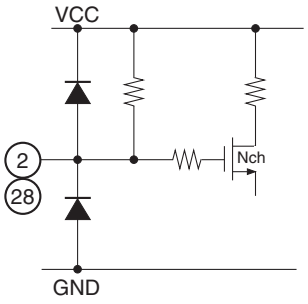
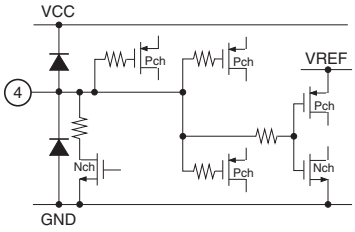
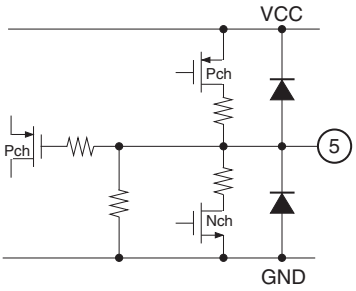
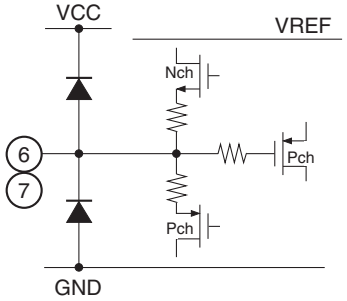
Pin Configuration

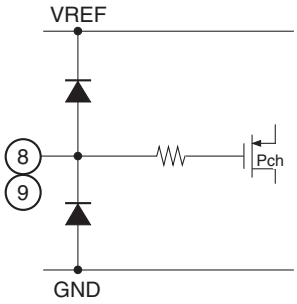
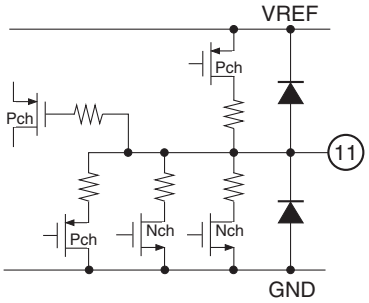
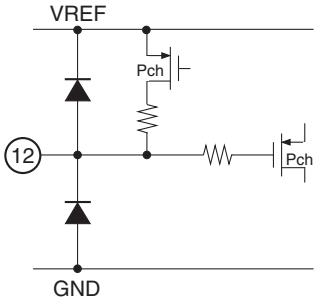
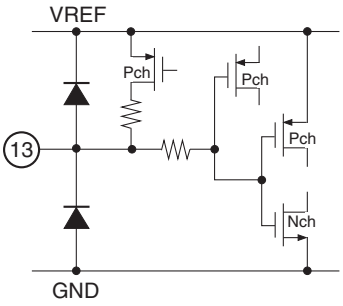


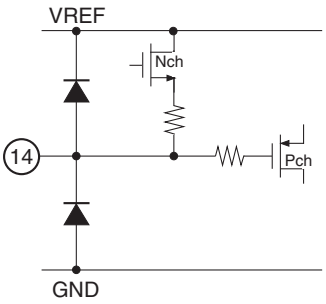
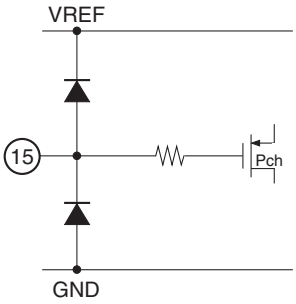
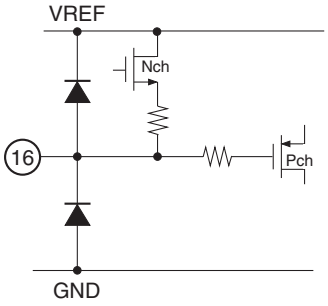
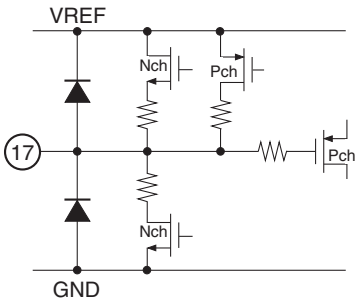
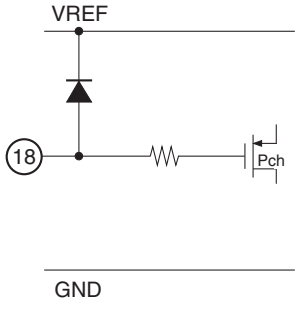
Pin Table

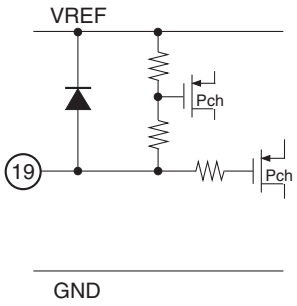
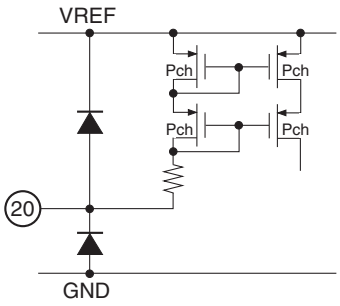
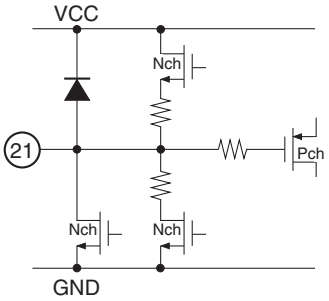
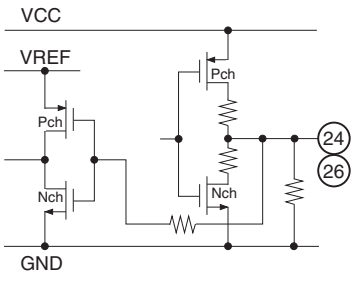
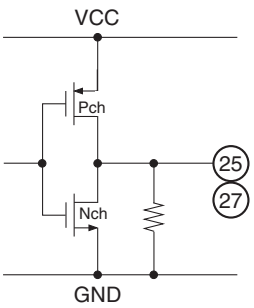
Pin No.	Symbol	Description	Connection end of protection diode
1	PFC_OUT1	PFC MOSFET gate driver output (master)	—
2	MODE1	Mode determination pin1 (Active STBY when MODE1 = Low, MODE2 = High)	VCC, GND
3	PFC_OUT2	PFC MOSFET gate driver output (slave)	—
4	AC_DETIN	AC voltage sense input	VCC, GND
5	AC_VRMS	AC peak voltage sense and PFC enable	VCC, GND
6	PFC_ZCD1	PFC zero current detect input (master)	VCC, GND
7	PFC_ZCD2	PFC zero current detect input (slave)	VCC, GND
8	PFC_CS1	PFC overcurrent detect input (master)	VREF, GND
9	PFC_CS2	PFC overcurrent detect input (slave)	VREF, GND
10	GND_S	Sub GND for connecting external parts	—
11	PFC_VAO	PFC voltage control error amplifier output	VREF, GND
12	PFC_VSENSE	PFC output voltage sense input	VREF, GND
13	PFC_OVP	PFC output overvoltage sense input	VREF, GND
14	PFC_TONMAX	PFC maximum ON time control	VREF, GND
15	RM_OFFADJ	Resonant controller stop voltage adjustment and abnormal latch input	VREF, GND
16	RM_FMIN	Resonant controller minimum frequency setting	VREF, GND
17	RM_SS	Resonant controller soft start and overcurrent timer-latch setting	VREF, GND
18	RM_CS2	Resonant controller overcurrent sense input (continuous overcurrent)	VREF
19	RM_CS1	Resonant controller overcurrent sense input (pulse by pulse overcurrent)	VREF
20	RM_RT	Resonant controller frequency control	VREF, GND
21	VREF	Internal supply voltage	VCC, GND
22	GND	GND	—
23	VCC	Power supply input	GND
24	B_OK	PFC-OK signal output	—
25	RM_OUTN	Resonant controller Low-side MOSFET driver output	—
26	AC_DETOUT	AC off detect signal output	—
27	RM_OUTP	Resonant controller High-side MOSFET driver output	—
28	MODE2	Mode determination pin2 (SEQ mode when MODE1 = Low, MODE2 = Low)	VCC, GND

Pin Description

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
1 3	PFC_OUT1 PFC_OUT2	O O	VCC to GND		PFC MOSFET gate driver output (Connect to the NMOS gate for PFC)
2 28	MODE1 MODE2	II	VCC to GND		Mode select input (GND connection: Normal sequence VCC connection: Standby mode)
4	AC_DETIN	I	VCC to GND		AC voltage input (Connect to AC input detection resistor)
5	AC_VRMS	I/O	(VCC – 2.0V) to GND		AC peak voltage sense and PFC enable (Connect to peak voltage hold capacitor)
6 7	PFC_ZCD1 PFC_ZCD2	I I	4.4V to 0.6V		PFC zero current detect input (Connect to boost inductor of auxiliary winding)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
8 9	PFC_CS1 PFC_CS2	I I	VREF to GND		PFC current sense input (Connect to the detection side of current sense resistor)
10	GND_S	—	—	—	Sub GND
11	PFC_VAO	O	3.2V to GND		PFC voltage control error amplifier output (Connect a phase compensation circuit: between PFC_VAO and GND)
12	PFC_VSENSE	I	VREF to GND During steadystate: 2.5V		PFC output voltage sense input (Connect to PFC output detection resistor)
13	PFC_OVP	I	VREF to GND During steadystate: 2.5V		PFC output overvoltage sense input (Connect to PFC output detection resistor)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
14	PFC_TONMAX	I/O	3.2V to GND		PFC maximum ON time control (Connect to ON time control capacitor)
15	RM_OFFADJ	I	VREF to GND		Resonant controller stop voltage adjustment and abnormal latch input
16	RM_FMIN	I	1.2V		Resonant controller minimum frequency setting (Connect to minimum frequency control resistor)
17	RM_SS	I/O	VREF to GND During steadystate: 2.5V		Resonant controller soft start and overcurrent timer-latch setting (Connect to the capacitor for soft start)
18	RM_CS2	I I	VREF to –0.3V		Resonant controller overcurrent sense input (Connect to the resistor for current detection)

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit	Description
19	RM_CS1	I	VREF to –0.3V		Resonant controller overcurrent sense reference input (Connect to the resistor for current detection)
20	RM_RT	I	(3.5V)		Resonant controller frequency control (Connect to the photo coupler for output feedback)
21	VREF	O	5.0V		Internal supply voltage output (Connect to the capacitor for stabilization)
22	GND	—	—	—	GND
23	VCC	—	—	—	Power supply input
24	B_OK	O	VCC to GND		PFC-OK signal output
26	AC_DETOUT	O			AC off detect signal output
25	RM_OUTN	O	VCC to GND		Resonant controller Low-side MOSFET driver output (Connect to the drive transformer)
27	RM_OUTP	O			Resonant controller High-side MOSFET driver output (Connect to the drive transformer)

Electrical Characteristics

◆ Shared Blocks

(Unless otherwise specified, the conditions are Ta = 27[℃], VCC = 12[V], MODE = GND)

1. Current Consumption (VCC and PVCC pins)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption in standby mode	Istb	MODE = VCC	—	750	1000	μA
Current consumption in operation mode	Iact	AC_DETIN = 1.0V, PFC_VSENSE = 1.0V * Non Switching	—	3.6	4.3	mA

2. Under Voltage Lock Out Circuit Block (VCC pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Operation start voltage	Vact		10.2	11.0	11.8	V
Operation stop voltage	Voff		9.0	9.6	10.2	V
Hysteresis width	Vact-Voff	Vact – Voff	1.1	1.4	1.7	V

3. Reference Voltage Output Circuit Block (VREF pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output voltage	Vvref		4.85	5.00	5.15	V
Input stability	Vline	VCC = 10.5V to 18V	—	10	30	mV
Load stability	Vload	Iload = 0.1mA to 5mA	—	20	50	mV
Pin voltage when NG latch (When TSD)	Vvrefng	Iout = 10mA (Design guarantee)	—	0.1	0.5	V

4. AC Input Detection Circuit Block (AC_DETIN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC operation start and stop voltage	Vpfcon	AC_DETIN peak voltage (rise)	1.80	1.85	1.90	V
	Vpfcoff	AC_DETIN peak voltage (fall)	1.60	1.65	1.70	V
Hysteresis width	Vpfchys	Vpfcon – Vpfcoff	0.17	0.20	0.23	V
AC detection reference voltage High 1	Vthach1	AC_VRMS = 7.5V	4.675	4.875	5.075	V
AC detection reference voltage High 2	Vthach2	AC_VRMS = 2.0V	1.1	1.3	1.5	V
AC off detection delay time	Tdlyacoff	AC_DETIN < AC_VRMS × 65% (State B)	6.4	8	9.6	ms
AC recovery detection delay time	Tdlyacon	AC_DETIN > AC_VRMS × 65% (State C)	8	10	12	ms

5. AC Off Detect Signal Output Circuit Block (AC_DETOUT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vacoutl	VCC = 18V, Iout = 10mA	—	0.5	1.0	V
Output High voltage	Vacouth	VCC = 18V, .Iout = –10mA	17.0	17.5	—	V

6. MODE Pin Voltage Detection Circuit Block (MODE1, MODE2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
MODE detection voltage Low	Vmodel		5.2	—	5.6	V
MODE detection voltage High	Vmodeh		7.6	—	8.4	V
Internal pull-up resistor value	Rmode	MODE = 0.1V	35	50	65	kΩ

7. Clock Timer

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
1ms clock	Tclock		972	1024	1075	μs

◆ PFC Block

(Unless otherwise specified, the conditions are Ta = 27[℃], VCC = 12[V], MODE1 = GND, MODE2 = GND)

8. PFC Output Circuit Block (PFC_OUT1, PFC_OUT2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vpoutl	VCC = 18V, Iout = 10mA	—	0.03	0.1	V
Output High voltage	Vpouth	VCC = 18V, Iout = –10mA	17.85	17.9	—	V
Rise time*1	Tpoutr	VCC = 18V, CLOAD = 1000pF	—	35	100	ns
Fall time*1	Tpoutf	VCC = 18V, CLOAD = 1000pF	—	25	100	ns

*1 Rise time and fall time use VCC × 0.1 to VCC × 0.9 as the judgment voltages.

9. PFC-OK Signal Circuit Block (B_OK pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vacoutl	VCC = 18V, Iout = 10mA	—	0.5	1.0	V
Output High voltage	Vacouth	VCC = 18V, Iout = –10mA	17.0	17.5	—	V

10. AC Peak Voltage Sense Circuit Block (AC_VRMS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Internal pull-down resistor value	Rvrms	AC_VRMS = 1.0V	0.8	1.0	1.2	MΩ
AC off discharge resistor value	Rvrmsdchg	AC_VRMS = 7.0V	104	130	156	kΩ
Sag recovery operation switching voltage	Vthsag		4.950	5.100	5.250	V
ZCD protection disable voltage	Vthzcdp		7.14	7.29	7.44	V

11. PFC overcurrent detection circuit block master CH (PFC_CS1 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Overcurrent detection voltage1	Vthcs1	AC_VRMS = 1.65V	0.365	0.400	0.435	V
Overcurrent detection voltage2	Vthcs2	AC_VRMS = 2.55V	0.365	0.400	0.435	V
Power limit detection voltage1	VthDPL1	AC_VRMS = 2.55V	0.442	0.491	0.540	V
Power limit detection voltage2	VthDPL1	AC_VRMS = 6.0V	0.209	0.232	0.255	V
Blanking time	Tleb	PFC_CS = 1.0V	200	250	300	ns
Delay time	Tcsdly	CS to DRV PFC_CS = 0V ⇒ 1V (Rectangular waveform input)	100	150	200	ns

12. PFC overcurrent detection circuit block slave CH (PFC_CS2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Overcurrent detection voltage1	Vthcs1	AC_VRMS = 1.65V	0.365	0.400	0.435	V
Overcurrent detection voltage2	Vthcs2	AC_VRMS = 2.55V	0.365	0.400	0.435	V
Blanking time	Tleb	PFC_CS = 1.0V	200	250	300	ns
Delay time	Tcsdly	CS to DRVPFC_CS = 0V ⇒ 1V (Rectangular waveform input)	100	150	200	ns

13. PFC zero current detection circuit block (PFC_ZCD1, PFC_ZCD2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Input threshold voltage	Vthzcd		1.2	1.3	1.4	V
Hysteresis width	Vzcdhys		180	200	220	mV
Clamp High voltage	Vclph	I = 3mA	4.0	4.4	5.0	V
Clamp Low voltage	Vclpl	I = –3mA	0.3	0.6	1.0	V
Restart timer delay	Tstart	(master CH only)	180	200	220	μs
Minimum off time (During overcurrent detection)	Toffmin	PFC_CS = 1.0V	3.32	4.00	4.73	μs
Blanking time	Tteb		(384)	(480)	(576)	ns

14. Error Amplifier Output Circuit Block for PFC Voltage Control (PFC_VAO pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Trans-conductance	Vvaogm	(Design guarantee)	—	(90)	—	μA/V
Output High clamp voltage	Vvaoh	PFC_VSENSE = 2.0V	3.1	3.3	3.5	V
Power limit clamp voltage ratio1	Vvao1	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	85	90	95	%
Power limit clamp voltage ratio2	Vvao2	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	75	80	85	%
Power limit clamp voltage ratio3	Vvao3	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	65	70	75	%

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Power limit clamp voltage ratio4	Vvao4	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	55	60	65	%
Power limit clamp voltage ratio5	Vvao5	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	45	50	55	%
Power limit clamp voltage ratio6	Vvao6	PFC_VSENSE = 2.0V Voltage ratio to internal reference voltage (typ.3.0V) to determine PFC max. ON time	35	40	45	%
Source current	Ivaosc	PFC_VSENSE = 2.2V, PFC_VAO = 0.5V	10	20	40	μA
Output Low voltage	Vvaol	PFC_VSENSE = 2.55V	0	—	0.2	V
Sink current	Ivaosk	PFC_VSENSE = 2.65V, PFC_VAO = 3.0V	5	15	25	μA

15. PFC Maximum ON Time Control Circuit Block (PFC_TONMAX pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
ON time1 master CH	Ton1	PFC_VSENSE = 2.0V, AC_VRMS = 2.5VRt = 5.6kΩ	10.08	11.20	12.32	μs
ON time2 master CH	Ton2	PFC_VSENSE = 2.0V, AC_VRMS = 5.0VRt = 5.6kΩ	2.67	2.97	3.27	μs
ON time matching	Rton2/1	PFC_VSENSE = 2.0V, AC_VRMS = 2.5V Rt = 5.6kΩ (Design assurance)	(–8.0)	(–5.0)	(–2.0)	%

16. PFC Output Voltage Detection Circuit Block (PFC_VSENSE pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC stop voltage	Vovp2		2.659	2.7	2.742	V
PFC stop cancel voltage	Vovp2hys		2.548	2.6	2.652	V
PFC control voltage	Vpfccnt		2.475	2.5	2.525	V
PFC non-operating detection voltage and B_OK High level threshold	Vpfcnonact		2.280	2.4	2.520	V
B_OK Low level threshold	Vpfcbokl		2.254	2.3	2.346	V
Resonant controller operation start voltage	Vrmstart		2.100	2.143	2.186	V
Resonant controller operation stop voltage	Vrmstop	RM_OFFADJ = 1.883V	1.789	1.883	1.977	V
PFC stop voltage during active standby	Vasovp		1.654	1.688	1.722	V
PFC stop cancel voltage during active standby	Vasovphys		1.523	1.554	1.585	V
Resonant operation voltage during active standby	Vasrmen		1.390	1.419	1.448	V
Pin short-circuit detection	Vshort		0.2	0.3	0.4	V
Pull-up current	Ivs	PFC_VSENSE = 0.1V	0.05	0.1	0.2	μA

17. Resonant Controller Stop Voltage Adjustment Circuit Block (RM_OFFADJ pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Latch voltage for external error detection	Voffadjng		3.8	4.0	4.2	V

18. PFC Overvoltage Detection Circuit Block (PFC_OVP pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
PFC overvoltage detection voltage	Vovp11		2.857	2.922	2.981	V
Pull-up current	Iovp	PFC_VSENSE = 0.1V	0.05	0.1	0.2	μA

◆ Resonant Controller Block

(Unless otherwise specified, the conditions are Ta = 27[℃], VCC = 12[V], MODE = GND, RM_RT = OPEN, Rfmin = 120kΩ)

19. Resonant Controller Output Circuit Block (RM_OUTP, RM_OUTN pins)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Output Low voltage	Vroutl	VCC = 18V, Iout = 10mA	—	0.05	0.1	V
Output High voltage	Vrouth	VCC = 18V, Iout = –10mA	17.9	17.95	—	V
Rise time*1	Vroutr	VCC = 18V, CLOAD = 1000pF	—	35	100	ns
Fall time*1	Vroutf	VCC = 18V, CLOAD = 1000pF	—	35	100	ns

*1 Rise time and fall time use VCC × 0.1 to VCC × 0.9 as the judgment voltages.

20. Resonant Controller Soft Start Circuit Block (RM_SS pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Soft start current1	Irmss1	RM_SS = 0V	7.5	10	12.5	μA
Soft start current2	Irmss2	RM_SS = 0V, Active STBY (MODE1 = GND, MODE2 = VCC)	4.6	6.25	7.8	μA
Clamp voltage	Vrmss		2.3	2.5	2.7	V
Overcurrent timer latch detection voltage	Vtimerlatch		3.8	4.0	4.2	V
Charging current during overcurrent detection	Iocc	RM_CS = 0.3V, SS = 3.0V	3.2	5.0	6.8	μA

21. Resonant Controller Frequency Control Circuit Block (RM_RT pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Maximum oscillation frequency	Frmmax	Irt = 2mA, Rfmin = 39kΩ	800	—	—	kHz
Deadband width	Tdb		270	300	330	ns
Multiple number of clamp frequency when soft star	Fclamp	f0/f4 (f0:RM_SS = 0V, f4:RM_SS = open) Rfmin = 390kΩ	3.5	4.0	4.5	times

22. Resonant Controller Minimum Frequency Adjustment Circuit Block (RM_FMIN pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Setting frequency 1	Fmin1	Rfmin = 390kΩ	–3%	46.1	+3%	kHz
Setting frequency 2	Fmin2	Rfmin = 120kΩ	–4%	96.7	+4%	kHz
Setting frequency 3	Fmin3	Rfmin = 39kΩ	–5%	144.1	+5%	kHz
Low current detection threshold	Ifminlow		0.85	1.25	1.65	μA

23. Resonant Controller Current Detection Circuit Block (RM_CS1 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Positive side detection	Vcs1p	When RM_OUTP = High	0.209	0.220	0.231	V
Negative side detection	Vcs1n	When RM_OUTN = High	–0.295	–0.260	–0.235	V
Detection delay time	Tcsdly	CS to DRV RM_CS = –0.3V ↔0.3V (Rectangular input)	100	150	200	ns
Detection mask time	Tcsmask	RM_CS = 0.3V	384	480	576	ns
Overcurrent detection voltage ratio when +B falls	Rrmocp	VSENSE < 2.143V	10	15	20	%
RM_CS1 pin offset current	Ics1ofs	RM_CS1 = 0.1V	6.6	9.5	12.5	μA

24. Resonant Controller Current Detection Circuit Block (RM_CS2 pin)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Continuous load detection voltage	Vcs2	When RM_OUTP = High	0.158	0.175	0.193	V
Detection mask time	Tcsmask	RM_CS = 0.3V	(384)	(480)	(576)	ns
Continuous load detection time	Tcs2	(When the time corresponds to 2.1s × 5 times)		(10)		s
RM_CS2 pin offset current	Ics2ofs	RM_CS2 = 0.1V	–1.0	0	1.0	μA

Note) The shipping inspection is performed at room temperature. (The design is guaranteed with respect to temperature fluctuation.)

25. List of Electrical Characteristics

Item	Specification ratings (Ta = 27°C)			Design guarantee ratings (Ta = –25 to +85°C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (VCC, PVCC pins)							
Current consumption in standby mode	—	750	1000	—	750	1000	μA
Current consumption in operation mode	—	3.6	4.3	—	3.6	4.3	mA
Low voltage misoperation prevention circuit block (VCC pin)							
Operation start voltage	10.2	11.0	11.8	10.2	11.0	11.8	V
Operation stop voltage	9.0	9.6	10.2	9.0	9.6	10.2	V
Hysteresis width	1.1	1.4	1.7	1.1	1.4	1.7	V
Reference voltage output block (VREF pin)							
Output voltage	4.85	5.00	5.15	4.85	5.00	5.15	V
Input stability	—	10	30	0	10	30.5(*2)	mV
Load stability	—	20	50	—	20	50	mV
Pin voltage when NG latch (When TSD)	—	0.1	0.5	—	0.1	0.5	V
AC input detection circuit block (AC_DETIN pin)							
PFC operation start voltage	1.80	1.85	1.90	1.80	1.85	1.90	V
	1.60	1.65	1.70	1.60	1.65	1.70	V
Hysteresis width	0.17	0.20	0.23	0.17	0.20	0.23	V
AC detection reference voltage High 1	4.675	4.875	5.075	4.675	4.875	5.075	V
AC detection reference voltage High 2	1.1	1.3	1.5	1.1	1.3	1.5	V
AC off detection delay time	6.4	8	9.6	6.4	8	9.6	ms
AC recovery detection delay time	8	10	12	8	10	12	ms
AC input error detection output circuit block (AC_DETOUT pin)							
Output Low voltage	—	0.5	1	—	0.5	1	V
Output High voltage	17	17.5	—	17	17.5	—	V
Mode pin determination circuit block (MODE1, MODE2 pin)							
MODE detection voltage Low	5.2	—	5.6	5.2	—	5.6	V
MODE detection voltage High	7.6	—	8.4	7.6	—	8.4	V
Internal pull-up resistor value	35	50	65	35	50	65	kΩ
Clock timer							
1ms clock	972	1024	1075	972	1024	1075	μs
PFC Output Circuit Block (PFC_OUT1, PFC_OUT2 pin)							
Output Low voltage	—	0.03	0.1	—	0.03	0.1	V
Output High voltage	17.85	17.9	—	17.85	17.9	—	V
Rise time	—	35	100	—	35	100	ns
Fall time	—	25	100	—	25	100	ns
PFC-OK signal circuit block (PFC_OK pin)							
Output Low voltage	—	0.5	1	—	0.5	1	V
Output High voltage	17	17.5	—	17	17.5	—	V

Item	Specification ratings (Ta = 27°C)			Design guarantee ratings (Ta = –25 to +85°C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
AC peak voltage monitor circuit block (AC_VRMS pin)							
Internal pull-down resistor value	0.8	1.0	1.2	0.8	1.0	1.2	MΩ
AC off discharge resistor value	104	130	156	104	130	156	kΩ
Sag recovery automatic switching voltage	4.950	5.100	5.250	5.233	5.383	5.533	V
ZCD protection disable voltage	7.14	7.29	7.44	7.14	7.29	7.44	V
PFC overcurrent detection circuit block master CH (PFC_CS1 pin)							
Overcurrent detection voltage1	0.365	0.400	0.435	0.365	0.400	0.435	V
Overcurrent detection voltage2	0.365	0.400	0.435	0.365	0.400	0.435	V
Power limit detection voltage1	0.442	0.491	0.540	0.442	0.491	0.540	V
Power limit detection voltage2	0.209	0.232	0.255	0.209	0.232	0.255	V
Blanking time	200	250	300	200	250	300	ns
Delay time	100	150	200	100	150	200	ns
PFC overcurrent detection circuit block slave (PFC_CS2 pin)							
Overcurrent detection voltage1	0.365	0.400	0.435	0.365	0.400	0.435	%
Overcurrent detection voltage2	0.365	0.400	0.435	0.365	0.400	0.435	%
Blanking time	200	250	300	200	250	300	ns
Delay time	100	150	200	100	150	200	ns
PFC zero current detection circuit block (PFC_ZCD1, PFC_ZCD2 pin)							
Input threshold voltage	1.2	1.3	1.4	1.2	1.3	1.4	V
Hysteresis width	180	200	220	180	200	220	mV
Clamp High voltage	4	4.4	5	4	4.4	5	V
Clamp Low voltage	0.3	0.6	1	0.3	0.6	1	V
Restart timer delay	180	200	220	180	200	220	μs
Minimum off time (When overcurrent is detected)	3.32	4.00	4.73	3.32	4.00	4.73	μs
Blanking time	(384)	(480)	(576)	(180)	(220)	(260)	ns
Error amplifier output circuit block for PFC voltage control (PFC_VAO pin)							
Trans-conductance	—	(90)	—		(90)		μA/V
Output High clamp voltage	3.1	3.3	3.5	3.1	3.3	3.5	V
Power limit clamp voltage ratio1	85	90	95	85	90	95	%
Power limit clamp voltage ratio2	75	80	85	75	80	85	%
Power limit clamp voltage ratio3	65	70	75	65	70	75	%
Power limit clamp voltage ratio4	55	60	65	55	60	65	%
Power limit clamp voltage ratio5	45	50	55	45	50	55	%
Power limit clamp voltage ratio6	35	40	45	35	40	45	%
Source current	10	20	40	10	20	40	μA
Output Low voltage	0	—	0.2	0	—	0.2	V
Sink current	5	15	25	5	15	25	μA

Item	Specification ratings (Ta = 27°C)			Design guarantee ratings (Ta = –25 to +85°C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PFC maximum ON time control circuit block (PFC_TONMAX pin)							
ON time1 master CH	10.08	11.20	12.32	10.08	11.20	12.32	μs
ON time2 master CH	2.67	2.97	3.27	2.67	2.97	3.27	μs
ON time matching	(–8.0)	(–5.0)	(–2.0)	(–8.0)	(–5.0)	(–2.0)	%
PFC output voltage detection circuit block (PFC_VSENSE pin)							
PFC stop voltage	2.659	2.7	2.742	2.657	2.7	2.744	V
PFC stop cancel voltage	2.548	2.6	2.652	2.548	2.6	2.652	V
PFC control voltage	2.475	2.5	2.525	2.475	2.5	2.525	V
PFC non-operating detection voltage and B_OK High level threshold	2.28	2.4	2.52	2.28	2.4	2.52	V
B_OK Low level threshold	2.254	2.3	2.346	2.254	2.3	2.346	V
Resonant controller operation start voltage	2.100	2.143	2.186	2.100	2.143	2.186	V
Resonant controller operation stop voltage	1.789	1.883	1.977	1.789	1.883	1.977	V
PFC stop voltage during active standby	1.654	1.688	1.722	1.654	1.688	1.722	V
PFC stop cancel voltage during active standby	1.523	1.554	1.585	1.523	1.554	1.585	V
Resonant operation voltage during active standby	1.390	1.419	1.448	1.390	1.419	1.448	V
Pin short-circuit detection	0.2	0.3	0.4	0.2	0.3	0.4	V
Pull-up current	0.05	0.1	0.2	0.05	0.1	0.2	μA
Resonant controller stop voltage adjustment circuit block (RM_OFFADJ pin)							
Latch voltage for external error detection	3.8	4	4.2	3.8	4	4.2	V
PFC overvoltage detection circuit block (PFC_OVP pin)							
PFC overvoltage detection voltage	2.857	2.922	2.981	2.855	2.922	2.983	V
Pull-up current	0.05	0.1	0.2	0.05	0.1	0.2	μA
Resonant controller output circuit block (RM_OUTP, RM_OUTN pins)							
Output Low voltage	—	0.05	0.1	—	0.05	0.1	V
Output High voltage	17.9	17.95	—	17.9	17.95	—	V
Rise time	—	35	100	—	35	100	ns
Fall time	—	35	100	—	35	100	ns
Resonant controller soft start circuit block (RM_SS pin)							
Soft start current1	7.5	10	12.5	7.5	10	12.5	μA
Soft start current2	4.6	6.25	7.8	4.6	6.25	7.8	μA
Clamp voltage	2.3	2.5	2.7	2.3	2.5	2.7	V
Soft start end detection voltage	2.2	2.4	2.6	2.2	2.4	2.6	V
Overcurrent timer latch detection voltage	3.8	4	4.2	3.8	4	4.2	V

Item	Specification ratings (Ta = 27°C)			Design guarantee ratings (Ta = –25 to +85°C) (*1)			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Charging current during overcurrent detection	3.2	5.0	6.8	3.2	5.0	6.8	μA
Resonant controller soft start circuit block (RM_RT pin)							
Maximum oscillation frequency	800	—	—	800	—	—	kHz
Deadband width	270	300	330	270	300	330	ns
Multiple number of clamp frequency when soft star	3.5	4.0	4.5	3.5	4.0	4.5	times
Resonant controller minimum frequency adjustment circuit block (RM_FMIN pin)							
Setting frequency 1	–3.0%	46.1	+3%	–3.8%(*2)	46.1	+3.0%(*2)	kHz
Setting frequency 2	–4.0%	96.7	+4%	–4.7%(*2)	96.7	+4.0%(*2)	kHz
Setting frequency 3	–5.0%	144.1	+5%	–5.6%(*2)	144.1	+5.0%(*2)	kHz
Constant current detection threshold	0.85	1.25	1.65	0.85	1.25	1.65	μA
Resonant controller current detection circuit block (RM_CS1 pin)							
Positive side detection	0.209	0.220	0.231	0.209	0.220	0.231	V
Negative side detection	–0.295	–0.260	–0.235	–0.295	–0.260	–0.235	V
Detection delay time	100	150	200	100	150	200	ns
Detection mask time	384	480	576	384	480	576	ns
Overcurrent detection voltage ratio when +B falls	10	15	20	10	15	20	%
RM_CS1 pin offset current	6.6	9.5	12.5	6.6	9.5	12.5	μA
Resonant controller current detection circuit block (RM_CS2 pin)							
Continuous load detection voltage	0.158	0.175	0.193	0.158	0.175	0.193	V
Detection mask time	(384)	(480)	(576)	(384)	(480)	(576)	ns
Continuous load detection voltage	0.158	0.175	0.193	0.158	0.175	0.193	V
Continuous load detection time	—	(10)	—		(10)		s
RM_CS2 pin offset current	–1.0	0	1.0	–1.0	0	1.0	μA

*1 Ratings are design guarantee values within this temperature range.

*2 Specification values at room temperature may not be satisfied because of temperature dependence.

Detailed Description of Each Block

◆ Common Circuit Block

1. Misdetection Prevention Circuit

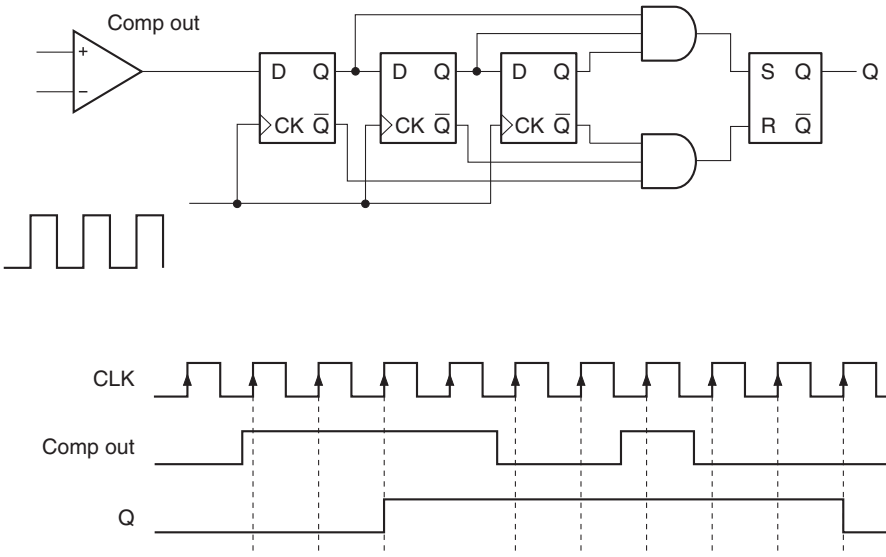


Fig. 1. Equivalent Circuit of 1 ms × 3 times-Sampling Chatter Filter

Fig. 1 above shows the equivalent circuit of 1 ms × 3 times-sampling chatter filter.
When CLK has a 1 ms cycle, Comp out is monitored at the rising edge of every 1 ms, and the output Q is defined when it reaches three times. The other chatter filters also operate using a similar circuit.

The clocks used for each setup time are generated by frequency dividing the 1 MHz clock. The setup time variance of the 1 ms × 3 times chatter filter in the example above is as follows. Variance of 2 ms < setup time < 3 ms occurs due to the Comp out inversion timing. In addition, taking into account the basic clock 1 kHz variance, the 1 ms (1024 μs) clock has variance of 0.972 ms to 1.075 ms (±5 %), so at the maximum variance the setup time variance is 1.944 ms < setup time < 3.225 ms.

Setup time of misdetection prevention counter (when the basic clock of 1MHz has no variance) used for this IC is shown below.

- Corresponds to 1μs × 4 times.....3μs to 4μs
- Corresponds to 4μs × 3 times.....8μs to 12μs
- Corresponds to 16μs × 3 times.....32μs to 48μs
- Corresponds to 32μs × 3 times.....64μs to 86μs
- Corresponds to 128μs × 3 times.....256μs to 384μs
- Corresponds to 128μs × 5 times.....512μs to 640μs
- Corresponds to 1ms × 3 times.....2ms to 3ms (Converted by 1ms for 1.024ms)
- Corresponds to 1ms × 5 times.....4ms to 5ms
- Corresponds to 8ms × 6 times.....40ms to 48ms (Converted by 8ms for 8.192ms)
- Corresponds to 66ms × 8 times.....462ms to 528ms (Converted by 66ms for 65.5ms)
- Corresponds to 2.1s × 3 times.....4.2s to 6.3s (Converted by 2.1s for 2.097s)
- Corresponds to 2.1s × 5 times.....8.4s to 10.5s

2. AC Detection Circuit Block

Fig. 2-1 shows the AC detection block equivalent circuit.

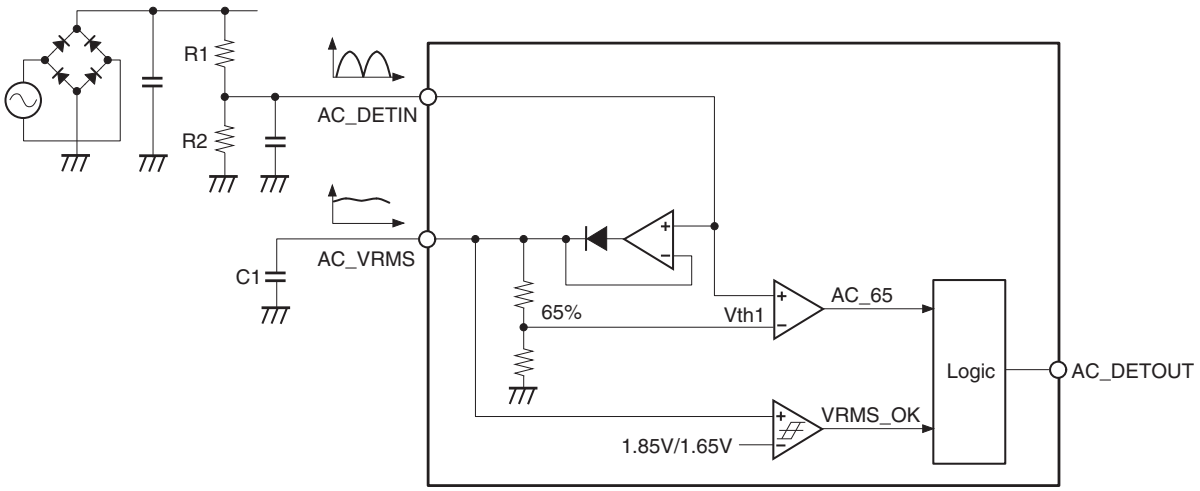


Fig. 2-1. AC Detection Block Equivalent Circuit

The AC detection circuit block detects the AC input voltage by directly monitoring the full-wave rectified AC input waveform.The wave input to the AC_DETIN pin is peak-held at the AC_VRMS pin by a buffer circuit, and reference voltages equivalent to 65% (Vth1) of the peak value are generated internally.The AC input is constantly monitored to determine the voltage range by comparing these reference voltages and the AC_DETIN pin voltage.The AC_VRMS pin voltage is compared with the internal reference voltages, and AC input is detected when the AC_VRMS pin voltage is 1.85V or more, or AC OFF when 1.65V or less. When R1 = 1320kΩ and R2 = 27kΩ in Fig. 2-1, AC input is detected when VAC = 65.3Vrms or more.In addition, connect a capacitor of at least 0.47μF or more to the AC_VRMS pin.An internal resistor is provided to generate the 65% voltages of the AC_VRMS pin voltage, and when this external capacitance value is too small, discharge may make peak hold impossible.

Fig. 2-2 shows the state transition diagram for the AC OFF detection circuit.The state transition conditions are related to the POR, AC65 and VRMSOK input signals, and the timer values in each state.POR is the IC reset signal, and AC65 and VRMSOK are the outputs of each comparator shown in Fig. 2-1. 4μs × 3 times filter processing is applied to these signals.The state transition logic operating frequency is 7.8kHz.In addition, regardless of the state transitions shown in Fig. 2-2, VRMSOK2 = High (AC_VRMS pin voltage > 1.85V) must be set up to obtain AC_DETOUT = High output at start-up. After VRMSOK2 = High is detected (1ms × 3 times), AC_DETOUT goes High.

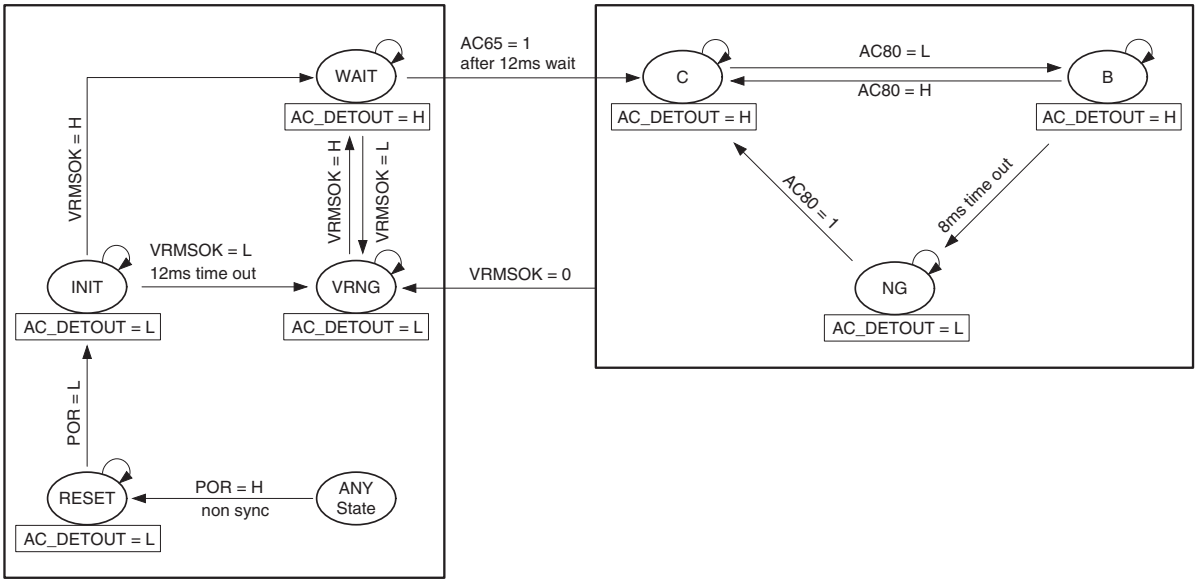


Fig. 2-2. AC Detection State Transition Diagram

The AC_DETOUT pin is the output signal for this function, and outputs High when the AC input state is normal, or Low when AC OFF or other abnormal state is detected. Changing “L” to “H” of AC_DETOUT pin requires detecting "C" period one time or remaining in "C" period 10ms or more.

Fig. 2-3 shows an image of the state transitions when normal AC input continues.

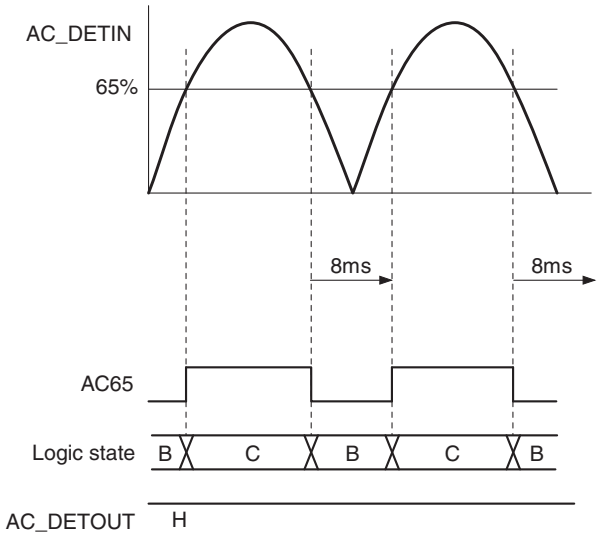


Fig. 2-3. AC_DETIN Input Waveform and State Transitions

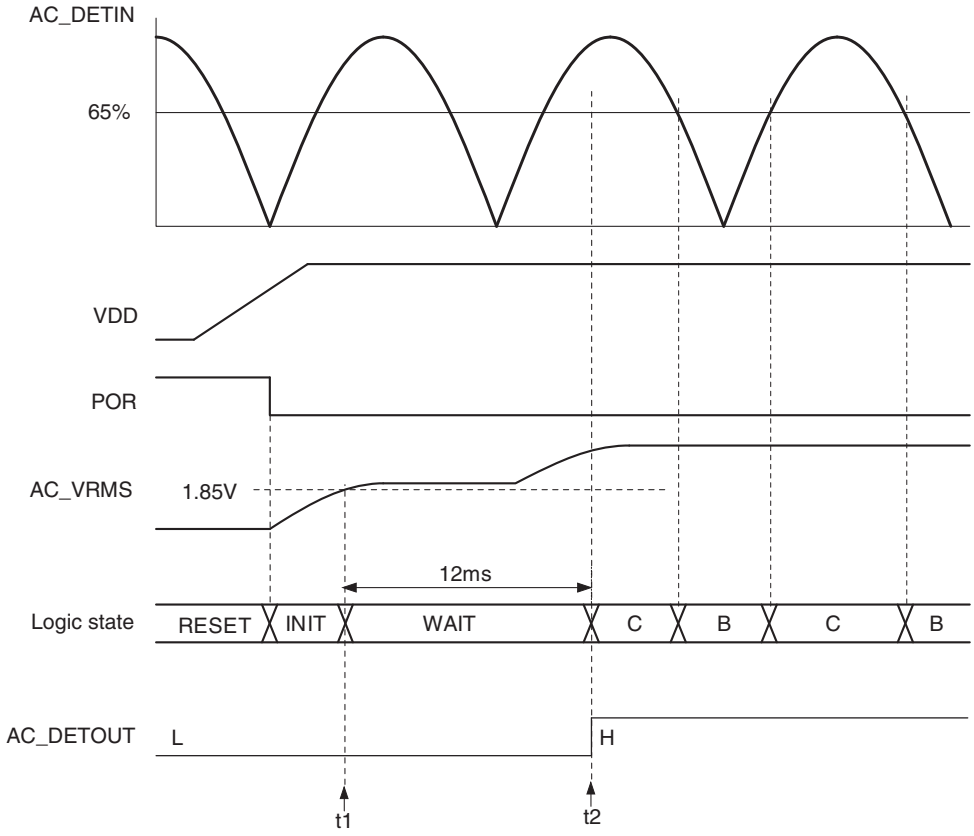
In Fig. 2-3, the internal logic signal transitions as follows.

- When the AC input rises to 65% or more within 8ms after the state transitions to "B", the state transitions to "C".
- When the AC input falls to 65% or less after the state transitions to "C", the state transitions to "B".

When the above cycle repeats, AC_DETOUT continues to output High.

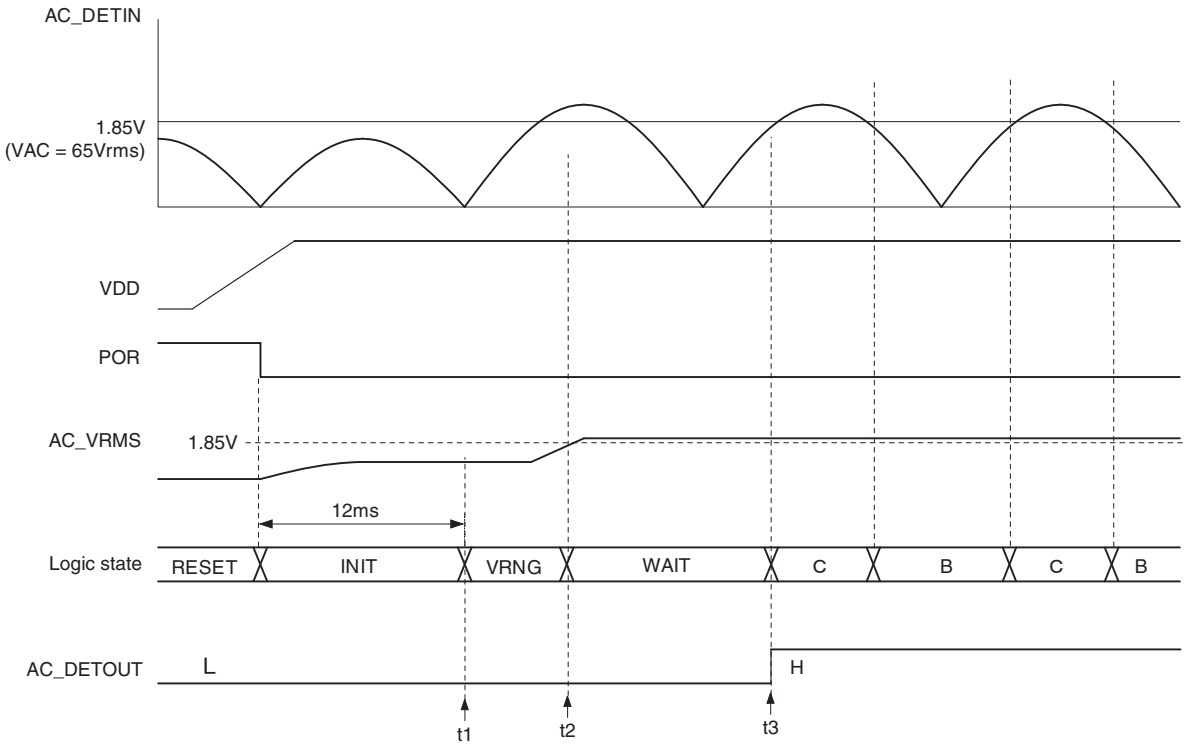
Other behaviors during start-up or AC voltage OFF are described on the following pages.

◆ **During normal start-up**



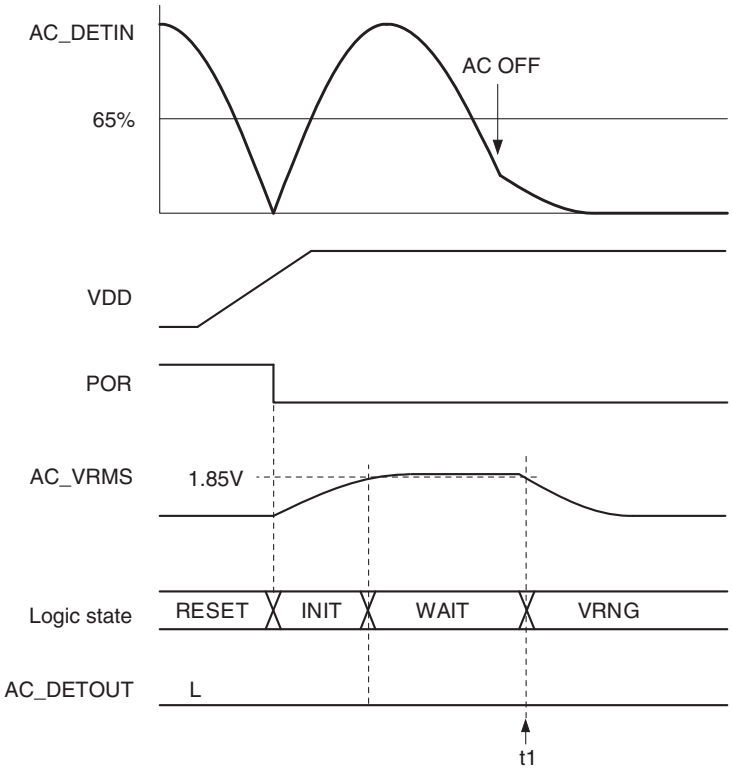
- When POR is canceled after power-on, the state transitions to "INIT". AC_DETOUT is Low output in the "RESET" and "INIT" states.
- When the AC_VRMS pin voltage rises to 1.85V or more in the "INIT" state, the state transitions to "WAIT" (t1).
- When the AC_DETIN pin voltage exceeds 65% of the AC_VRMS pin voltage after 12ms have elapsed in the "WAIT" state, the state transitions to "C" (t2) and the normal state judgment cycle starts.

◆ **Start-up when the AC voltage is low**



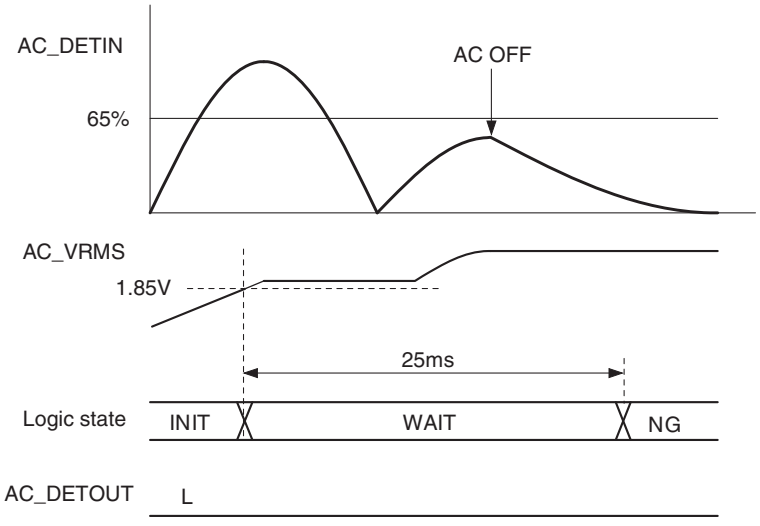
- When the AC_VRMS pin voltage does not reach 1.85V within 12ms in the "INIT" state after POR is canceled, an AC input error is judged, the state transitions to "VRNG", and AC_DETOUT continues to output Low (t1).
- When the IC detects that the AC_VRMS pin voltage has risen to 1.85V or more in the "VRNG" state, the state transitions to "WAIT" (t2).
- When the IC detects "C" period after 12ms has passed in the "WAIT" state, AC_DETOUT = “H” output is setup (t3).

◆ **When AC OFF occurs in the "WAIT" state (1)**



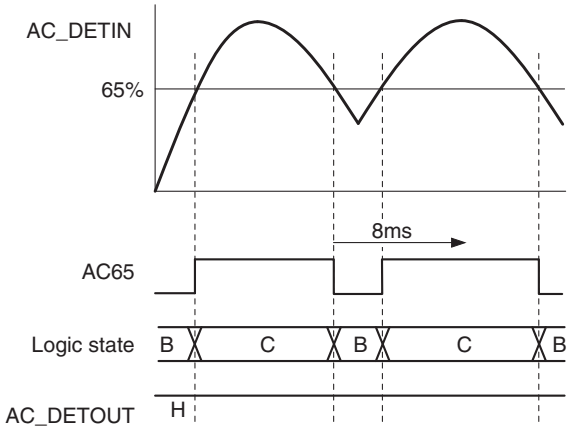
- When the AC_VRMS pin voltage falls to 1.85V or less in the "WAIT" state, AC OFF is judged, the state transitions to "VRNG" (t1). In this case, the AC_DETOUT pin does not output “H” because "C" period is not detected.

◆ **When AC OFF occurs in the "WAIT" state (2)**



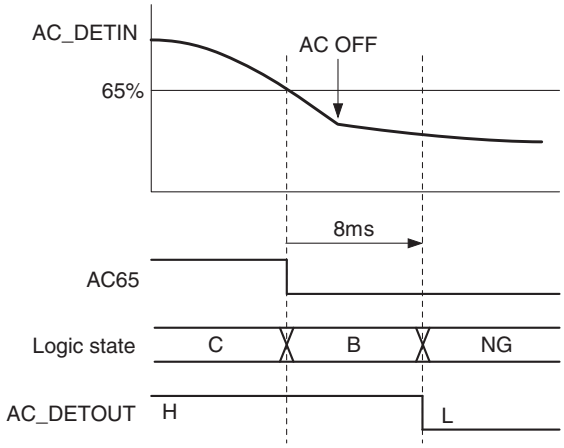
- When the AC_VRMS pin voltage is 1.85V or more but the AC_DETIN pin voltage has not reached 65% of the AC_VRMS pin voltage (the state has not transitioned to "C") within 25ms after the state transitions to "WAIT", AC OFF is judged, the state transitions to "NG", and the AC_DETOUT outputs Low.In this case, the AC_DETOUT pin does not output High because "C" period is not detected.

◆ **During normal AC input**



- When the AC_DETIN pin voltage rises to 65% or more of the AC_VRMS pin voltage within 8ms after the state transitions to "B", the state transitions to "C".
- AC_DETOUT continues to output High even if AC_DETIN voltage does not decrease to 0V when the state continues to repeat the cycle of “C” → “B” → “C”.

◆ **AC OFF in the "B" state**

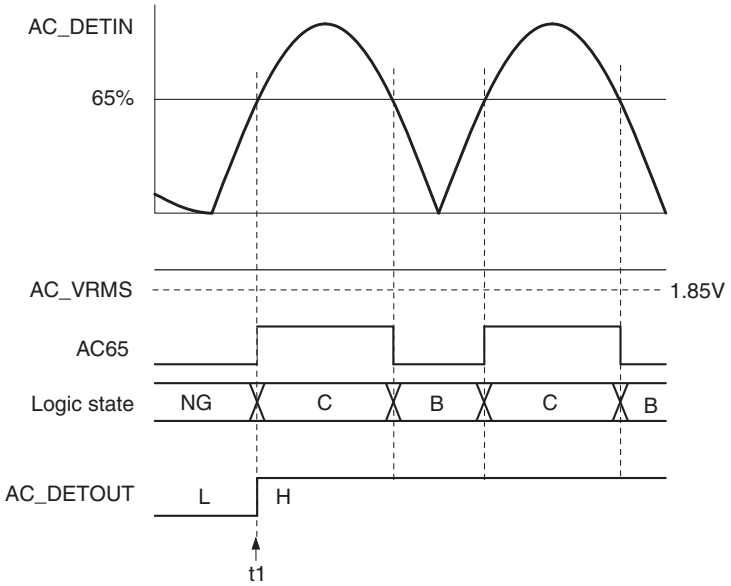


- When the AC_DETIN pin voltage does not rise to 65% or more of the AC_VRMS pin voltage within 8ms after the state transitions to "B", AC OFF is judged, the state transitions to "NG", and AC_DETOUT outputs Low.

◆ **AC OFF in the "C" state**

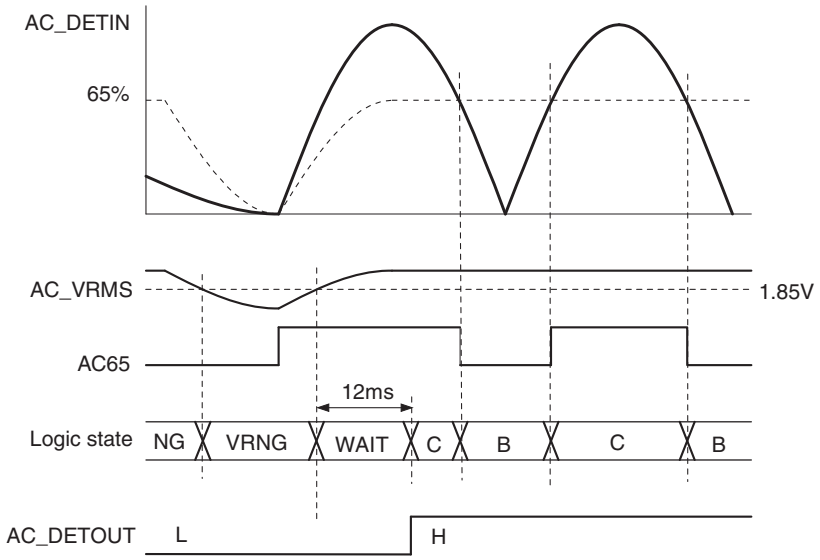
- When the AC_DETIN pin voltage does not fall to 65% or less of the AC_VRMS pin voltage after the state transitions to "C", AC OFF is not judged and the AC_DETOUT continues to output High. In other words, AC OFF is not judged in the "C" state.
- AC OFF in the "C" state is judged after the AC_DETIN pin voltage falls to 65% or less of the AC_VRMS pin voltage and the state transitions to "B" or the AC_VRMS pin voltage falls to 1.85V or less.

◆ **Return to the normal cycle from the "NG" state (1)**



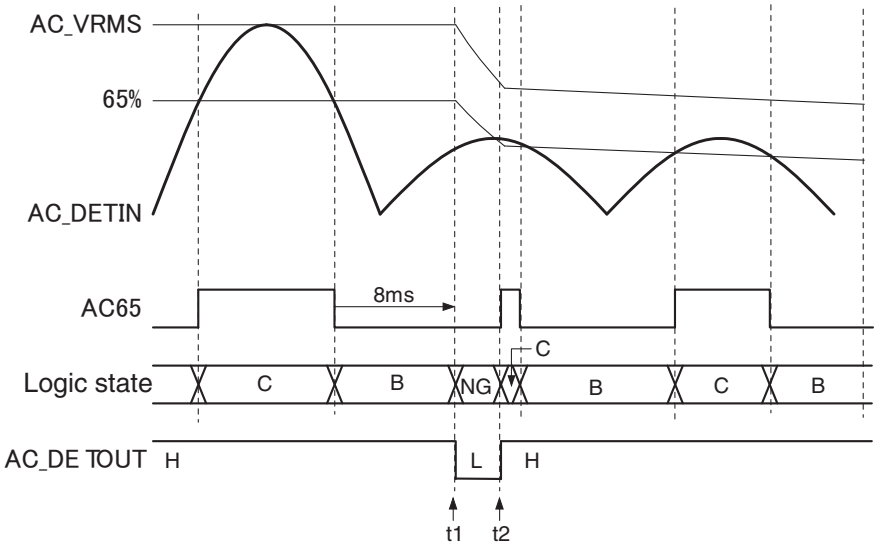
- When the AC_DETIN pin voltage rises to 65% or more of the AC_VRMS pin voltage while the AC_VRMS pin voltage is 1.85V or more in the "NG" state, the state transitions to "C", the AC_DETOUT outputs High (t1), and the normal state judgment cycle starts.

◆ **Return to the normal cycle from the "NG" state (2)**



- When the AC_VRMS pin voltage falls to 1.85V or less in the "NG" state, the state transitions to "VRNG".
- When AC is input again and the AC_VRMS pin voltage rises to 1.85V or more, the state transitions to "WAIT", Then, when the AC input rises to 65% or more the state transitions to "C". After that, the AC_DETOUT = High output is setup and the normal state judgment cycle starts.

◆ **AC_VRMS pin discharge function in the "NG" state**



- This IC has a function of discharging the AC_VRMS pin in the "NG" state in order to return quickly to the state of the AC_DETOUT = “H” when AC OFF is detected because AC input voltage is changed rapidly.
- When 8ms or more has passed after the state transitions to "B", the state transitions to "NG" and starts discharge of the AC_VRMS pin (t1).
- Discharge of the AC_VRMS pin continues till the AC_DETIN pin voltage exceeds 65% of the AC_VRMS pin voltage (t2) or the AC_VRMS pin voltage falls to 1.85V or less.
- When the AC_DETIN pin voltage exceeds 65% of the AC_VRMS pin voltage, the state transitions to "C". and the AC_DETOUT outputs High (t2) and the normal state judgment cycle starts.

3. MODE1, MODE2 Pin Voltage Detection Circuit Block

Four normal mode of standby mode, sequence start-up mode, rapid start-up mode and active standby mode can be set in accordance with the MODE pin input voltage.In addition, this IC has two test modes used to set the minimum resonant controller and to check PFC overcurrent point. The table below shows MODE1, MODE2 pin voltage setting and mode transition setup time in each mode.

MODE1 pin	MODE2 pin	Operation mode	Description of operation mode	Mode setup time
VCC or OPEN	VCC or OPEN	Standby mode	Standby mode ACDET enable/PFC OFF/Resonant controller OFF	32μs × 3 times
GND	GND	Sequence start-up mode	Sequence start-up mode same as CXA3809 After +B > 330V is detected, resonant controller starts up by 8ms × 6 times.	32μs × 3 times
VCC or OPEN	GND	Rapid start-up mode	Start-up mode aimed at shortening start-up time After +B > OFFADJ is detected, resonant controller starts up by 8ms × 4 times.	32μs × 3 times
GND	VCC or OPEN	Active standby mode	Mode aimed at developing efficiency when applying light load PFC performs burst operation (single operation) at 260V to 240V, resonant controller starts up by 8ms × 4 times after +B > 220V is detected.	16μs × 3 times
VCC or OPEN	Interme diate voltage	PFC overcurrent test mode	Test mode to disable power limit Outputs overcurrent detection signal from B_OK pin, start-up is same as SEQ start-up mode.	1ms × 3 times
Interme diate voltage	VCC or OPEN	Resonant test mode	Test mode to check resonant frequency Same as test mode when CXA3809 MODE pin voltage = intermediate voltage During this mode, AC_DETOUT/B_ OK pin is Hi-Z.	1ms × 3 times

In addition, intermediate voltage in the table indicates 5.6V to 7.6V.

4. State Transition between operation modes

Fig. 4 shows the state transition diagram between operation modes. Transition between active standby mode and rapid start-up mode requires simultaneous inversion of MODE1 and MODE2 logic. Always switch logic through MODE1 = “L”, MODE2 = “L” because the state may transition to standby mode if the state of MODE1 = “H”, MODE2 = “H” is occurred even in a socond.

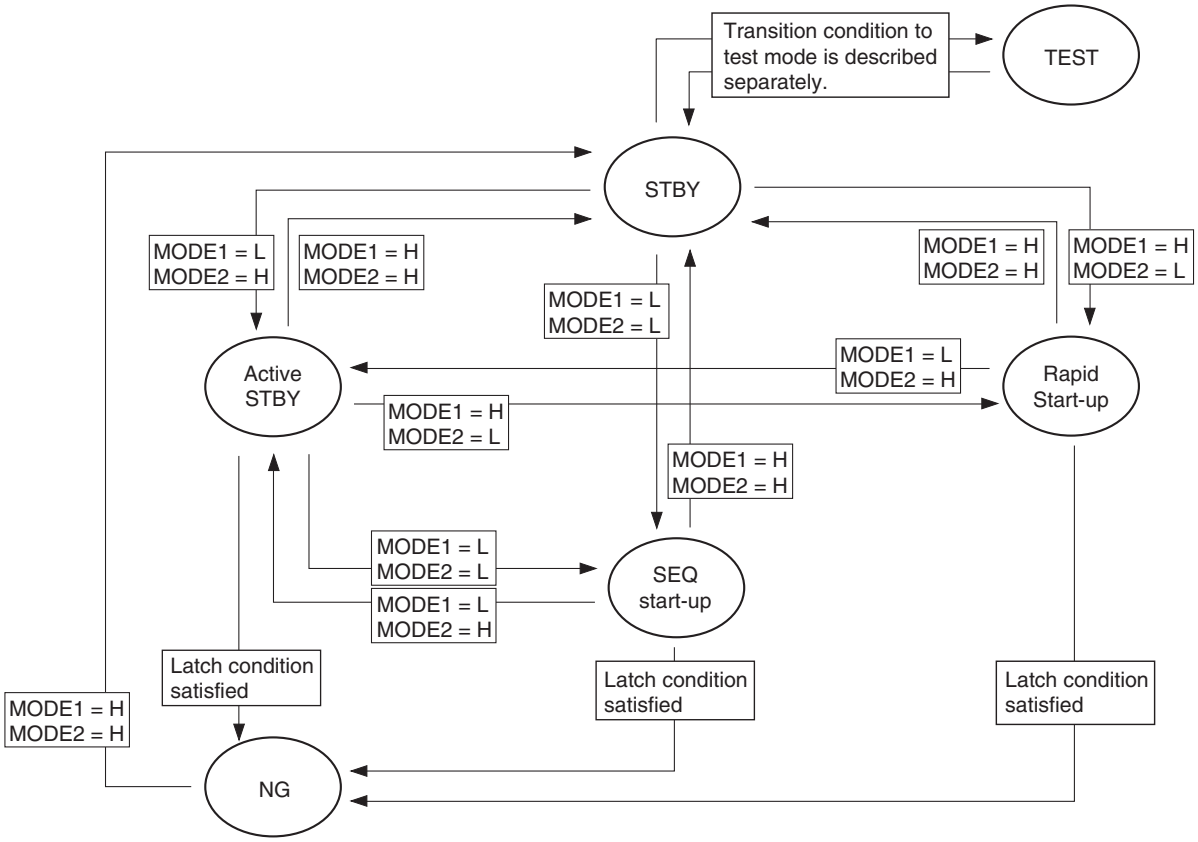


Fig.4 State Transition Diagram

5. B_OK Signal Output Circuit Block

When the PFC output voltage (+B) rises to 370V or more is detected, the B_OK signal goes to High output. In addition, when the PFC output voltage falls to 354V or less is detected, the B_OK signal goes to Low output. Detection setup time is correspondence of 128µs × 3 times for both rise and fall.Fig. 5 shows the B_OK signal output timing chart. In addition, the B_OK signal is also Low during the follwing operations.

- During NG latch
- When transition to standby mode
- When the PFC circuit is stopped (after AC_VRMS < 1.65V, 66ms × 8 times is set up)

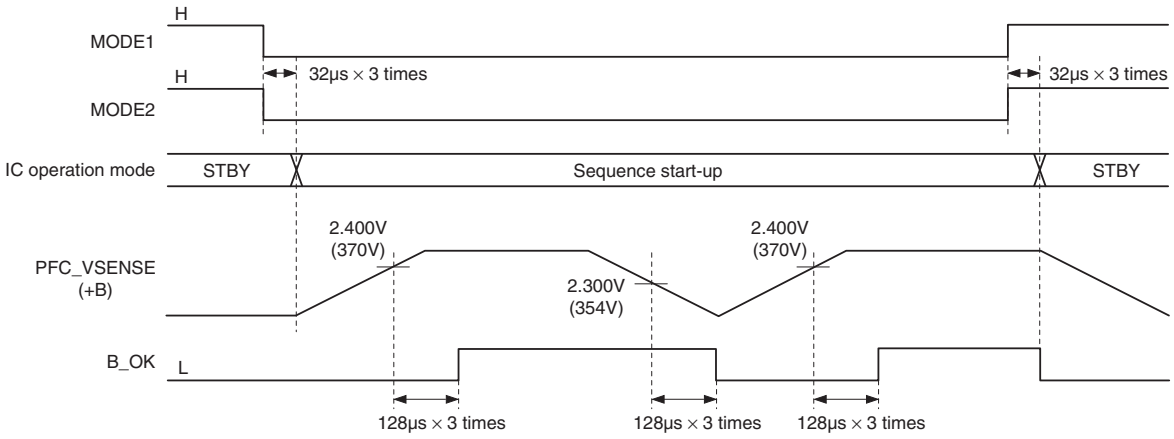


Fig.5. B_OK Signal Output Sequence

◆ PFC Block

6. PFC Control Circuit Block

This IC has control circuit of interleave power-factor correction converter in critical conduction mode. As shown in the Fig. 6, this includes the cycle measurement circuit and the sync circuit which control ON pulse of the two converters connected in parallel to have 180° phase difference. The interleave operation is performed by the sync control of master slave method. The phase of step-up converter which the PFC_OUT1 drives is master, and the phase of step-up converter which the PFC_OUT2 drives is slave. The turn on timing of main switch (Q2) on slave side is controlled by the timing which is delayed 1/2 times of the cycle of master side from the turn on timing of main switch (Q1) on master side.

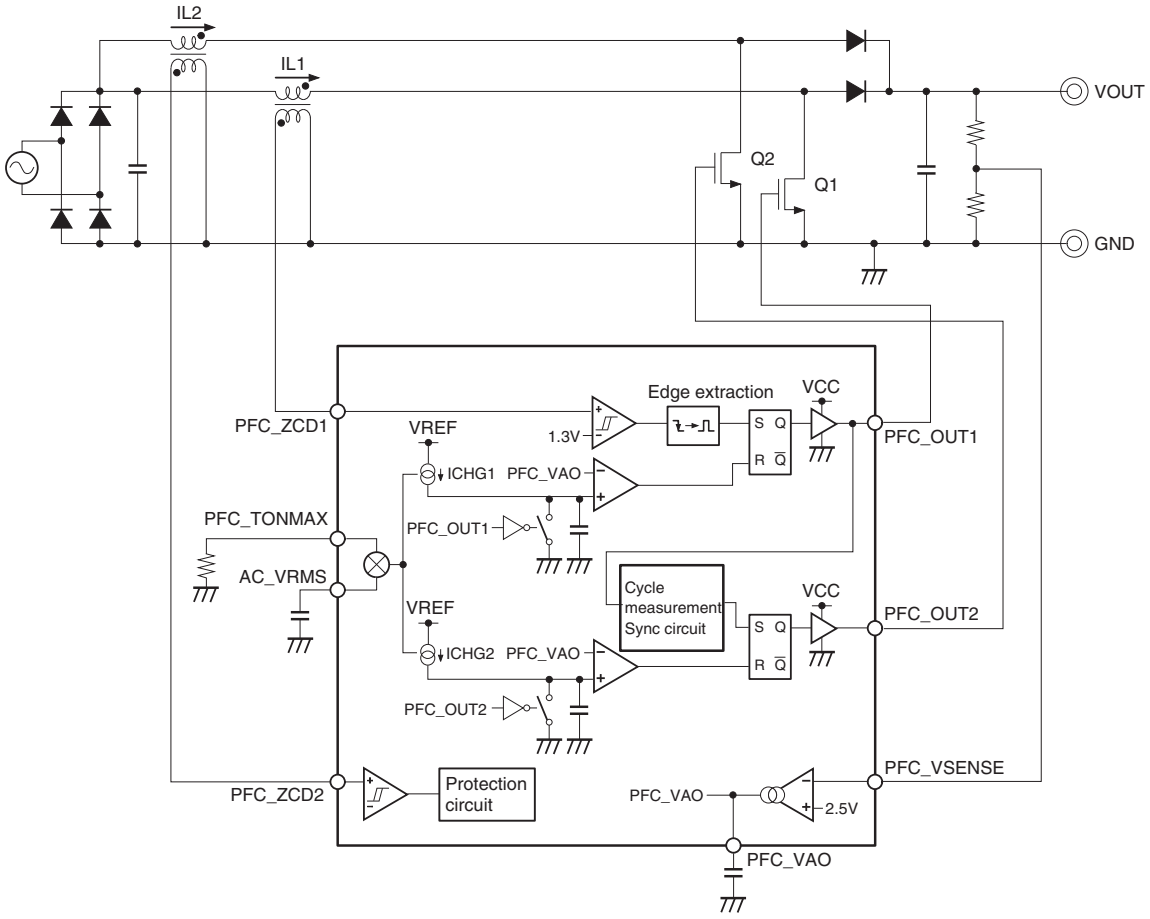


Fig. 6. Interleave PFC Circuit Block Diagram

7. PFC Master Side Control Circuit Block

The master (PFC_OUT1) side operates as a single power-factor correction converter in critical conduction mode. Fig. 7-1 describes an overview of operation.

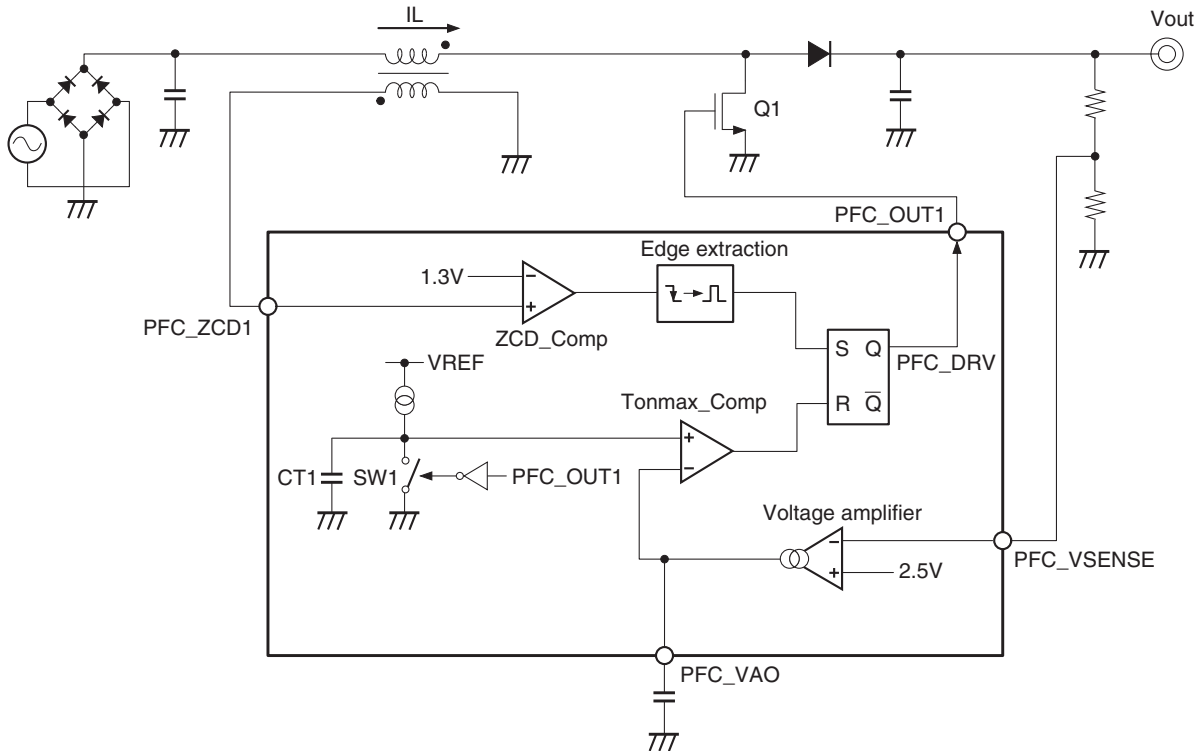


Fig. 7-1. PFC Operation Circuit Block Diagram

This IC performs PFC switching operation in critical conduction mode that applies self-oscillation without oscillator.Fig. 7-2 shows the output waveform of each block in the steady state.

t1 : When MOSFET Q1 goes ON, SW1 goes OFF, and the inductor current (IL) rises from zero at the slope Vin/L. At the same time charging starts to the internal capacitor CT1, and continues until the CT1 voltage reaches the PFC_VAO pin voltage.The PFC_VAO pin voltage value corresponds to the PFC output voltage (Vout).

t2 : When the CT1 voltage reaches the PFC_VAO pin voltage, Tonmax_Comp inverts and a High signal is output, the RESET signal is input to the RS latch circuit, and Q1 goes OFF.When Q1 goes OFF, the inductor voltage inverts, and current is supplied to the output side via the diode.In addition, during this period the inductor current decreases at the slope (Vout – Vin)/L, and a positive voltage is generated in the auxiliary winding (PFC_ZCD pin voltage). The charge stored on the CT1 is discharged instantly by setting SW1 to ON.

t3 : When the inductor current reaches 0A, the inductor voltage drops rapidly, and at the same time the PFC_ZCD pin voltage also drops.When the IC detects that the PFC_ZCD pin voltage has fallen to 1.3V or less, the SET signal is input to the RS latch circuit, Q1 is turned back ON, and operation shifts to the next switching cycle.

Critical conduction mode switching is continued by repeating the above operations. Note that PFC control circuit in critical conduction mode, the switching frequently changes constantly according to the instantaneous value of the AC input voltage.

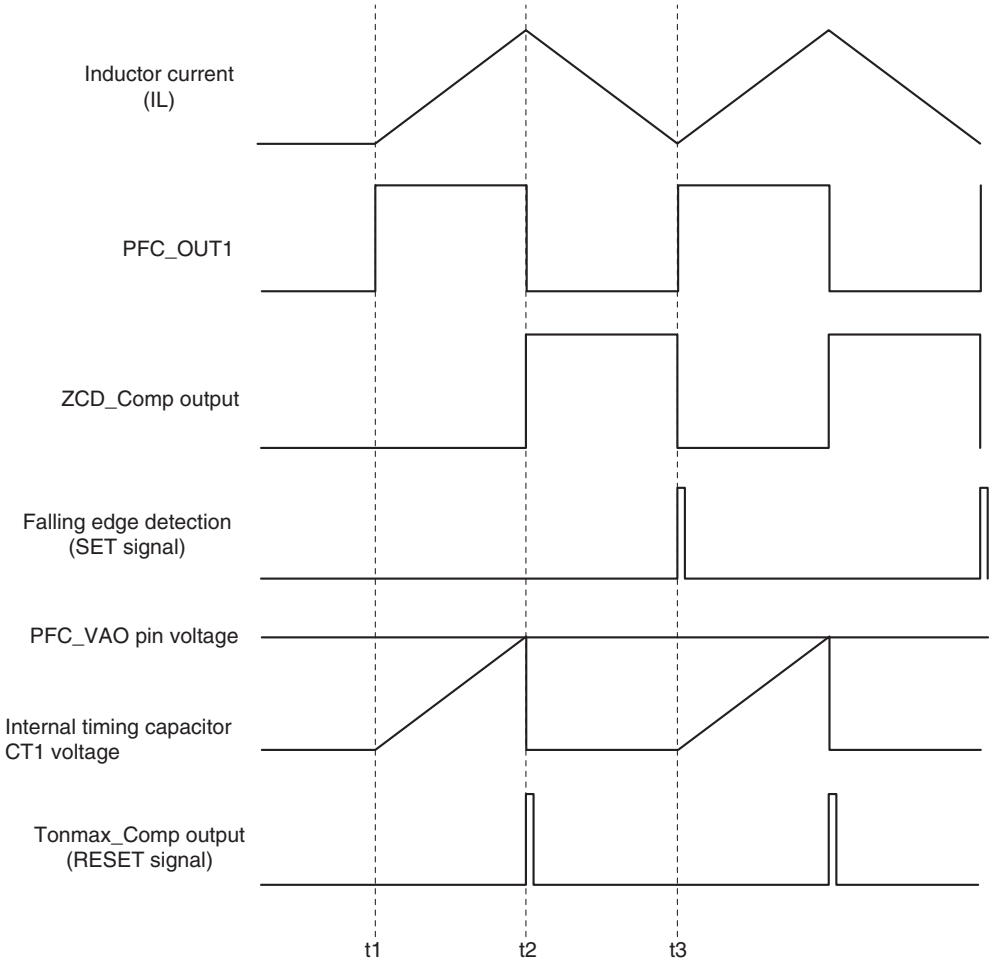


Fig. 7-2. Switching Operation Block Waveforms

8. PFC Slave Side Control Circuit Block

The slave (PFC_OUT2) side is phase controlled to have 180° phase difference to the master (PFC_OUT1) side.Fig. 8 shows the phase control timing chart.
The phase control circuit measures T_{Mn} (n = 1, 2, 3, ...) which is the cycle on master side and it makes the switch on slave side turn on at the timing half of the measured cycle.The measurement of the cycle and the generation of the sync trigger is performed alternatively using the two phase control circuits. The on time on slave side is shorter than that on master side by 5%. To prevent turning on of the switch on slave side before the choke coil current falls to zero is expected on account of this.
In addition, the input signal to the PFC_ZCD2 pin has no effect on the on timing on slave side.This signal is used as measures to secondary failures which are the PFC_OUT1 pin open or MOSFET gate open of the main switch on slave side etc.

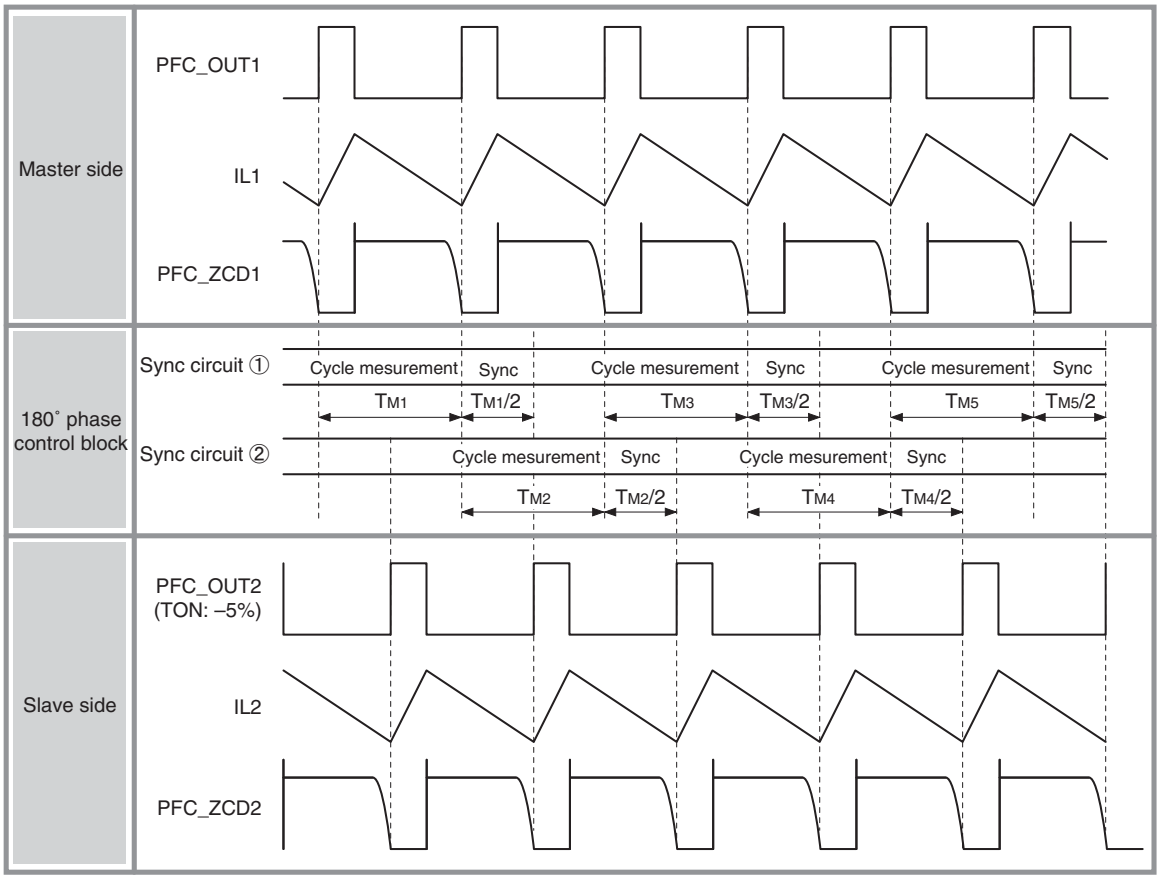


Fig.8 Phase Control Timing Chart

9. PFC Interleave Control Circuit Block

This IC has standby mode and three normal operation modes as described in the item 3. When the PFC is operating in sequence start-up mode or rapid start-up mode, this IC performs interleave control if PFC_VAO > 0.4V. When the load is low, it switches to critical conduction PFC operation in single mode on the master (PFC_OUT1) side only after correspondence to 8ms × 4 times if PFC_VAO < 0.4V. It switches to interleave operation after correspondence to 128μs × 3 times if PFC_VAO > 0.4V again. Fig. 9-1 shows the timing chart to describe this.

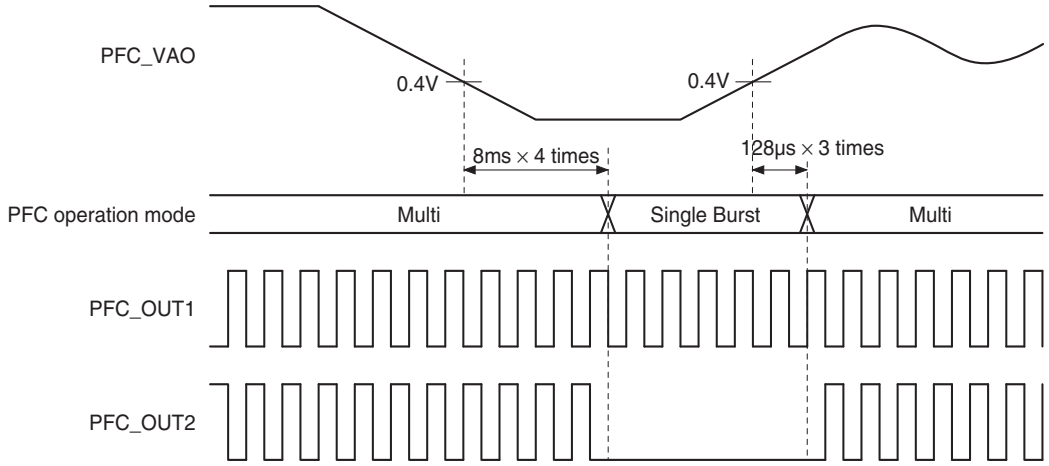


Fig. 9-1. Switching Timing Chart between Single RFC and Interleave PFC

When the PFC starts up, the phase control of the first several pulses may not be stabilized due to the voltage charged in X capacitor of the line filter. To prevent this, when the PFC starts up in sequence stat-up mode or rapid start-up mode and when changing single operation to interleave operation, the period which single operation of 16 pulses is performed is set for master side only. Fig. 9-2 shows the timing chart when interleave operation starts.

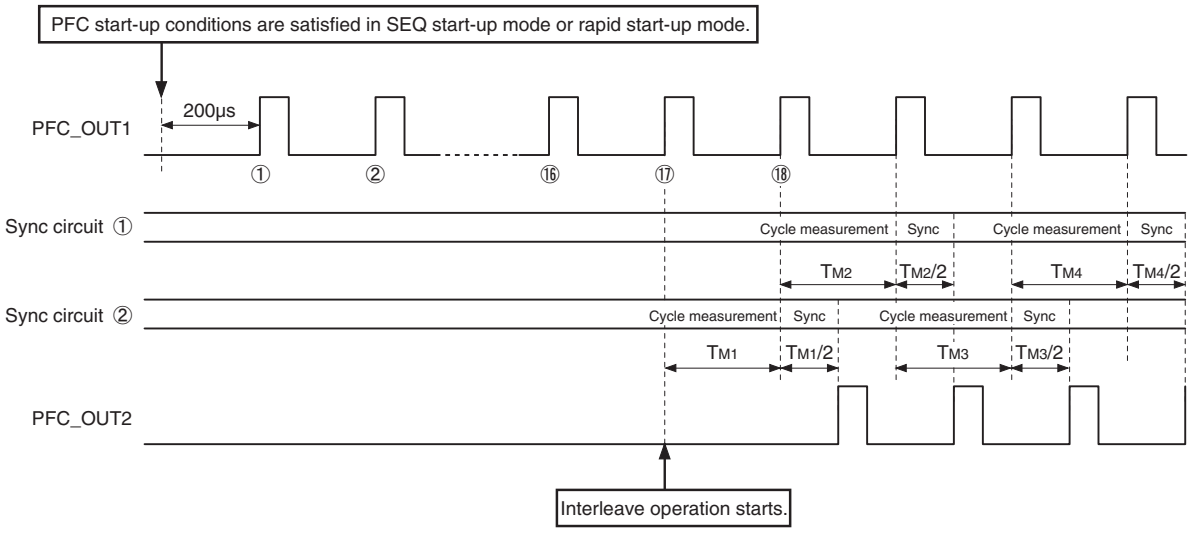


Fig.9-2. Timing Chart when Interleave Operation Starts

In addition, the PFC performs burst operation for master side only and the PFC_OUT2 outputs Low in active standby mode. Fig. 9-3 shows the outline of PFC burst operation in active standby mode.When +B voltage falls to 240V or less is detected PFC operation starts, and when +B voltage rises to 260V or more is detected PFC operation stops.

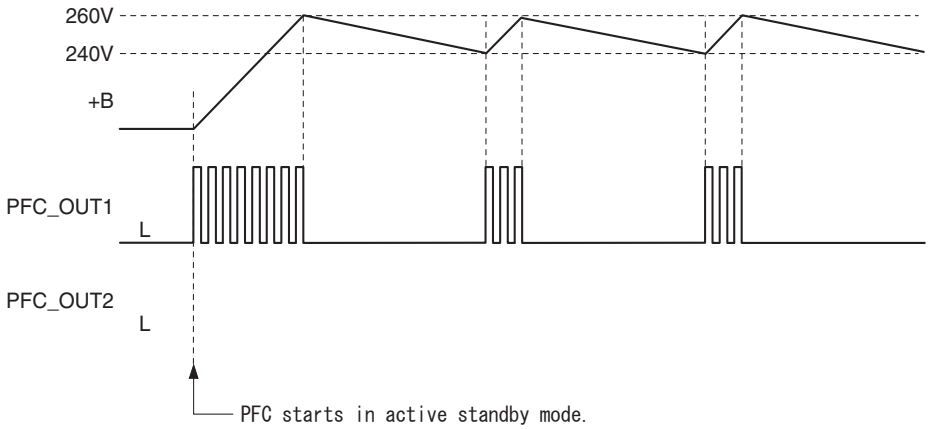


Fig. 9-3. Outline of Single PFC Burst Operation

Fig. 9-4 shows the outline of PFC start-up in active standby mode. IC transitions from standby mode to active standby mode by voltage setting of MODE1 and MODE2 (t1), and PFC starts up after correspondence of 1ms × 3 times when AC_VRMS pin voltage is 1.85V or more (t2). The single PFC burst operation starts for the master (PFC_OUT1) side only after correspondence of 128μs × 3 times when the PFC_VAO pin vlotage is 0.4V or more (t3).The clamp voltage of PFC_VAO is fixed to 1.2V in active standby mode. When IC transitions from active standby mode to sequence start-up mode (t4), the PFC switches from single burst operation to interleave operation if the PFC_VAO pin voltage is 0.4V or more.

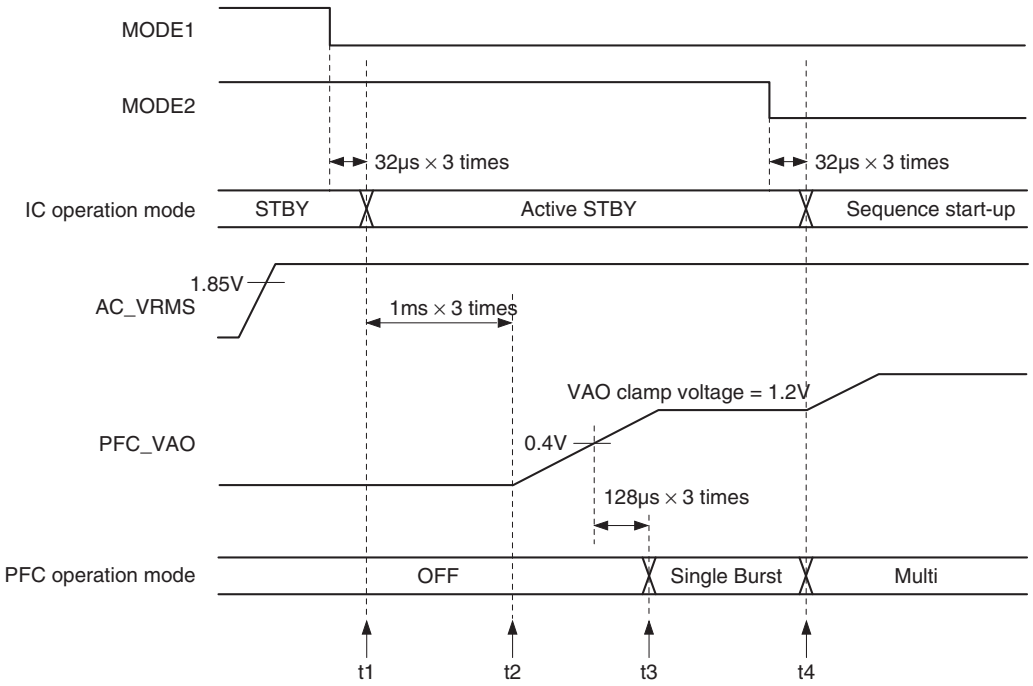


Fig. 9-4 Outline of PFC Start-up in Active Standby Mode

10. PFC Zero Current Detection Circuit Block

The zero current detection circuit performs critical conduction mode operation, so this circuit detects that the inductor current has become 0A. Fig. 10 shows the equivalent circuit diagram in single PFC operation.When the voltage of the inductor auxiliary winding connected to the PFC-ZCD pin is set at the polarity shown in Fig. 10, a positive voltage is generated in the auxiliary winding when MOSFET_Q1 is OFF, and a negative voltage is generated in the auxiliary winding l when MOSFET_Q1 is ON.This auxiliary winding voltage varies greatly according to the input voltage and the circuit configuration, so internal upper limit and lower limit clamp circuits are provided. A resistor (Rzcd) is required to limit the outflow and inflow current to the clamp circuit to ensure normal IC operation.Set the Rzcd value so that this clamp circuit current is ±3mA or less.

Threshold mode control that uses self-oscillation requires a trigger signal to realize stable operation during start-up or under light load conditions.This IC has a restart timer, and when the PFC_OUT output is continuously OFF for 200μs (typ.) or more, the trigger signal is automatically generated and MOSFET_Q1 is turned ON.

In addition, an internal maximum oscillation frequency limit function (Fpfcmax) is provided to prevent the PFC oscillation frequency from rising excessively during abnormal operation when an output diode short-circuit or other overcurrent state is detected.After an overcurrent is detected, the PFC output is forcibly turned OFF using pulse-by-pulse control.In this case, a counter (T_offmin: 4μs (typ.)) that temporarily fixes the PFC output Low operates by overcurrent detection signal. The signal from PFC_ZCD is masked during that period, and a High output pulse is generated after counter operation ends.

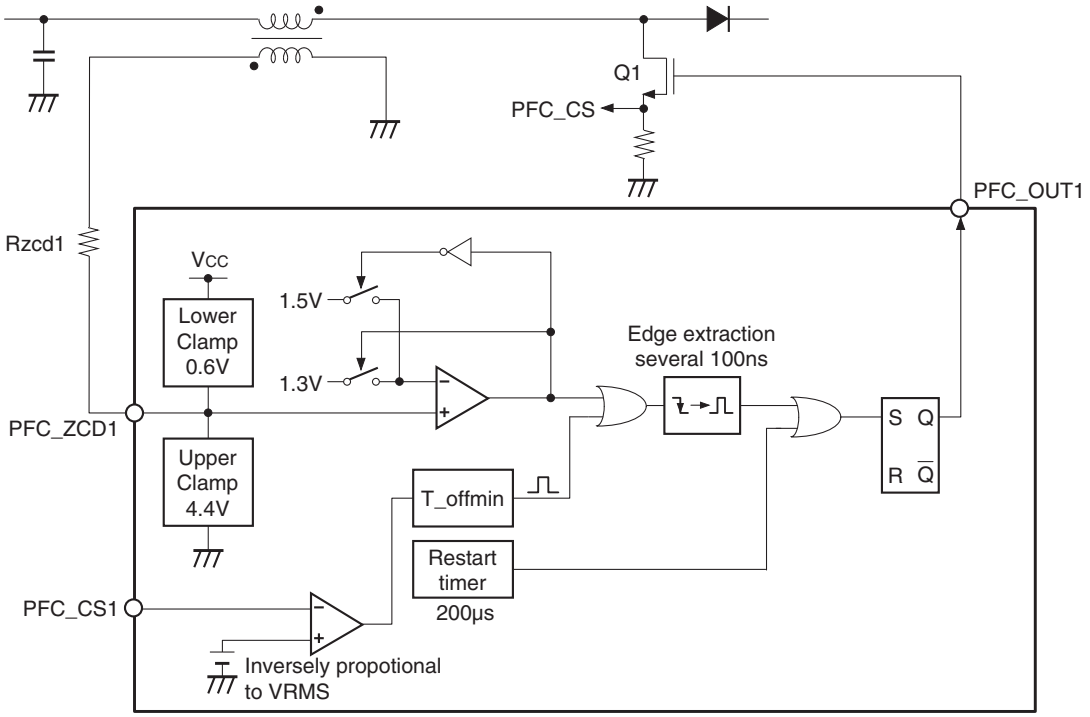


Fig. 10. ZCD Control Block Equivalent Circuit

11. PFC Maximum ON Time Control Circuit Block

The PFC_OUT1, PFC_OUT2 ON time (Tonmax) is determined by the AC_VRMS pin voltage and the resistor (Rt) connected to the PFC_TONMAX pin. Maximum ON time on the master (PFC_OUT1) side is obtained by the following equation.

$$\text{Tonmax}\ [\mu s] = \frac{12.25 \times \text{Rt}\ [k\Omega]}{\text{AC\_VRMS}\ [V]^2} + 0.227$$

When Rt = 5.6kΩ, ACΩVRMS = 2.5V, maximum ON time is 11.20_s (typ.).The maximum ON time on the slave (PFC_OUT2) side is shorter than that on the master side by approx. 5%.In addition, the PFC_OUT pin ON time according to the PFC_VAO pin voltage (Vvao) is obtained by the following equation. The offset voltage (Voffset) is 0.18V (typ.). The ON time on the slave side is shorter than that on the master side by approx. 5%.

$$\text{Ton}\ [\mu s] = \frac{4.344 \times \text{Rt}\ [k\Omega] \times (\text{Vvao} - \text{Voffset})\ [V]}{\text{AC\_VRMS}\ [V]^2} + 0.227$$

The maximum ON time is limited by the reference voltage of 3.0V generated in the IC though the maximum clamp voltage of the PFC_VAO pin is 3.3V (typ.).Fig. 11 shows the equivalent circuit diagram near the PFC_TONMAX pin.

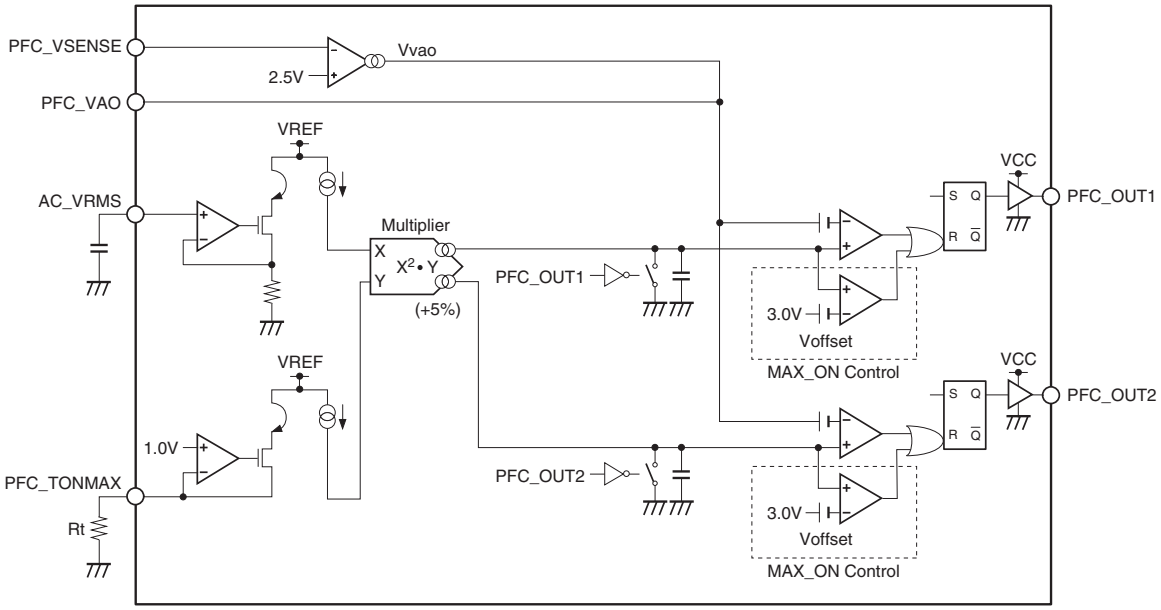


Fig. 11. Maximum ON Time Control Block Equivalent Circuit

12. PFC_VAO Clamp Voltage Control Circuit Block

This IC has a function that limits the power according to overcurrent detection operation as a countermeasure against choke coil and film capacitor squealing due to overcurrent control during startup and AC input voltage sag recovery.
For the PFC_CS1 pin, the threshold (Vthcs1) which is overcurrent detection level and the threshold (Vthdy1) which is dynamic power limit level are set, and the dynamic power limit threshold is set to 95% compared to the overcurrent detection threshold. The clamp value of the PFC_VAO pin vlotage is set to 3.3V in normal operation, and the PFC_VAO pin vlotage is clamped at the previous PFC_VAO pin voltage or lower when the PFC_CS1 pin voltage reaches dynamic power limit level.
The PFC_VAO clamp voltage is selected from the six points from 1.2V to 2.7V increment of 0.3V. When the PFC_CS1 pin voltage does not reach the threshold of dynamic power limit in master side switching cycle, the clamp value is set to the voltage by 0.3V higher at the start of the next cycle, in other words when outputting ON pulse of the PFC_OUT1 pin.
The clamp voltage control operation above is performed every ON pulse output of the PFC_OUT1 pin.
Adjustment of the PFC_VAO pin clamp voltage prevents squealing due to overcurrent detection operation.
For the PFC_CS2 pin on the slave side, the dynamic power limit threshold is not set, and this function operates depending on the master side only. Fig.12 shows the timing chart of clamp voltage control sequence of the PFC_VAO pin.

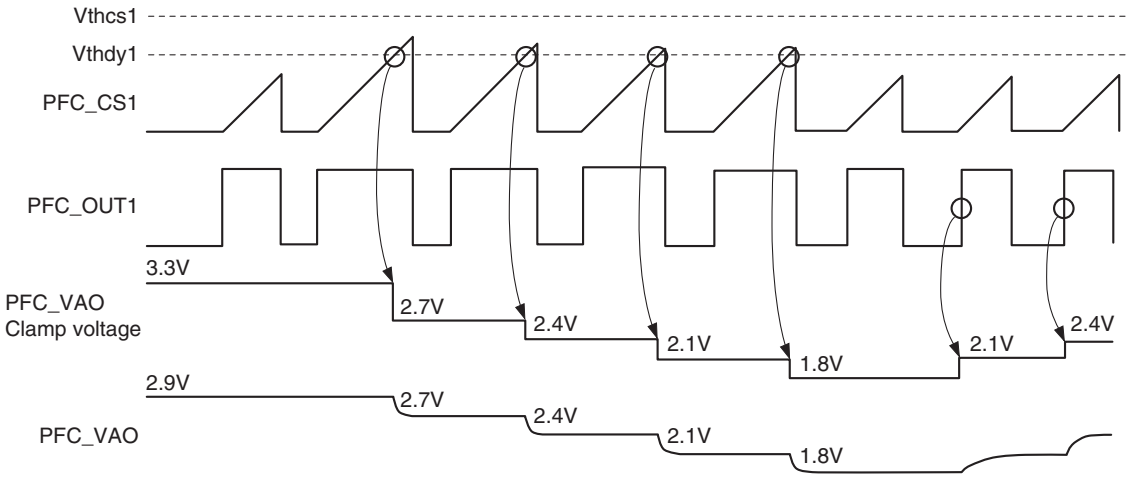


Fig. 12. PFC_VAO Clamp Voltage Cancel Sequence

13. PFC Sequence Control Circuit Block when AC Input Sag Recovery

This IC incorporates PFC recovery sequence control circuit for preventing PFC overcurrent when recovering from AC input voltage sag. If the boost operation of PFC starts while the current is flowing from AC input side to the direction of PFC output when AC recoveried, the MOSFET may have breakdown because the excessive drain current flows into the MOSFET of boost converter. The recovery sequnce control circuit perfoms the following control to avoid such phenomenon.In addition, phenomenon which current flows from AC input side to the direction of PFC output occurs only when the AC input voltage is higher than the PFC output voltage. When the AC input voltage is lower than the PFC output voltage, the PFC operation should be started as soon as possible after AC recover from output voltage hold time point of view. Therefore, the operation of this function varies according to the AC input voltage. This IC takes sampling of the AC_VRMS pin voltage at the moment when changing the AC_DETOUT pin voltage from “H” to “L” by detection of AC OFF. When the AC_VRMS pin voltage is higher than 5.1V (1) control below is enabled, and when the AC_VRMS pin voltage is lower than 5.1V (2) control below is enabled.

(1) When AC input voltage is high (AC_VRMS > 5.1V)

◆ PFC restart timer control

PFC restart timer is disabled so that the MOSFET switching operation does not occur when the AC_DETOUT pin voltage changes to “L”. When the restart timer is enabled again is the timing when the AC_DETOUT pin voltage changes to “H” by detection of the second "C" period after AC recover.

◆ Zero Current Detection Circuit Control by PFC_ZCD1 pin

The zero current detection operation by the PFC_ZCD1 pin is disabled 10ms after the AC_DETOUT pin voltage is “L” and the AC_DETIN pin voltage falls to 1.95V or less so that the PFC operation does not restart by error detection in the zero current detection circuit of choke coil by the PFC_ZCD1 pin when the current flows from the AC input side to the PFC output.When the zero current detection circuit is enabled again is the timing when the AC_DETOUT pin voltage changes to “H” by detection of the second "C" period after AC recover.
In addition, when the AC_DETIN pin voltage rises to 1.95V or more within 10ms after the AC_DETIN pin voltage falls to 1.95V or less, it is regarded as not instantaneous outage of AC input but rapid change of AC input as shown in the Fig. 13-2. This control is not performed because the continued PFC operation is required for limitting decrease of the PFC output voltage as small as possible.

◆ PFC_VAO pin voltage control

The PFC_VAO pin voltage rises and reaches High clamp voltage soon because the PFC output voltage falls when AC input sag occurs.The PFC overcurrent protection may function when the AC input is recovered from this state.In order to avoid this, the PFC_VAO pin voltage is held so that it does not rise more 20ms after the AC_DETOUT pin voltage is “L”. When the hold of the PFC_VAO pin voltage is cancelled is the timing when the AC_DETOUT pin voltage changes to _H“ by detection of the second "C" period after AC recovery.

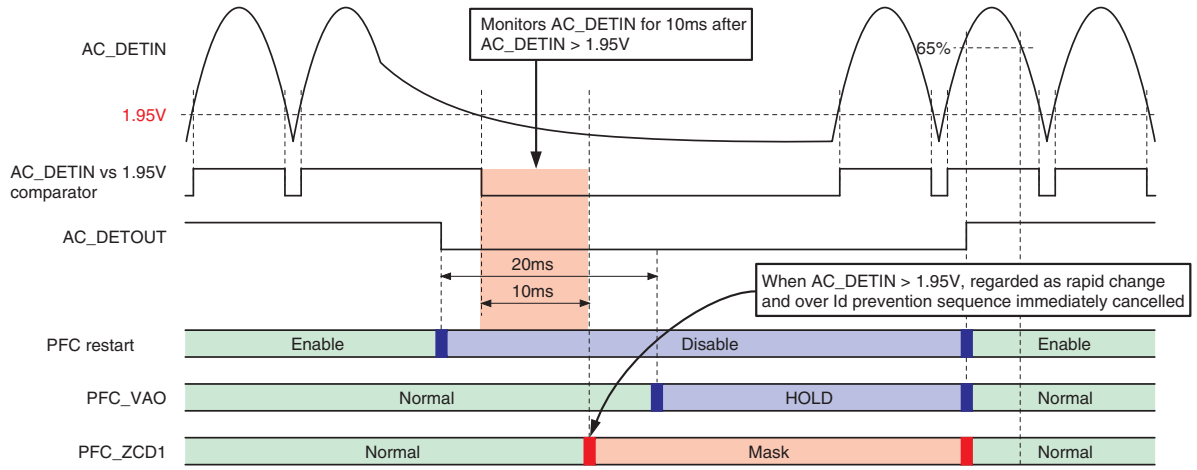


Fig. 13-1. Recovery from Instanteneous Voltage Outage of AC Input 200V

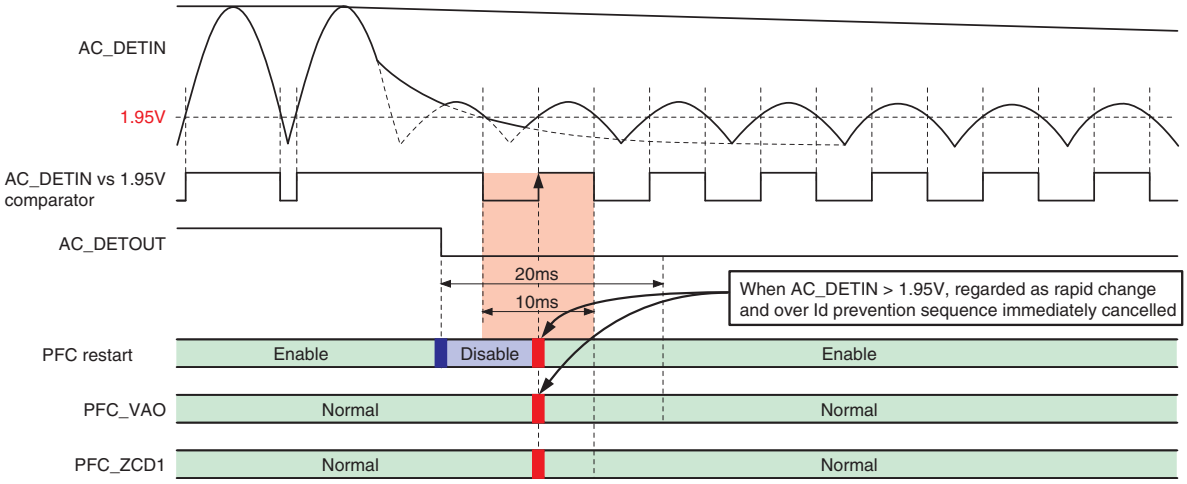


Fig. 13-2. Rapid Voltage Change of AC Input 200V

(2) .When AC input voltage is low (AC_VRMS < 5.1V)

◆ PFC restart timer control

PFC restart timer is disabled so that the MOSFET switching operation does not occur when the AC_DETOUT pin voltage changes to “L”.When the restart timer is enabled again is the timing when the first "C" period is detected after AC recovery.

◆ Zero Current Detection Circuit Control by PFC_ZCD1 pin

When the AC input voltage is low, the zero current detection operation by the PFC_ZCD1 pin is always enabled because the continued PFC operation is required for limitting decrease of the PFC output voltage as small as possible.

◆ PFC_VAO pin voltage control

The PFC_VAO pin voltage is held in order to avoid phenomenon which the PFC overcurrent protection functions when returning from the AC input sag 20ms after the AC_DETOUT pin voltage is “L”. When the hold of the PFC_VAO pin voltage is cancelled is the timing when the first "C" period is detected after AC recovery.

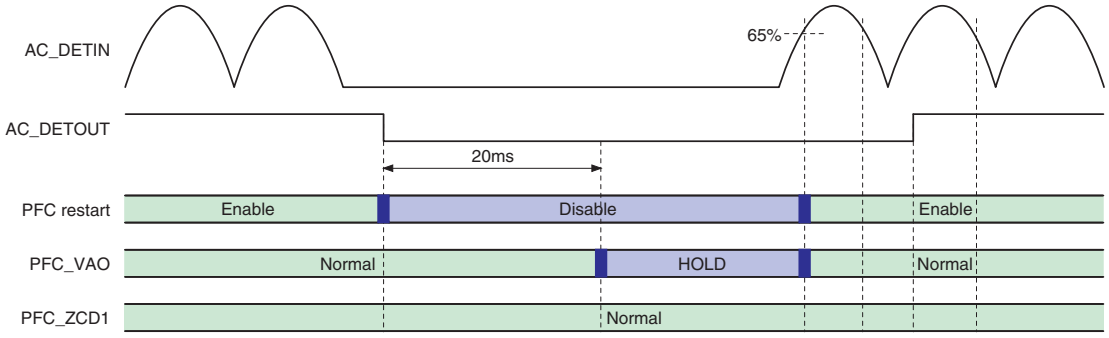


Fig.13-3.

14. PFC Output Voltage Detection Circuit Block

Fig. 14 shows the equivalent circuit the area around the _VSENSE and PFC_OVP pins.

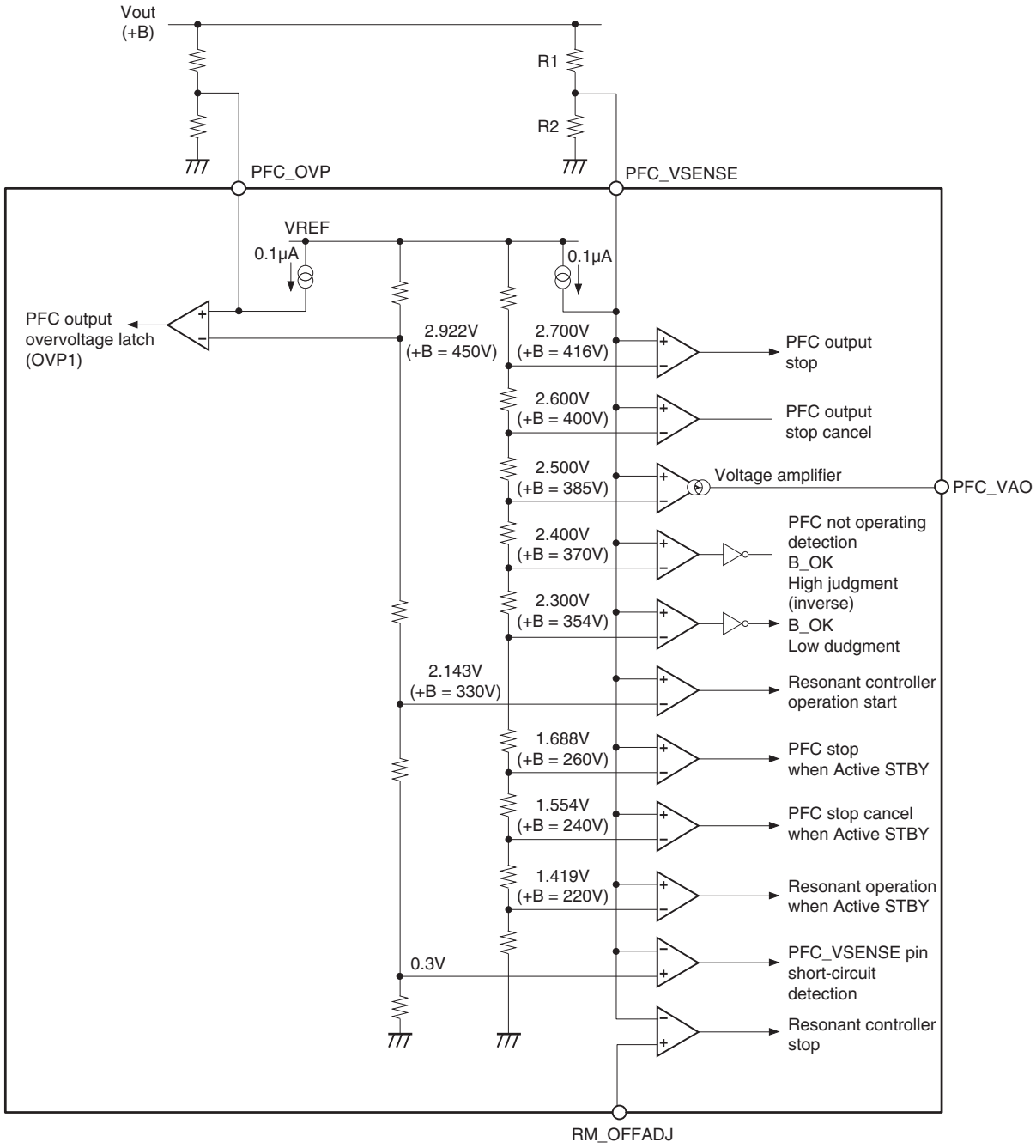


Fig. 14. PFC Output Voltage Detection Block Equivalent Circuit

The PFC_VSENSE pin detects the PFC output voltage, and is also the circuit that performs rise sequence control during start-up, and protects against output voltage fluctuations due to rapid load changes.

- **PFC overvoltage output stop**

  PFC_OUT output is stopped when PFC_VSENSE > 2.7V (+B > 416V) is detected.
  PFC_OUT output is canceled when PFC_VSENSE < 2.6V (+B < 400V) is detected.

- **PFC not operating detection and B_OK pin "H" output level threshold**

  IC latch operation results after PFC×VSENSE < 2.4V (+B < 370V) is detected for 10s (corresponds to 2.1s × 5 times) or more.
  The B_OK pin output goes to "H" when PFC_VSENSE > 2.4V (+B > 370V) is detected.

- **B_OK pin "L" output level threshold**

  The B_OK pin output goes to "L" when PFC_VSENSE < 2.3V (+B < 354V) is detected.

- **Resonant controller operation start**

  Resonant controller operation is started when PFC_VSENSE > 2.143V (+B > 330V) is detected.

- **Resonant controller stop**

  Resonant controller operation is stopped when PFC_VSENSE < RM_OFFADJ is detected.

- **PFC burst control in active standby mode**

  PFC_OUT output is stopped when PFC_VSENSE > 1.688V (+B > 260V) is detected.
  PFC_OUT output is canceled when PFC_VSENSE < 1.554V (+B < 240V) is detected.

- **Resonant controller operation start voltage in active standby mode**

  Resonant controller operation is started when PFC_VSENSE > 1.419V (+B > 220V) is detected.
  Resonant controller operation is stopped when PFC_VSENSE > 1.419V (+B > 220V) is detected.

- **PFC_VSENSE pin open/short-circuit detection**

  It stops PFC_OUT output when PFC_VSENSE < 0.3V is detected by open of resistor R1, short-circuit of resistor R2, etc.In addition, when the PFC_VSENSE pin is open, the pin voltage is forcibly pulled up by the internally supplied 0.1µA constant current, and the IC is latched when PFC_VSENSE > 2.922V is detected.

The PFC_OVP pin is a protective pin for when a PFC_VSENSE pin abnormality occurs.PFC_VSENSE pin, the PFC_OVP pin detects the PFC output voltage, and has only an overvoltage protection function.The detection voltage of PFC_OVP pin is the same as the detection voltage of PFC_VSENSE, and the reference voltage is set from the same resistor ladder.

- **PFC overvoltage latch (PFC_OVP pin)**

  IC latch operation results after FC_OVP > 2.922V (+B > 450V) is detected.

- **PFC_OVP pin open detection**

  When the PFC_OVP pin is open same as the PFC_VSENSE, the pin voltage is forcibly pulled up by the internally supplied 0.1µA constant current, and the IC is latched when PFC_OVP > 2.922V is detected.

◆ Resonant Controller Block

15. Oscillator Block

15-1. Oscillator Circuit Block

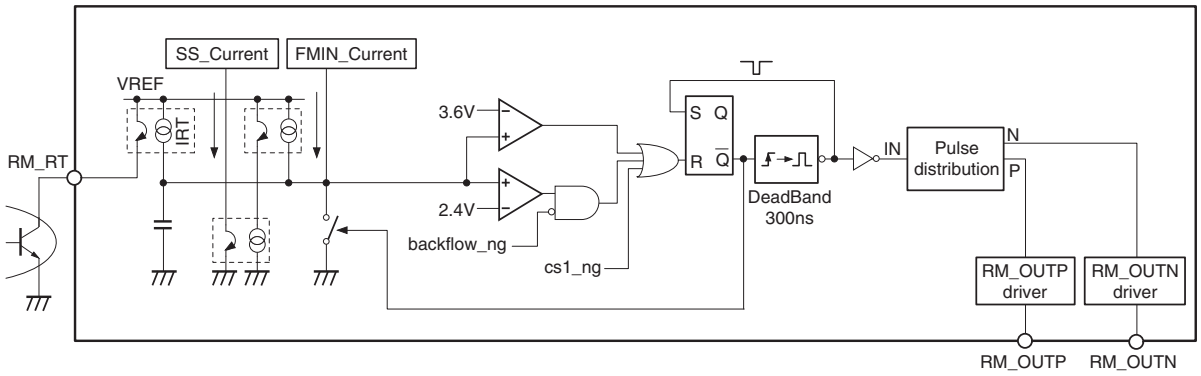


Fig. 15-1. Oscillator Equivalent Circuit

Fig. 15-1 shows the equivalent circuit for oscillator circuit.
Outputs of some current mirror circuits are connected to internal timing capacitor, discharge switch , and positive input of comparator. The resonant oscillation frequency is determined by the current led from the RM_RT pin, the current from the minimum frequency setting circuit, and the current from the soft start circuit. The deadband width is fixed internally to 300 ns.
The Fig. 15-2 graph shows the resonant oscillation frequency characteristics at a minimum frequency setting of 60kHz, relative to the current led from the RM_RT pin.

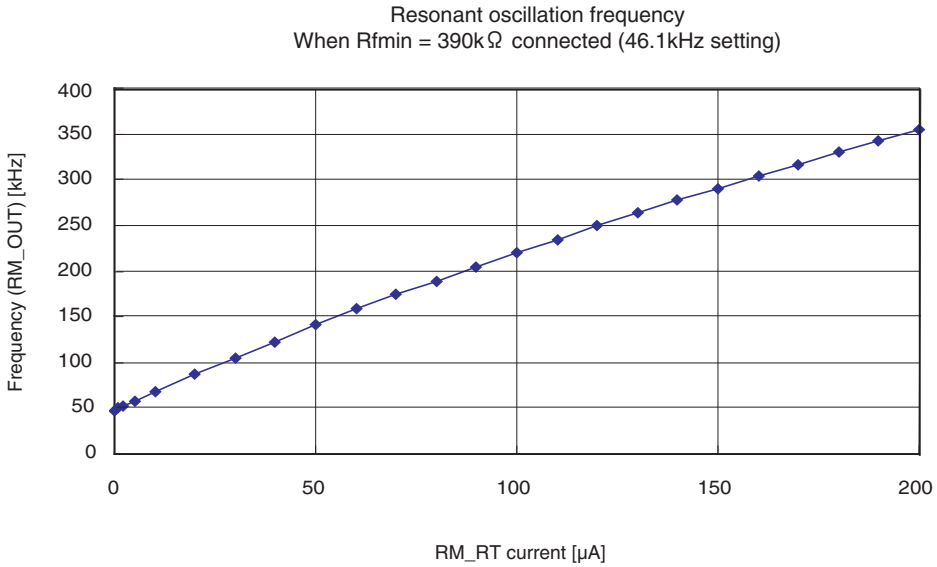


Fig. 15-2. Resonant Oscillation Frequency

15-2. Minimum Frequency Setting Circuit Block

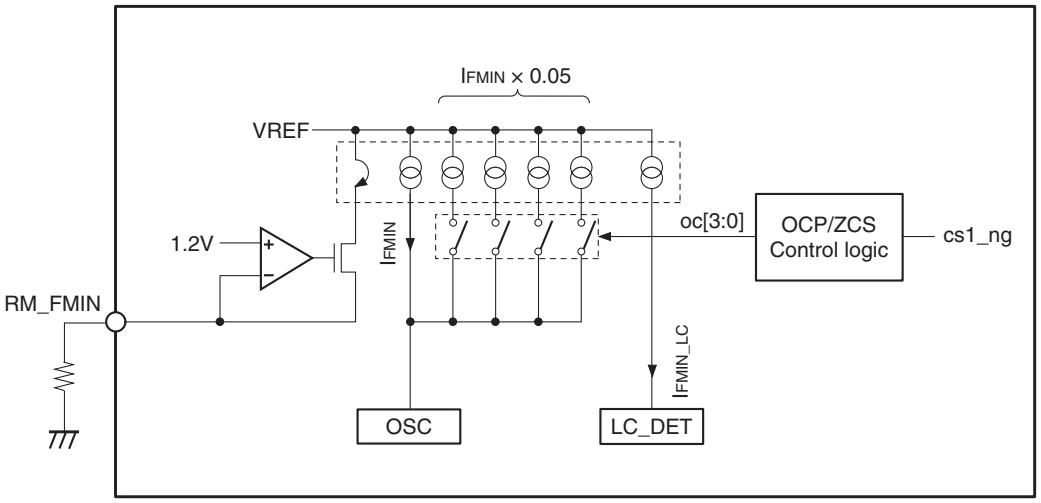


Fig. 15-3. Minimum Frequency Control Block Equivalent Circuit

Fig. 15-3 shows the minimum frequency control block equivalent circuit.
The minimum frequency can be set by externally connecting a resistor to the RM_FMIN pin. The Fig. 15-4 graph shows the minimum frequency characteristics relative to the external resistor value.

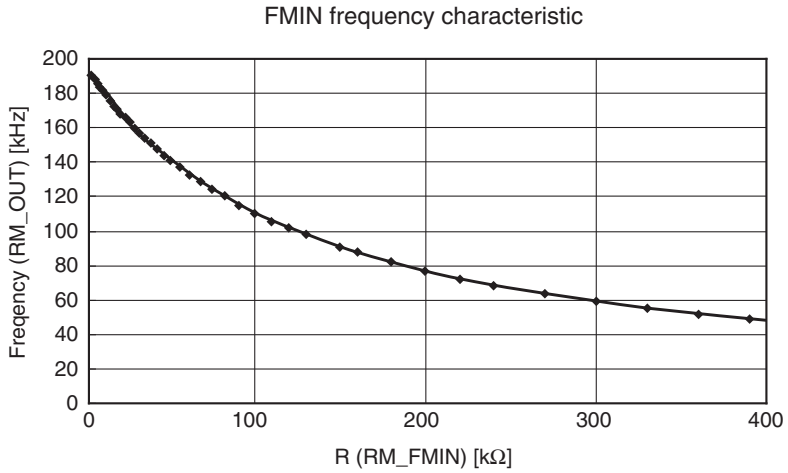


Fig. 15-4. Minimum Oscillation Frequency Setting

The minimum oscillation frequency decreases when the RM_FMIN pin is left open or the current led from the pin decreases. IC latch operation forcibly results when the current led from the pin is detected as being continuously 1.25μA or less (LC_DET) for 6s (2.1s × 3 times).This pin voltage is equivalent to 925kΩ if it is converted into a resisor value connected to the pin. Connect a resisitor of 700kΩ or less to the RM_FMIN pin making allowance for unevenness of the IC characteristics.

15-3. Soft Start Circuit Block

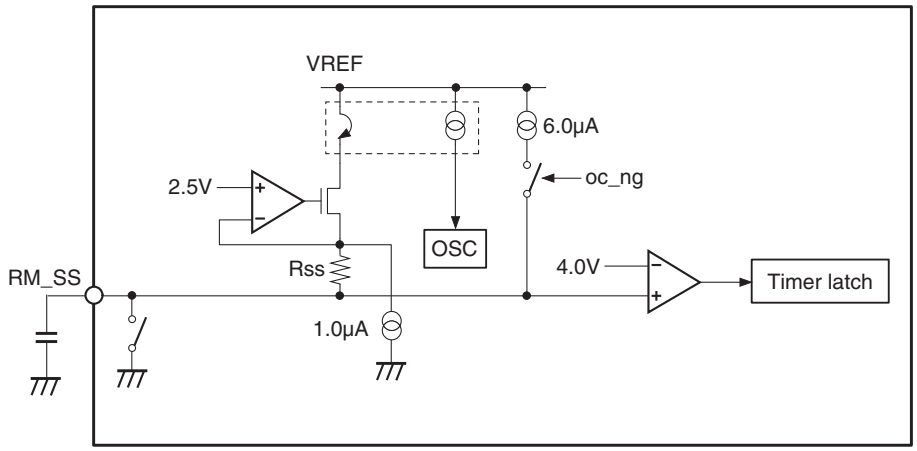


Fig. 15-5. Soft Start Circuit Block Equivalent Circuit

Fig. 15-5 shows the soft start block equivalent circuit.
The soft start circuit feeds back the current, determined by the internal 2.5V output, the internal resistor (Rss), and the external capacitor, to the oscillator of the resonant controller. The resistor value of Rss is 400kΩ in active standby mode, and 250kΩ in sequence start-up mode and rapid start-up mode.In addition, the maximum frequency during soft start is limited to 4 times (max.) the minimum frequency determined by the RM_FMIN pin external resistor. Note that the frequency other than during soft start is not limited to 4 times the minimum frequency. In these cases the frequency is controlled according to the current led from the RM_RT pin.The Fig. 15-6 graph shows the resonant oscillation frequency characteristics during soft start.

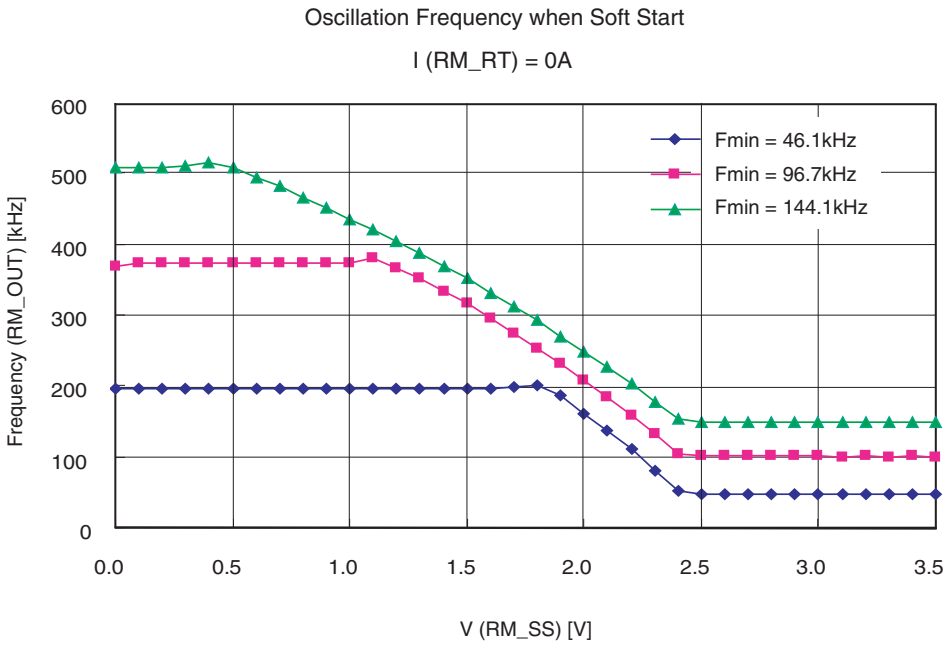


Fig. 15-6. Resonant Oscillation Frequency during Soft Start

16. Overcurrent Detection Circuit Block

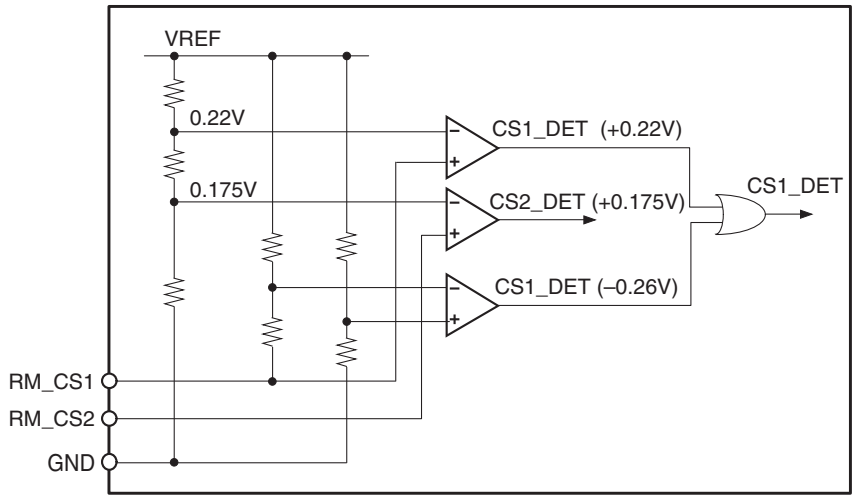


Fig. 16-1. Overcurrent Detection Circuit Block

Fig. 16 shows the resonant overcurrent detection block equivalent circuit. The voltage between the RM_CS1 and RM_CS1GND pins is monitored, and overcurrents in both the positive (+0.22V) and negative (-0.25V) directions are detected according to RM_OUTP and RM_OUTN pin operation.When the PFC output voltage falls (PFC_VSENSE < 2.143V), the overcurrent threshold voltage switch to 1.15 times normal operation both positive and negative directions. The positive threshold results +0.253V and the negative threshold results –0.299V. Operation in overcurrent detection mode is as shown in Fig. 16-2. When an overcurrent is detected, regardless of positive or negative direction, the output pulse is forcibly turned off by pulse-by-pulse control. In addition, when an overcurrent is detected, the minimum oscillation frequency is controlled to 1.2 times the setting value.Thereafter, the minimum oscillation frequency limit changes in the order of 1.2 times ⇒ 1.15 times ⇒ 1.1 times ⇒ 1.05 times ⇒ 1.0 times the setting value with each dead band pulse, and control is performed to return to the original setting frequency with each pulse (4 steps). The minimum oscillation frequency is controlled to 1.2 times the setting value in this manner each time an overcurrent is detected again during the frequency limit period.In addition, in overcurrent detection mode, the capacitor connected to the RM_SS pin is charged by approximately 5.0μA, and when the RM_SS pin voltage reaches 4.0V (128μs × 5 times), the IC is NG latched and the output goes off (both the RM_OUTP and RM_OUTN pins output Low). (Timer latch operation)Approx. 1.0μA is constantly discharged from the RM_SS pin to the inside of the IC, so when the overcurrent is canceled partway, the RM_SS pin is discharged until the clamp voltage is reached.

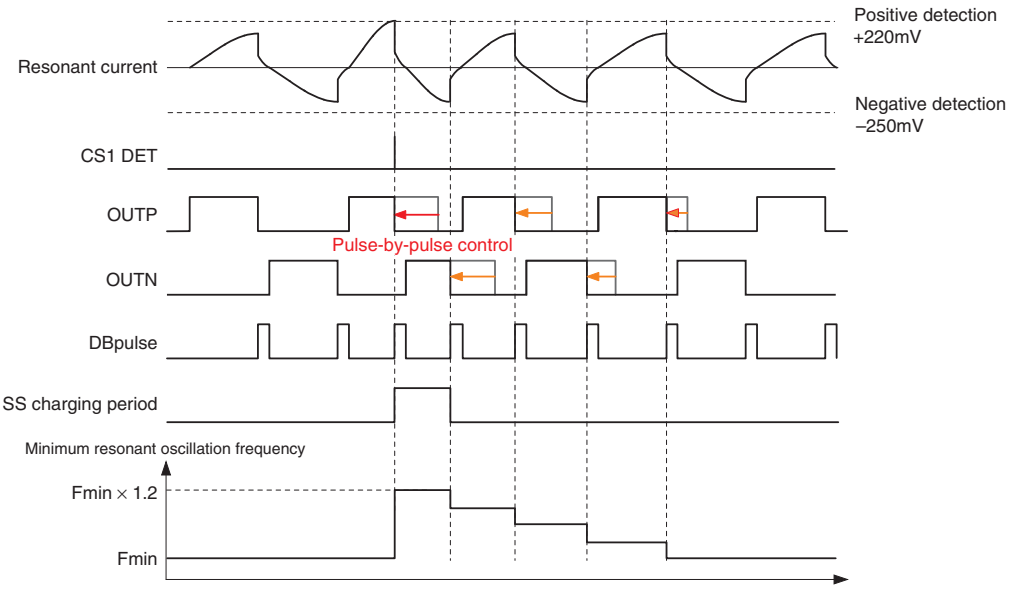


Fig.16-2. Operating Waveform in Overcurrent Detection Mode

Fig. 16-1 also shows the continuous pulse overcurrent detection (CS2_DET: +0.175V detection) circuit by monitoring the voltage between the RM_CS2 –and RM_CS2GND.Continuous overcurrent detection mode operation differs from the operation shown in Fig. 16-2, and instead normal operation continues.When CS2 overcurrent detection continues for approximately 10s (set up by 2.1s × 5 times), NG latch results and the IC forcibly stopped. When CS2 overcurrent is not detected for even one cycle during the approximately 10s count, the counter is reset. Then, when an overcurrent is detected again, the 10s counter starts from zero.

17. Resonant Circuit Stop Voltage Detection Block

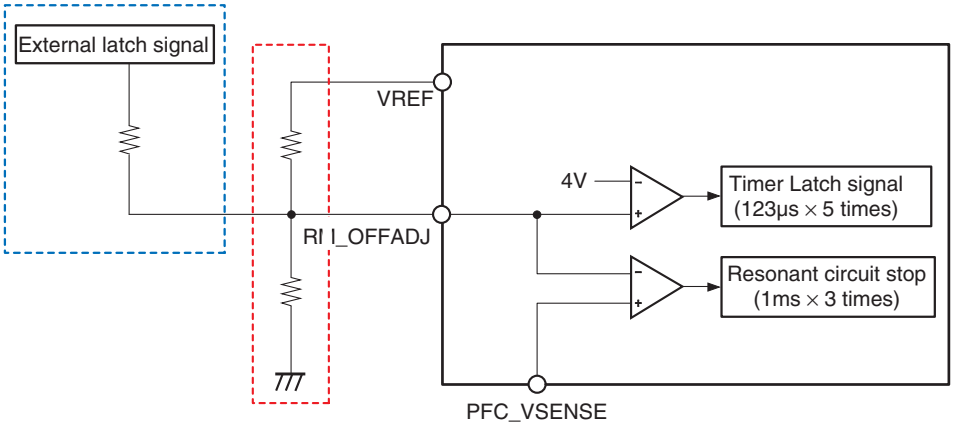


Fig. 17. RM_OFFADJ Pin Internal Equivalent Circuit

Fig. 17. shows the RM_OFFADJ pin internal equivalent circuitThe RM_OFFADJ pin is the threshold voltage setting pin to stop the resonance circuit when the PFC output voltage falls. The resonance circuit stops when the PFC_VSENSE pin voltage falls to the RM_OFFADJ pin voltage or less. The stop voltage can be set by the VREF devided voltage circuit by an external resistor enclosed by the red dotted line in Fig. 17.

Note) When the PFC output voltage is set to 385V (PFC_VSENSE = 2.5V) and the RM_OFFADJ pin is input 1.883V, the resonant circuit is stopped when the PFC output voltage falls to 290V or less (1ms × 5 times).

The RM_OFFADJ pin has an error latch detection function that activates at 4.0V or more, so the IC can be forcibly set to latch operation using the secondary side overvoltage detection or other signal by externally adding the circuit enclosed by the blue dotted line in Fig. 17.

18. NG Latch Operation

◆ PFC overvoltage latch

Latch operation results after PFC_OVP > 2.922V (+B > 450V) is detected and set up by 1ms × 3 times.

Note) The overvoltage detection does not function when PFC_VSENSE > 2.922V.
In addition, PFC_VSENSE > 2.700V (+B > 416V) overvoltage detection does not result in latch operation, and PFC output stops.

◆ PFC continuous overcurrent detection latch

IC latch operation results when a pin abnormality such as PFC_VAO pin open or PFC_TONMAX pin shortcircuited to GND occurs, and the overcurrent detection state is continuously detected due to abnormal PFC oscillation. When a PFC overvoltage is detected 4 times or more per commercial half cycle during AC detection operation, this is counted as one NG time. Latch operation results when the 2.1s counter detects this NG state 5 consecutive times.

◆ PFC continuous dynamic power limit latch

Latch operation results when detecting consecutively the state of dynamic power limit enabled by the detection method same as the PFC continuous overcurrent detection latch.

◆ PFC not operating detection latch

When a pin abnormality such as PFC_OUT pin open occurs, the AC input voltage is high, and the load is light, the PFC output voltage (+B voltage) maintains the high state, and the resonant circuit continues to operate. To avoid this phenomenon, latch operation results when PFC_VSENSE < 2.4V (+B < 370V) is continuously detected for 2.1s × 5 times.

◆ PFCZCD1 protection latch

When normal zero current detection of the choke coil is not performed due to the PFC_ZCD1 pin open or FET gate open on the master side, latch operation results after continuous state is detected by the PFC restart timer and set up by 2.1s × 5 times.
Sampling for detecting abnormal state is performed in the period only when detecting "C" period in the AC detection operation because zero current detection may not be performed when the phase angle of AC input voltage is near 0° and 180°. In addition, protection latch operation does not result when the AC input is high (VRMS pin voltage is 7.0V or more) and VAO pin voltage is 0.4V or less because of the same reason.

◆ PFCZCD2 protection latch

When normal zero current detection of the choke coil on the slave side is not performed due to the PFC_ZCD2 pin open or FET gate open on the master side, latch operation results after detection of the state which zero current is not detected by the PFC_ZCD2 pin and set up by 2.1s × 5 times in order to avoid phenomenon of continuous operation by the master side only.
Sampling for detecting abnormal state is performed in the period only when detecting "C" period in the AC detection operation because zero current detection may not be performed when the phase angle of AC input voltage is near 0° and 180°.In addition, protection latch operation does not result when the AC input is high (VRMS pin voltage is 7.0V or more) and VAO pin voltage is 0.4V or less because of the same reason.

◆ Resonant overcurrent timer latch

When RM_CS > 0.22V or RM_CS < -0.25V is detected, the RM_SS pin is charged by a charging current of 5.0μA. Latch operation results after RM_SS > 4.0V is detected and set up by 128μs × 5 times.

◆ Resonant continuous overcurrent latch

Latch operation results after RM_CS > 0.175V is detected continuously and set up by 2.1s × 5 times.

◆ TSD (IC overheat) latch

Latch operation results after a chip temperature of approximately 140°C is detected and delay time of approximately 30μs due to analog circuit.

◆ RM_OFFADJ latch

Latch operation results after RM_OFFADJ > 4.0V is detected and set up by 128μs × 5 times.

◆ Other latch

Latch operation results after any of the following operations are detected and set up by 2.1s × 3 times.

- VREF_OVLO detection 5.5V or more
- PFC_VAO pin overcurrent detection 80μA or more
- PFC_ZCD clamp circuit overcurrent detection +6.0mA or more, –6.0mA or less
- PFC_VSENSE short-circuit detection 0.3V or less
- RM_FMIN pin low current 10μA or less

Circuit operation stops after NG latch other than latch due to TSD, but the VREF pin continues to output High, and the AC detection function remains enabled.In addition, the B_OK outputs Low.NG latch is canceled by transitioning to standby mode.During TSD latch the VREF pin outputs Low, and the TSD latch state is canceled only by turning the IC power off and on again, or by detecting VCC UVLO (VCC < 9.6V).

Timing Chart

PFC → Resonant controller startup sequence

◆ Sequence start-up mode

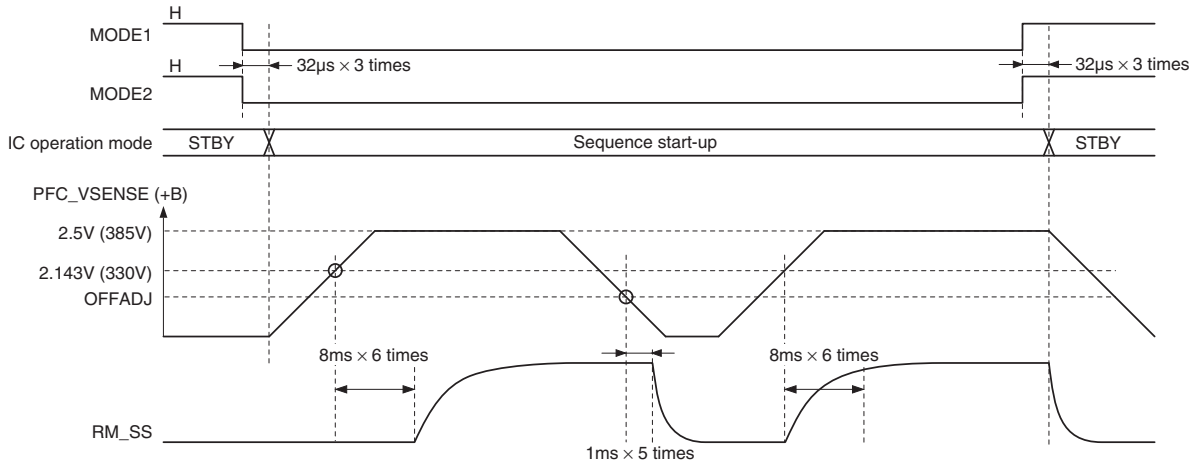


Fig. 18. Start-up Waveform in Sequence start-up mode

(* The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.)

◆ Rapid start-up mode

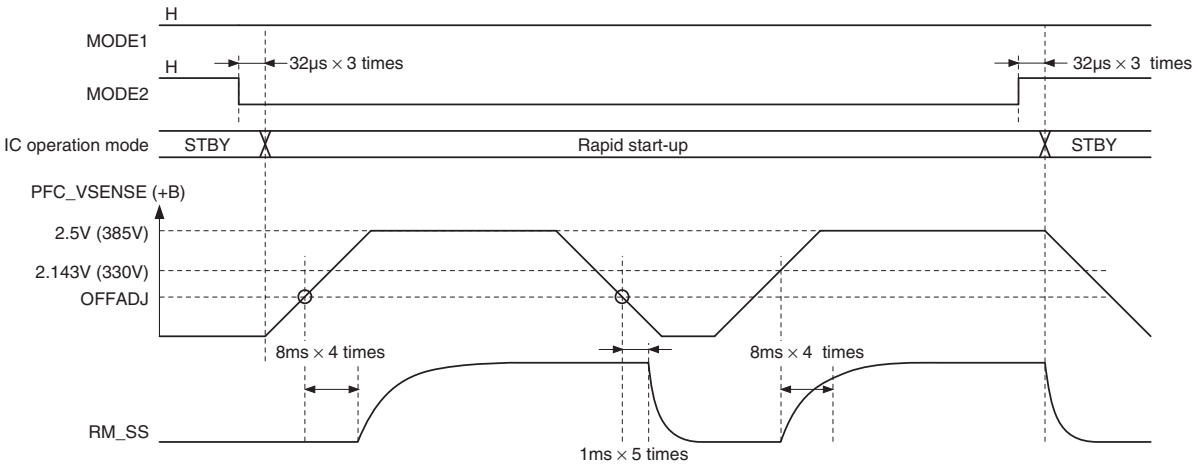


Fig. 19. Start-up Waveform in Rapid Start-up Mode

(* The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.)

◆ Active standby mode

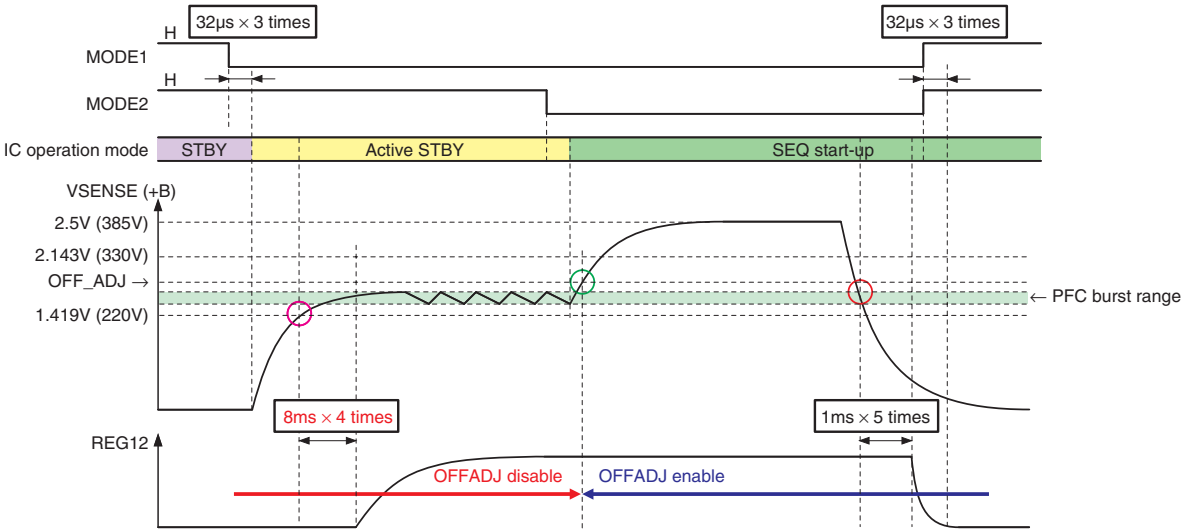
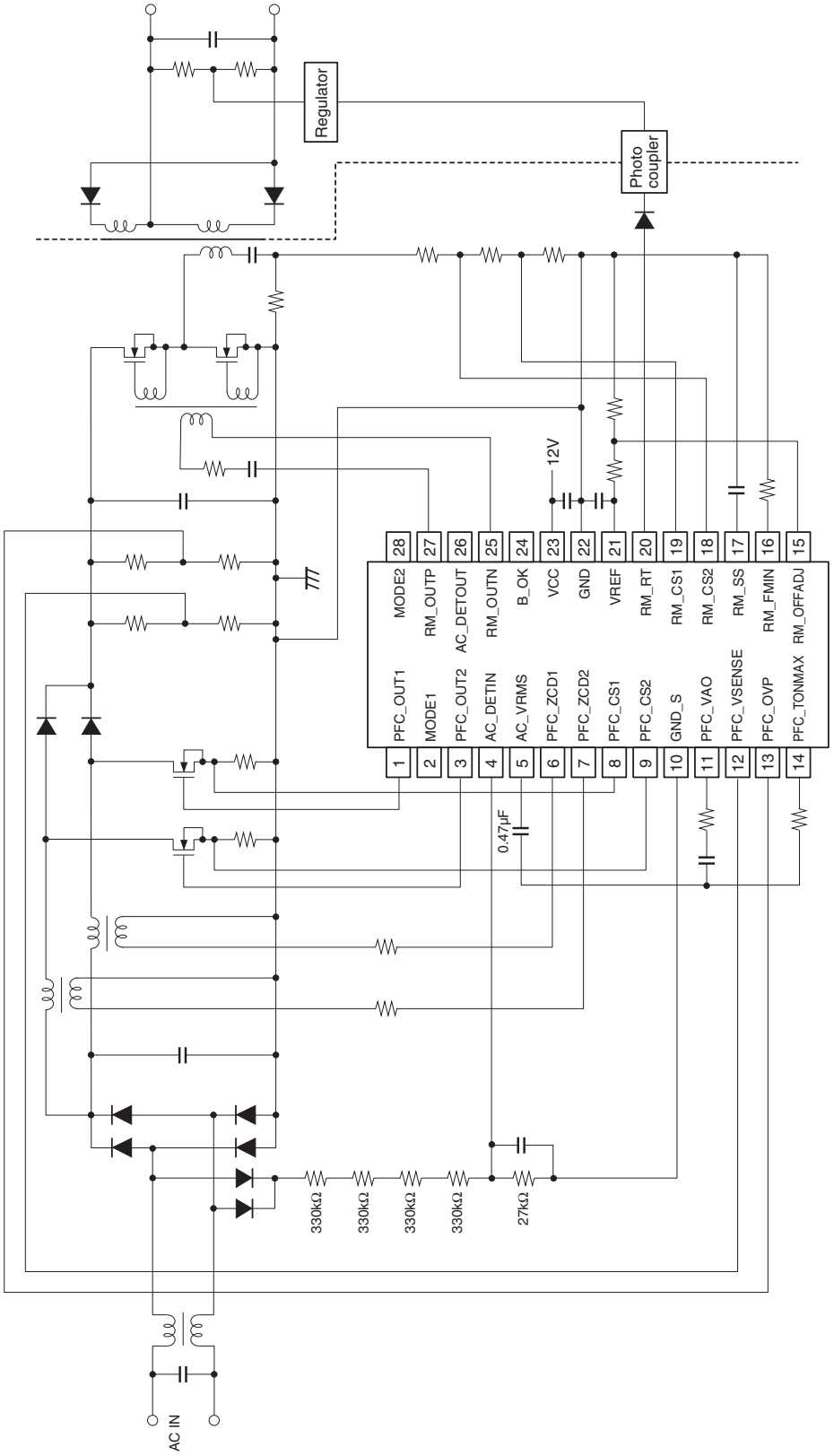


Fig. 20. Start-up Waveform in Active Standby Mode

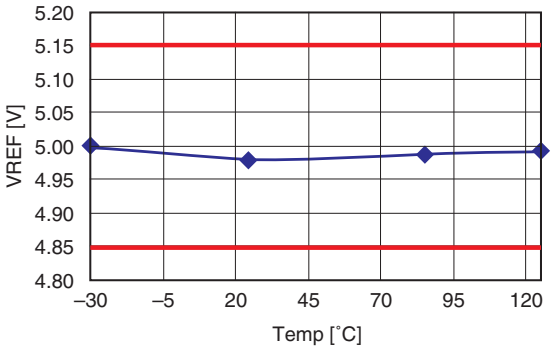
(* The +B voltage shows an example of setting that PFC_VSENSE = 2.5V when +B = 385V.)

Application Circuit

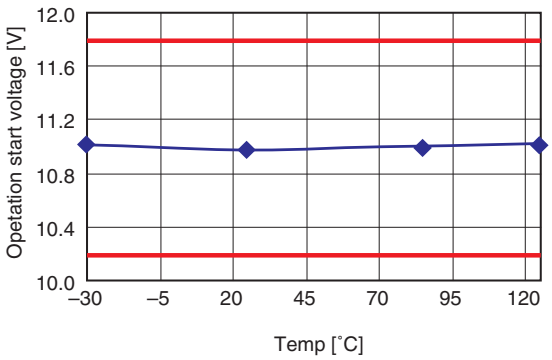


Example of Representative Characteristics

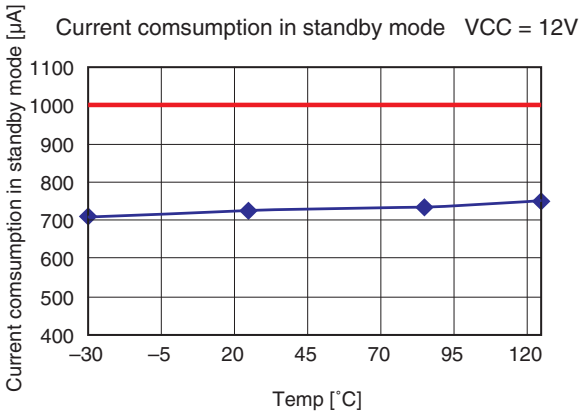
VREF output voltage VCC = 12V



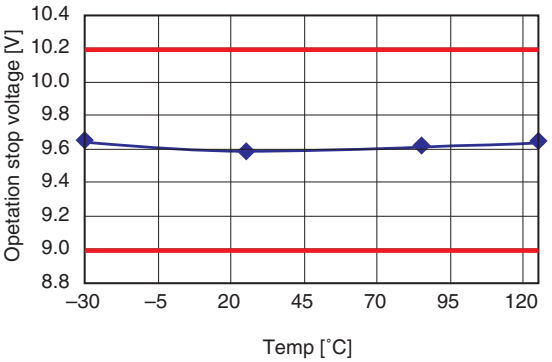
VCC_UVLO opetation start voltage



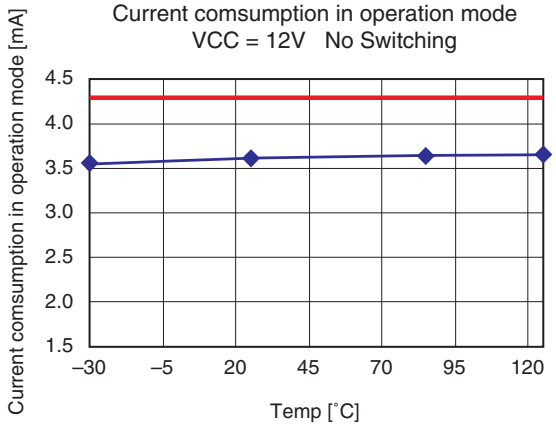
Current comsumption in standby mode VCC = 12V



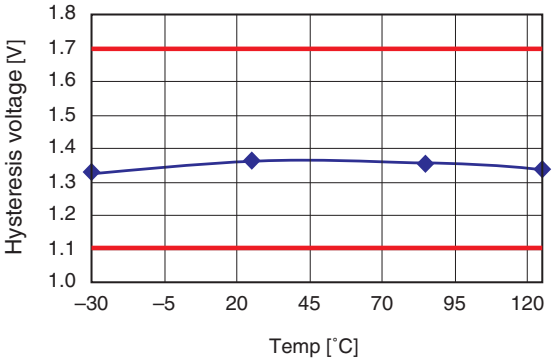
VCC_UVLO opetation stop voltage



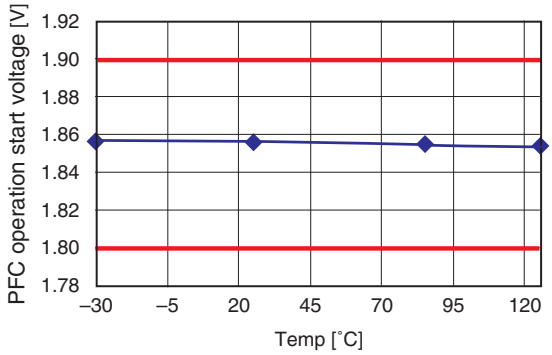
Current comsumption in operation mode
VCC = 12V No Switching



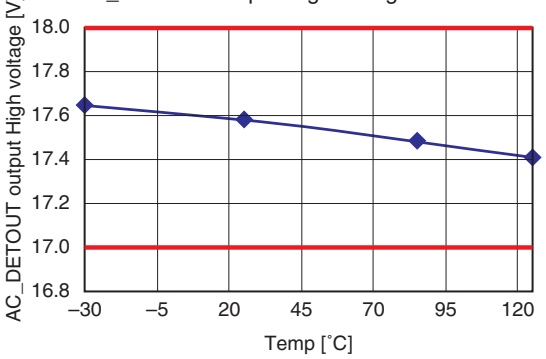
VCC_UVLO hysteresis voltage



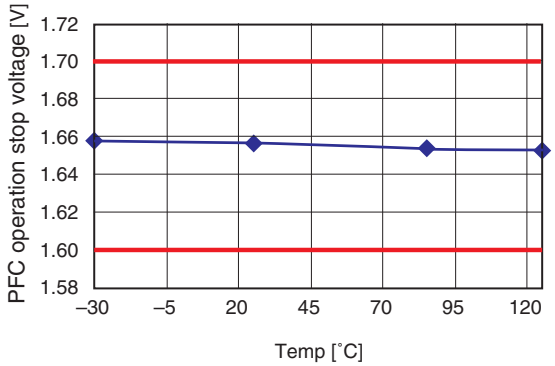
PFC operation start voltage



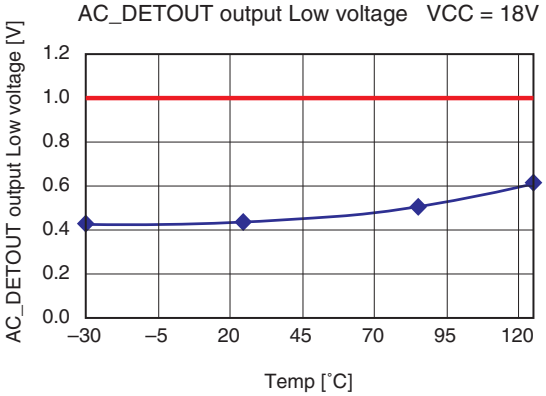
AC_DETOUT output High voltage VCC = 18V



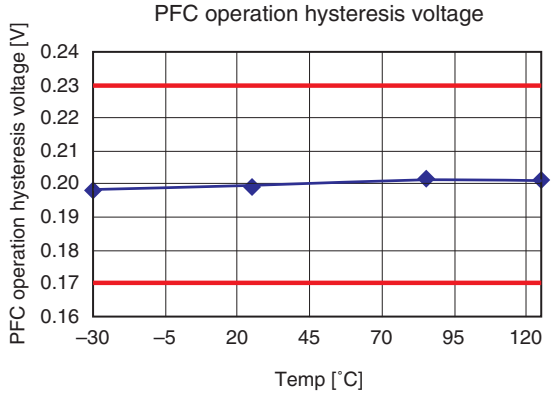
PFC operation stop voltage



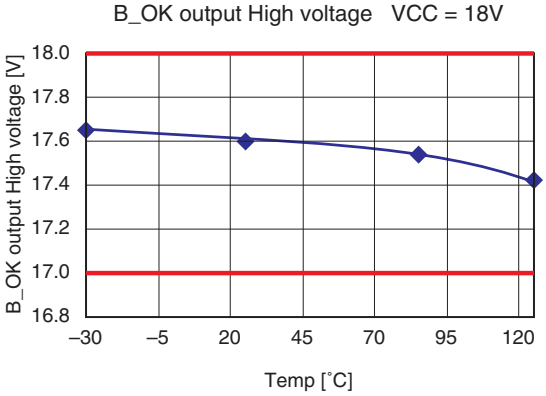
AC_DETOUT output Low voltage VCC = 18V

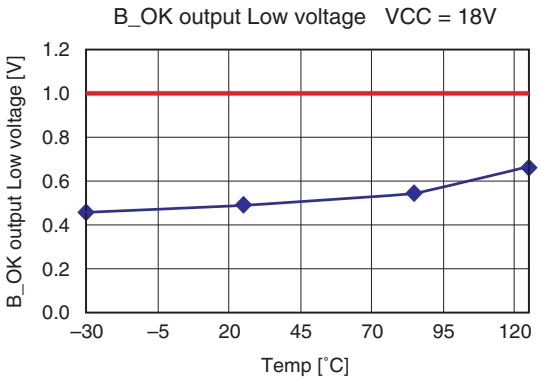


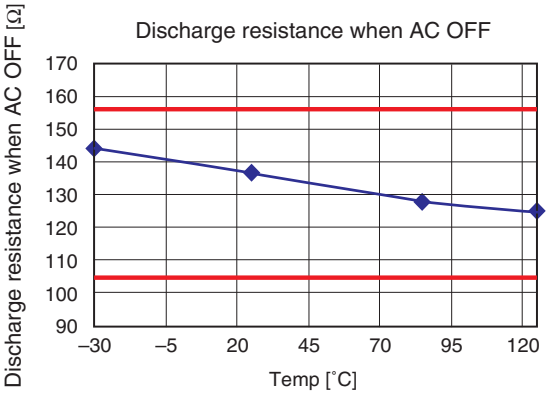
PFC operation hysteresis voltage

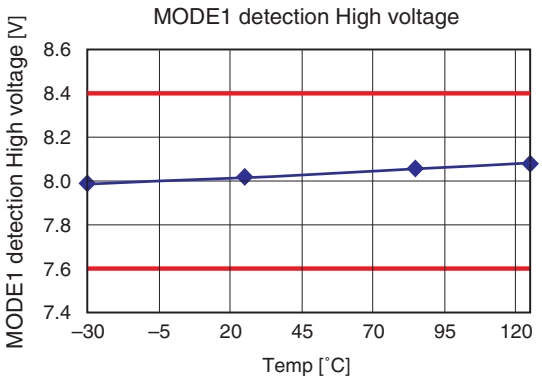


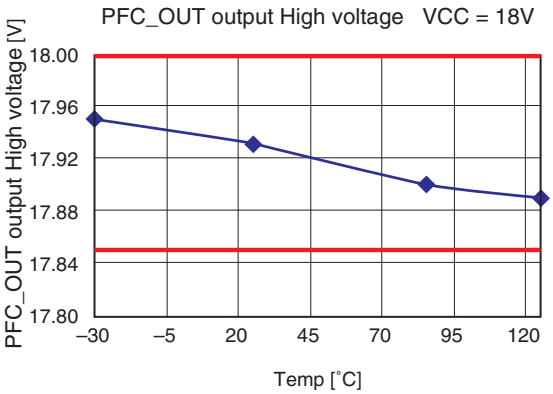
B_OK output High voltage VCC = 18V

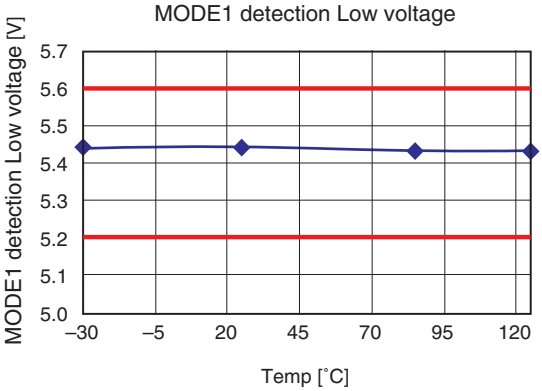


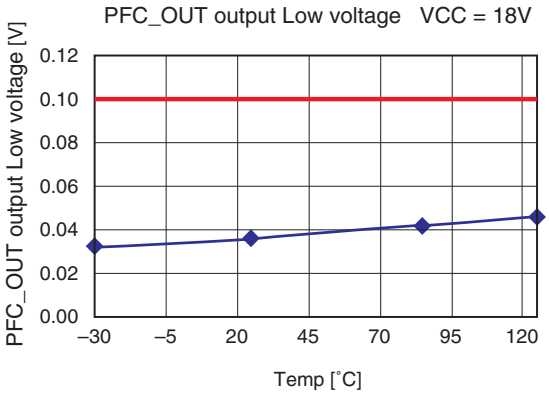

B_OK output Low voltage VCC = 18V
B_OK output Low voltage [V]
1.2
1.0
0.8
0.6
0.4
0.2
0.0
–30
–5
20
45
70
95
120
Temp [˚C]

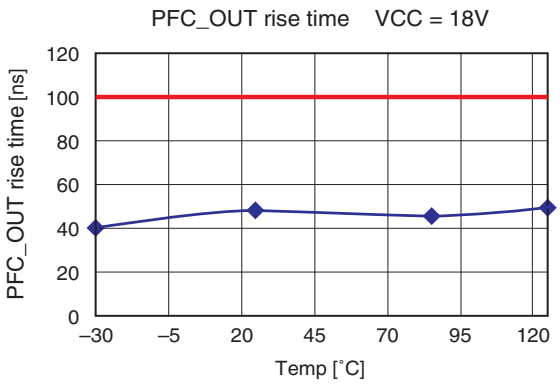

Discharge resistance when AC OFF
Discharge resistance when AC OFF [Ω]
170
160
150
140
130
120
110
100
90
–30
–5
20
45
70
95
120
Temp [˚C]

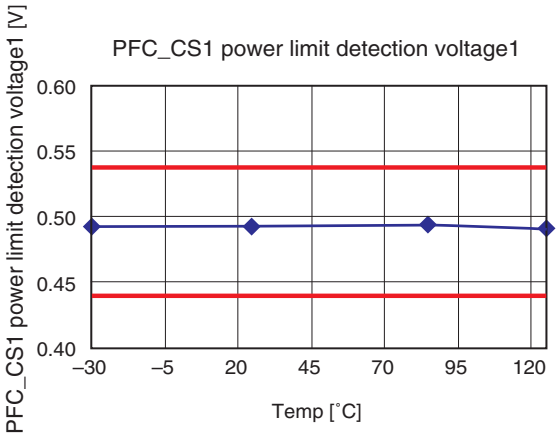

MODE1 detection High voltage
MODE1 detection High voltage [V]
8.6
8.4
8.2
8.0
7.8
7.6
7.4
–30
–5
20
45
70
95
120
Temp [˚C]

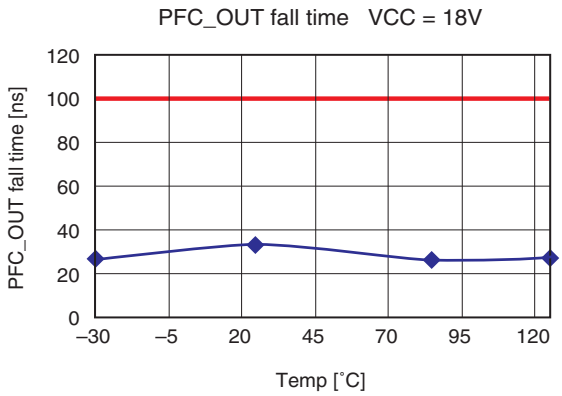

PFC_OUT output High voltage VCC = 18V
PFC_OUT output High voltage [V]
18.00
17.96
17.92
17.88
17.84
17.80
–30
–5
20
45
70
95
120
Temp [˚C]

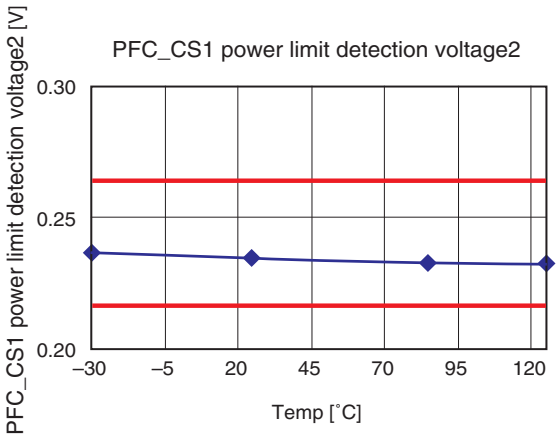

MODE1 detection Low voltage
MODE1 detection Low voltage [V]
5.7
5.6
5.5
5.4
5.3
5.2
5.1
5.0
–30
–5
20
45
70
95
120
Temp [˚C]

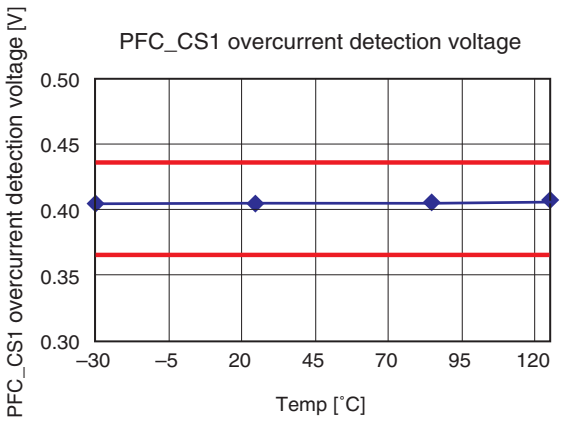

PFC_OUT output Low voltage VCC = 18V
PFC_OUT output Low voltage [V]
0.12
0.10
0.08
0.06
0.04
0.02
0.00
–30
–5
20
45
70
95
120
Temp [˚C]

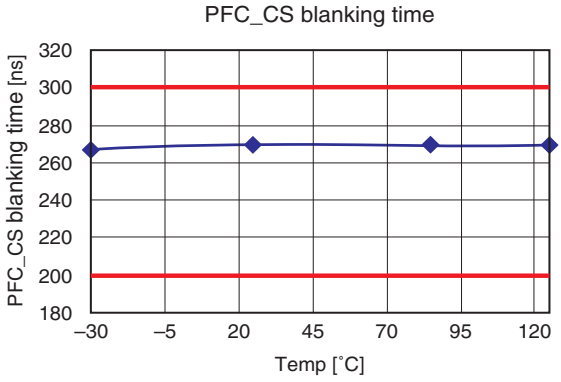

PFC_OUT rise time VCC = 18V
PFC_OUT rise time [ns]
120
100
80
60
40
20
0
–30
–5
20
45
70
95
120
Temp [˚C]

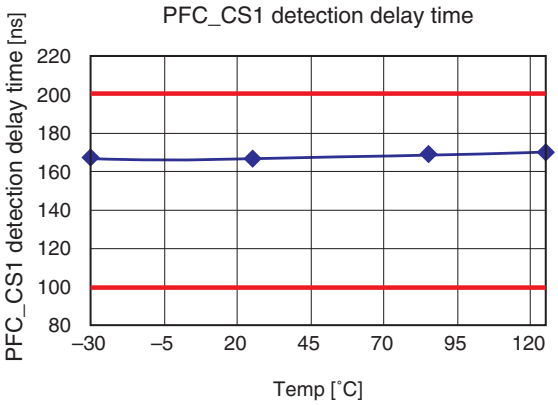

PFC_CS1 power limit detection voltage1
PFC_CS1 power limit detection voltage1 [V]
0.60
0.55
0.50
0.45
0.40
–30
–5
20
45
70
95
120
Temp [˚C]

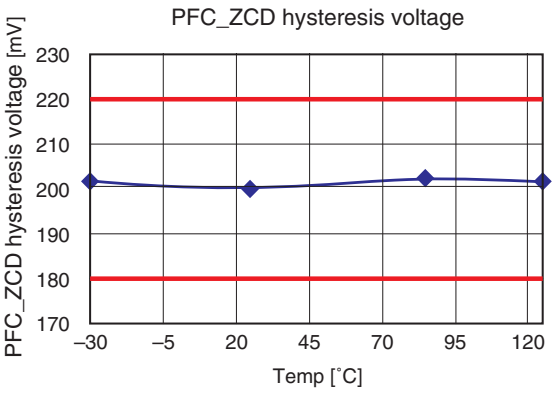

PFC_OUT fall time VCC = 18V
PFC_OUT fall time [ns]
120
100
80
60
40
20
0
–30
–5
20
45
70
95
120
Temp [˚C]

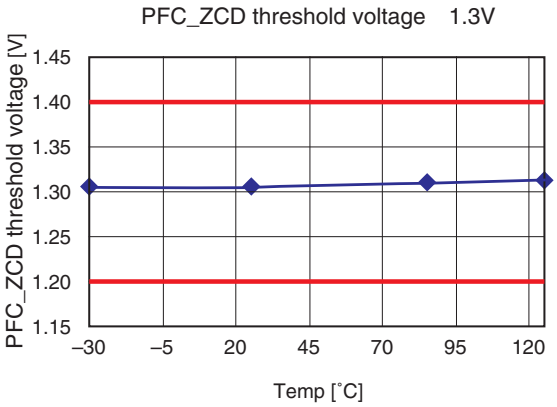

PFC_CS1 power limit detection voltage2
PFC_CS1 power limit detection voltage2 [V]
0.30
0.25
0.20
–30
–5
20
45
70
95
120
Temp [˚C]

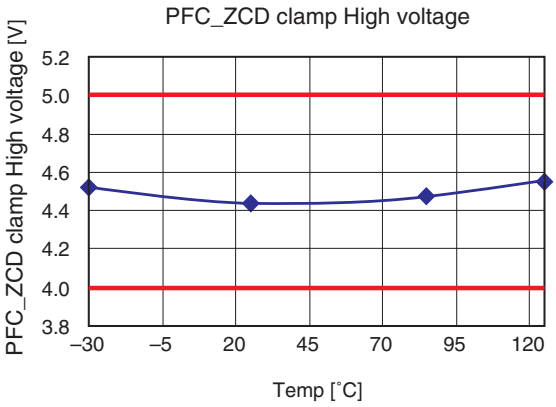

PFC_CS1 overcurrent detection voltage
PFC_CS1 overcurrent detection voltage [V]
0.50
0.45
0.40
0.35
0.30
–30
–5
20
45
70
95
120
Temp [˚C]

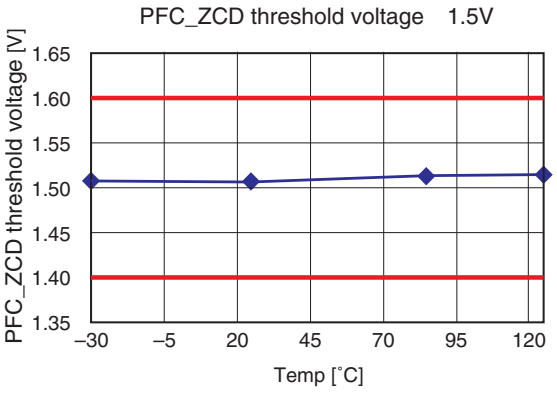

PFC_CS blanking time
PFC_CS blanking time [ns]
320
300
280
260
240
220
200
180
–30
–5
20
45
70
95
120
Temp [˚C]

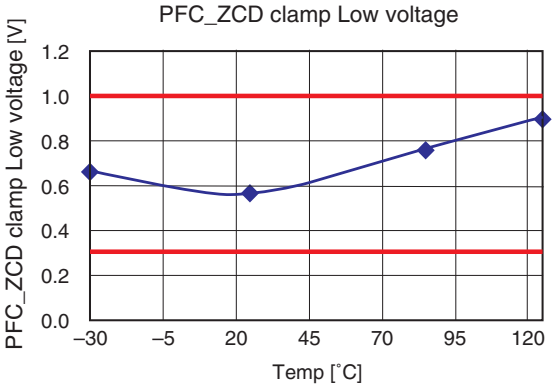

PFC_CS1 detection delay time
PFC_CS1 detection delay time [ns]
220
200
180
160
140
120
100
80
–30
–5
20
45
70
95
120
Temp [˚C]


PFC_ZCD hysteresis voltage
PFC_ZCD hysteresis voltage [mV]
230
220
210
200
190
180
170
–30
–5
20
45
70
95
120
Temp [˚C]

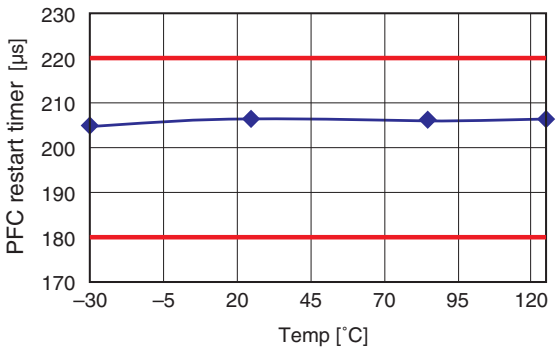

PFC_ZCD threshold voltage 1.3V
PFC_ZCD threshold voltage [V]
1.45
1.40
1.35
1.30
1.25
1.20
1.15
–30
–5
20
45
70
95
120
Temp [˚C]


PFC_ZCD clamp High voltage
PFC_ZCD clamp High voltage [V]
5.2
5.0
4.8
4.6
4.4
4.2
4.0
3.8
–30
–5
20
45
70
95
120
Temp [˚C]

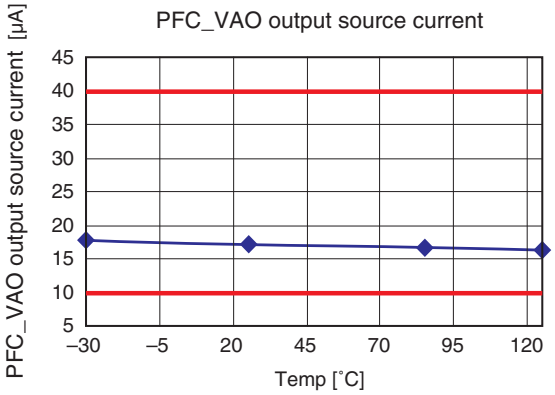

PFC_ZCD threshold voltage 1.5V
PFC_ZCD threshold voltage [V]
1.65
1.60
1.55
1.50
1.45
1.40
1.35
–30
–5
20
45
70
95
120
Temp [˚C]


PFC_ZCD clamp Low voltage
PFC_ZCD clamp Low voltage [V]
1.2
1.0
0.8
0.6
0.4
0.2
0.0
–30
–5
20
45
70
95
120
Temp [˚C]

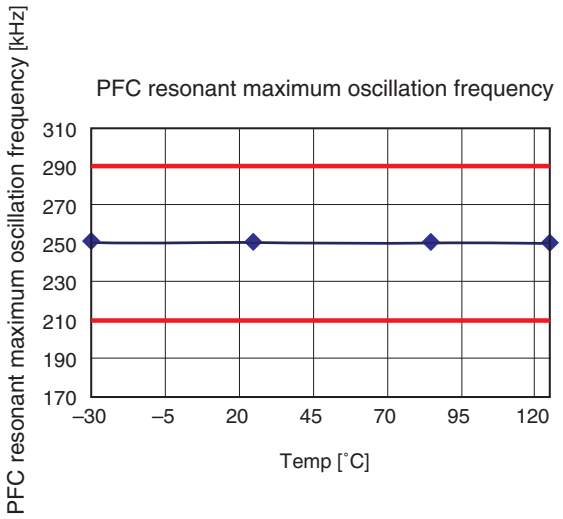
PFC restart timer



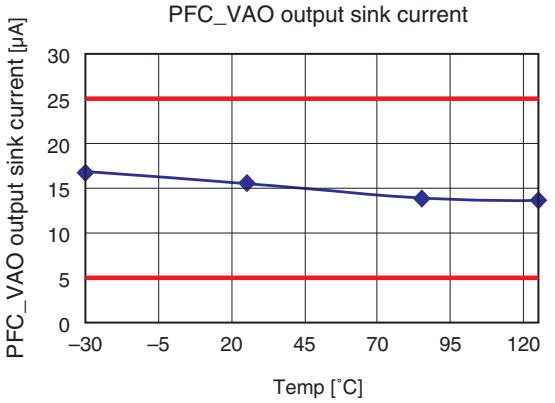
PFC_VAO output source current



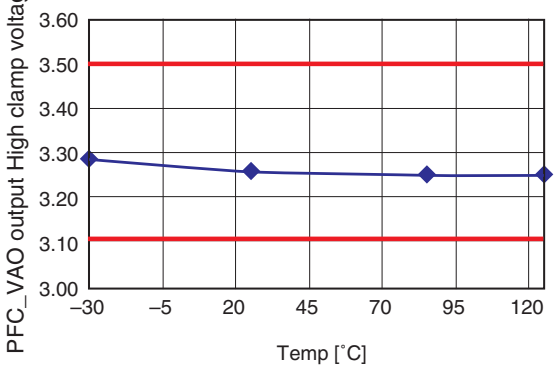
PFC resonant maximum oscillation frequency



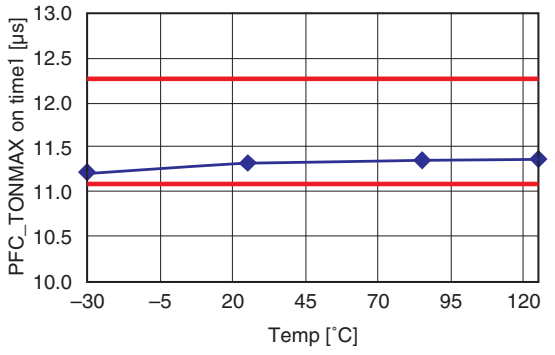
PFC_VAO output sink current

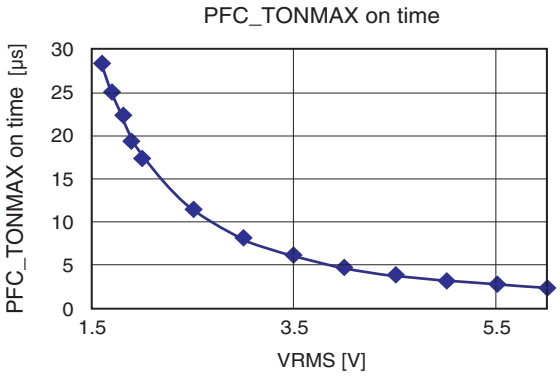


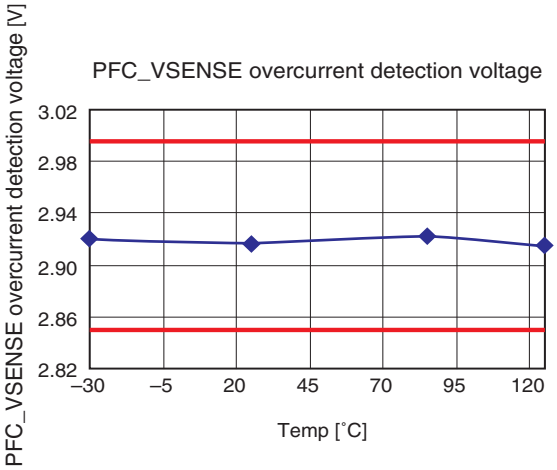
PFC_VAO output High clamp voltage

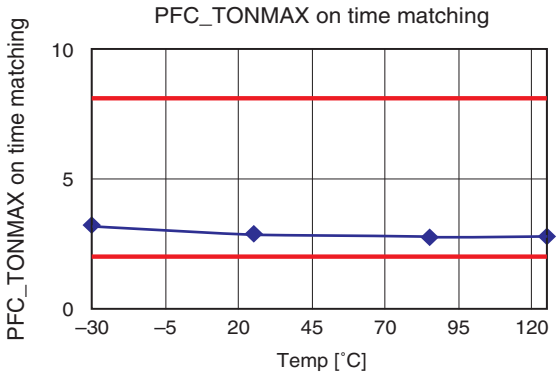


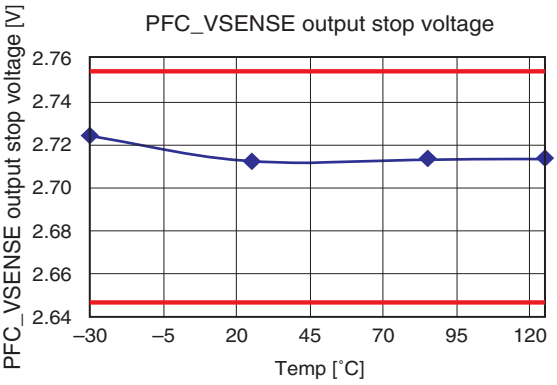
PFC_TONMAX on time1

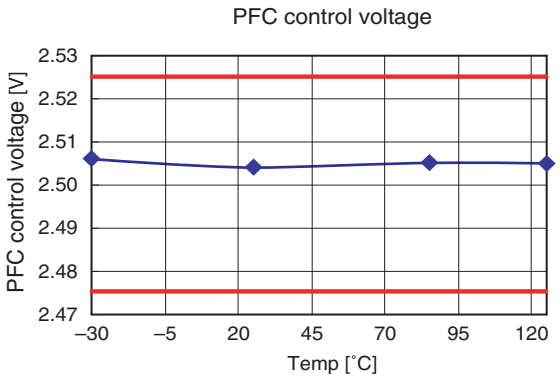


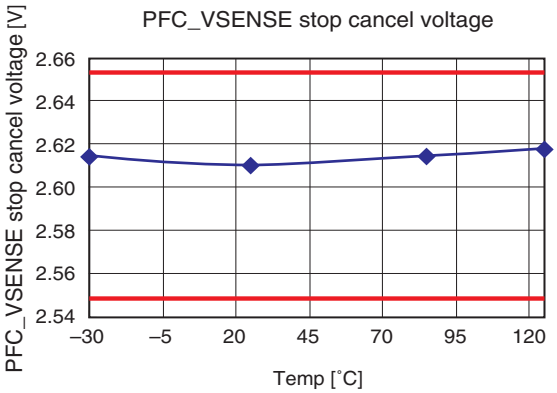

PFC_TONMAX on time
PFC_TONMAX on time [µs]
30
25
20
15
10
5
0
1.5
3.5
5.5
VRMS [V]

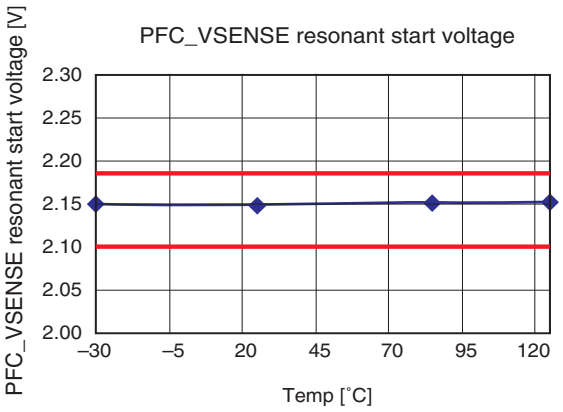

PFC_VSENSE overcurrent detection voltage
PFC_VSENSE overcurrent detection voltage [V]
3.02
2.98
2.94
2.90
2.86
2.82
–30
–5
20
45
70
95
120
Temp [˚C]

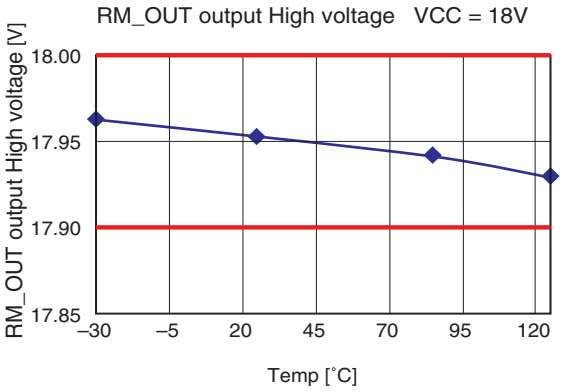

PFC_TONMAX on time matching
PFC_TONMAX on time matching
10
5
0
–30
–5
20
45
70
95
120
Temp [˚C]

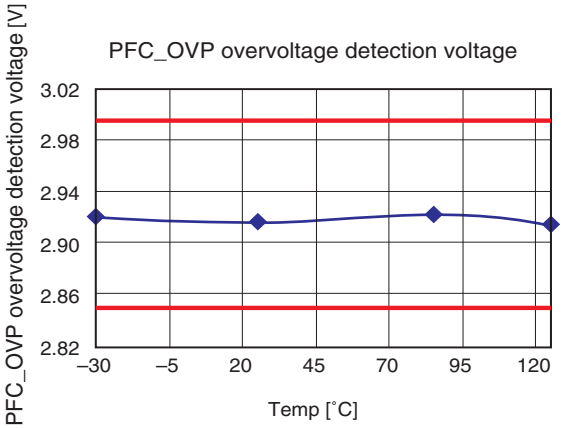

PFC_VSENSE output stop voltage
PFC_VSENSE output stop voltage [V]
2.76
2.74
2.72
2.70
2.68
2.66
2.64
–30
–5
20
45
70
95
120
Temp [˚C]

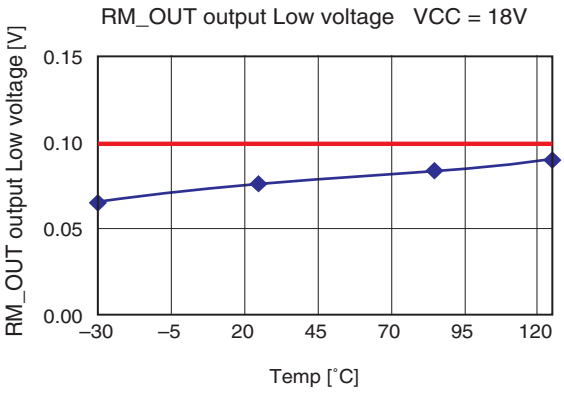

PFC control voltage
PFC control voltage [V]
2.53
2.52
2.51
2.50
2.49
2.48
2.47
–30
–5
20
45
70
95
120
Temp [˚C]

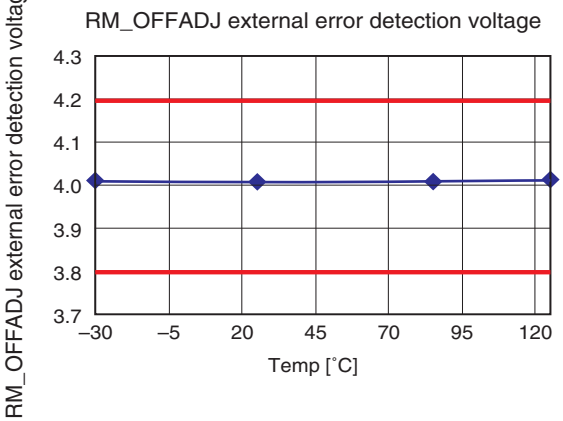

PFC_VSENSE stop cancel voltage
PFC_VSENSE stop cancel voltage [V]
2.66
2.64
2.62
2.60
2.58
2.56
2.54
–30
–5
20
45
70
95
120
Temp [˚C]

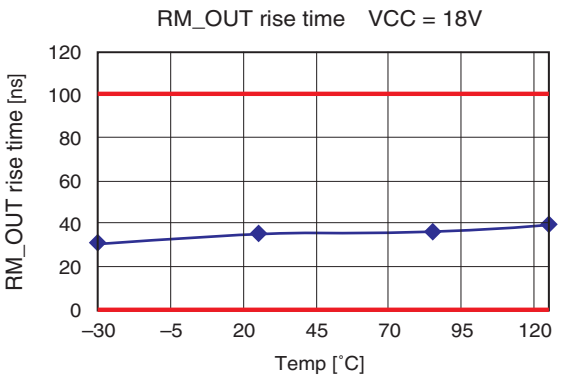

PFC_VSENSE resonant start voltage
PFC_VSENSE resonant start voltage [V]
2.30
2.25
2.20
2.15
2.10
2.05
2.00
–30
–5
20
45
70
95
120
Temp [˚C]


RM_OUT output High voltage VCC = 18V
RM_OUT output High voltage [V]
18.00
17.95
17.90
17.85
–30
–5
20
45
70
95
120
Temp [˚C]

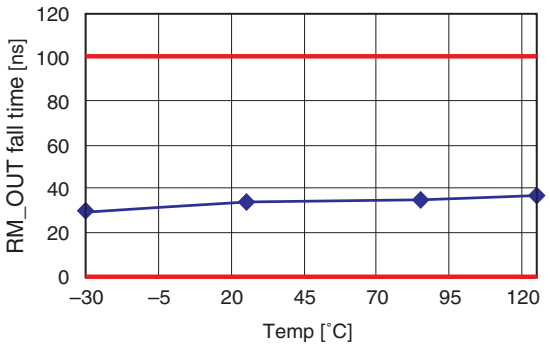

PFC_OVP overvoltage detection voltage
PFC_OVP overvoltage detection voltage [V]
3.02
2.98
2.94
2.90
2.86
2.82
–30
–5
20
45
70
95
120
Temp [˚C]


RM_OUT output Low voltage VCC = 18V
RM_OUT output Low voltage [V]
0.15
0.10
0.05
0.00
–30
–5
20
45
70
95
120
Temp [˚C]

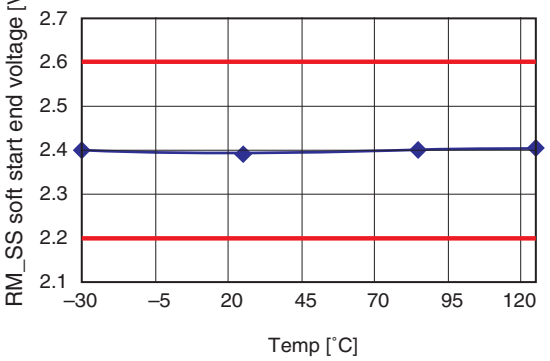

RM_OFFADJ external error detection voltage
RM_OFFADJ external error detection voltage [V]
4.3
4.2
4.1
4.0
3.9
3.8
3.7
–30
–5
20
45
70
95
120
Temp [˚C]


RM_OUT rise time VCC = 18V
RM_OUT rise time [ns]
120
100
80
60
40
20
0
–30
–5
20
45
70
95
120
Temp [˚C]

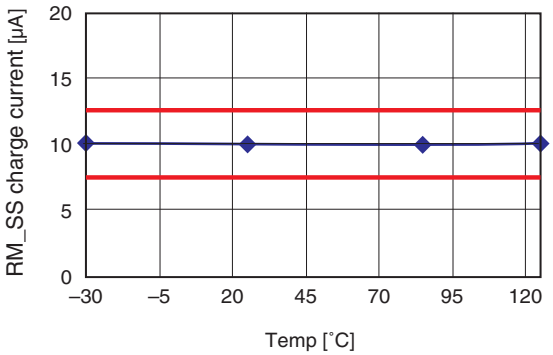
RM_OUT fall time VCC = 18V



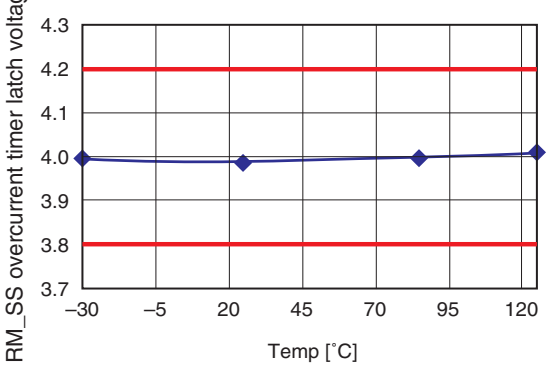
RM_SS soft start end voltage



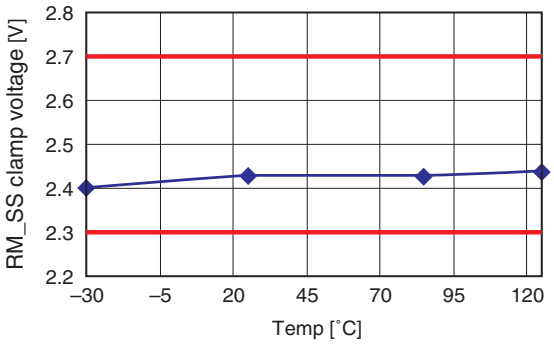
RM_SS charge current



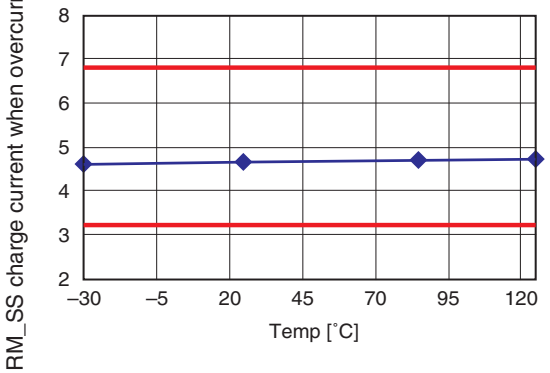
RM_SS overcurrent timer latch voltage



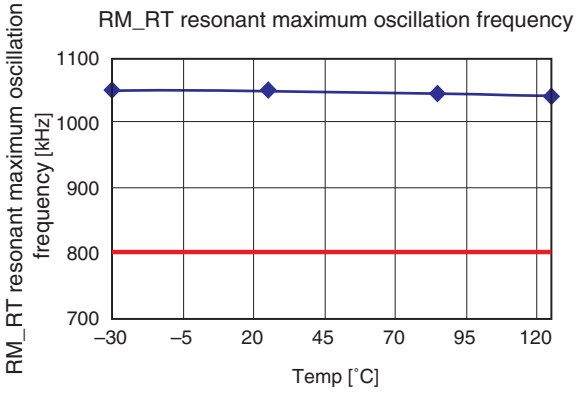
RM_SS clamp voltage



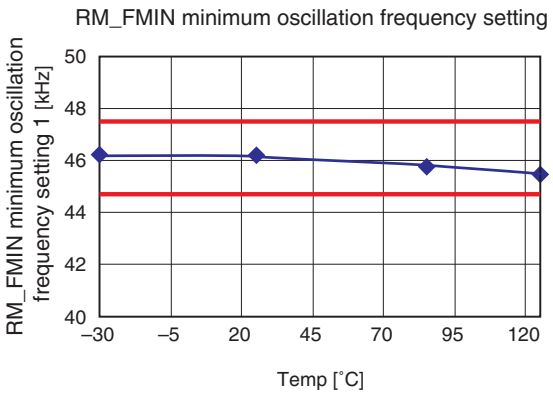
RM_SS charge current when overcurrent



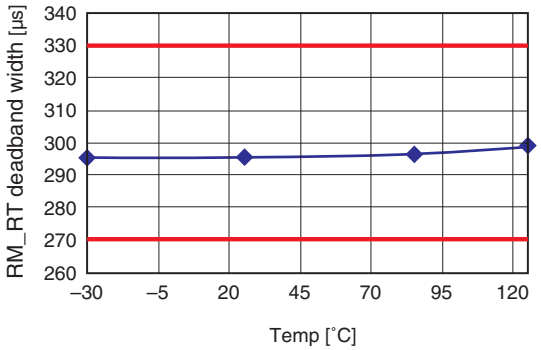
RM_RT resonant maximum oscillation frequency



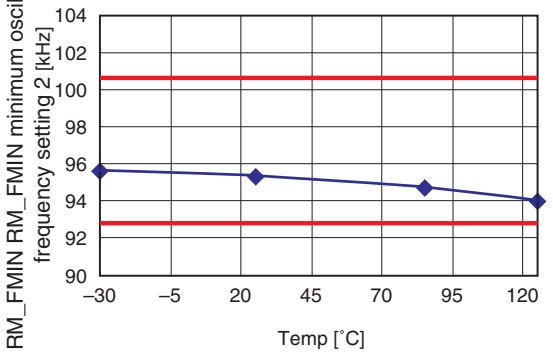
RM_FMIN minimum oscillation frequency setting 1



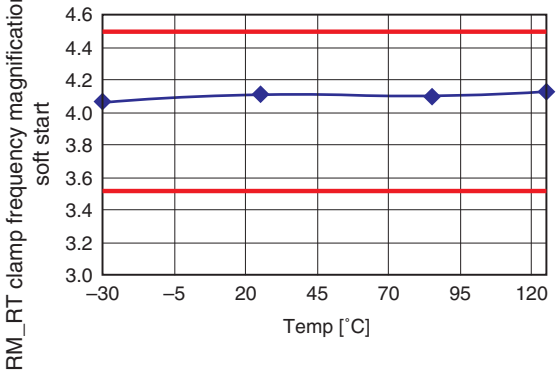
RM_RT deadband width



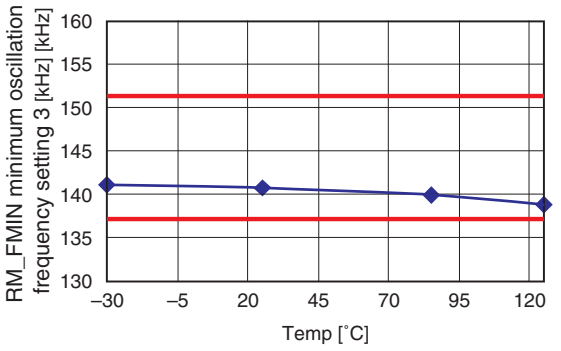
RM_FMIN minimum oscillation frequency setting 2



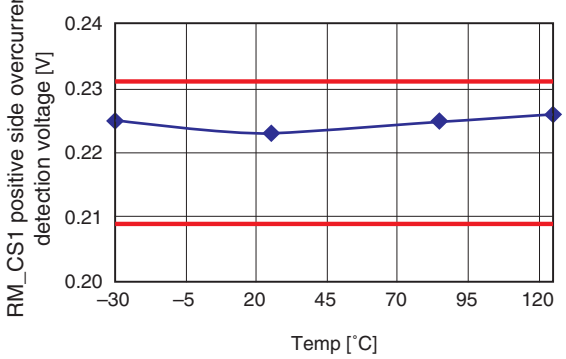
RM_RT clamp frequency magnification during soft start



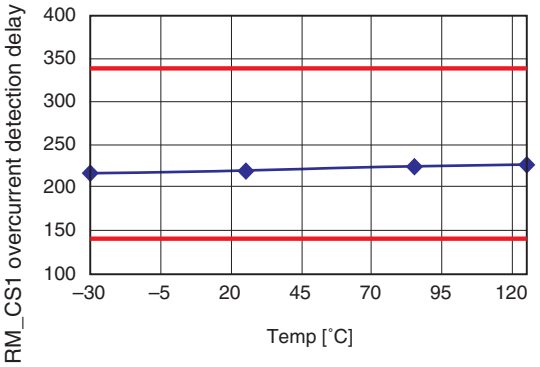
RM_FMIN minimum oscillation frequency setting 3



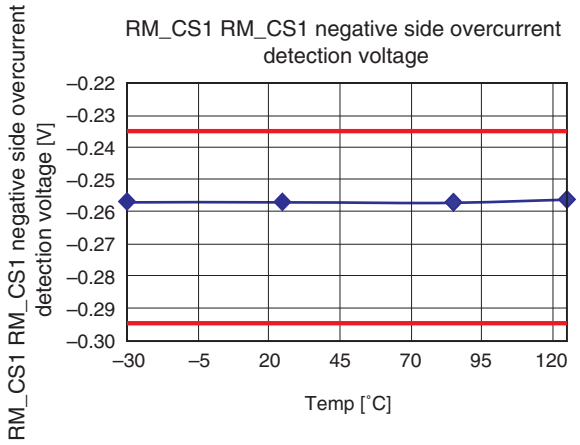
RM_CS1 positive side overcurrent detection voltage



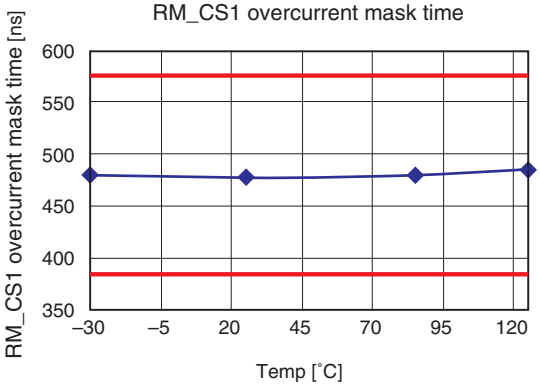
RM_CS1 overcurrent detection delay time
(sine wave input: 90kHz)
Reference data (Design assurance)



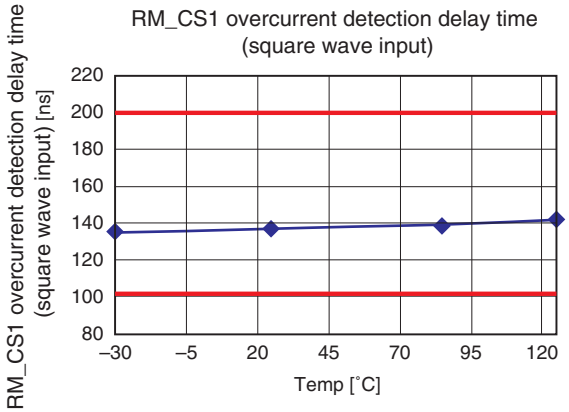
RM_CS1 RM_CS1 negative side overcurrent detection voltage



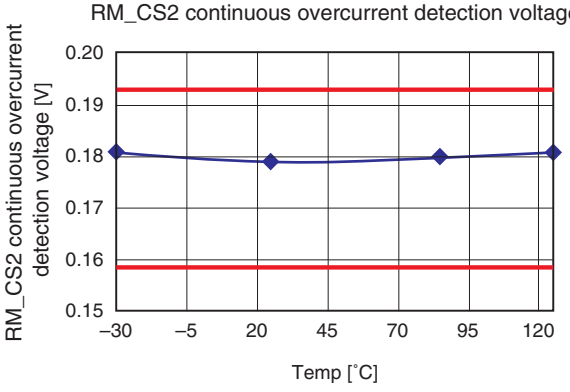
RM_CS1 overcurrent mask time

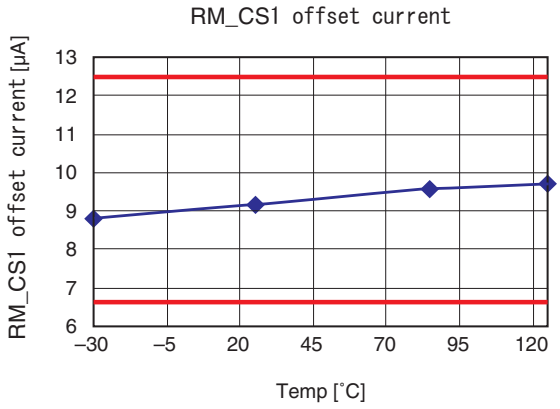


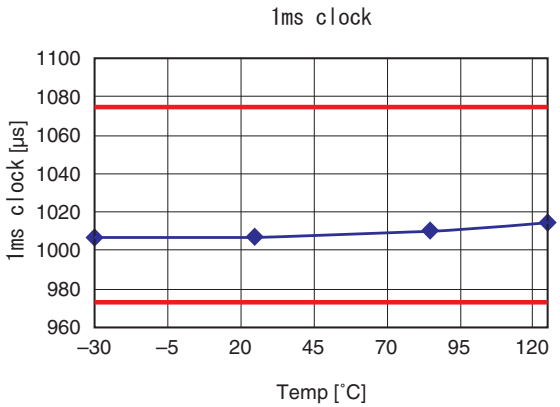
RM_CS1 overcurrent detection delay time
(square wave input)



RM_CS2 continuous overcurrent detection voltage




RM_CS1 offset current
RM_CS1 offset current [µA]
13
12
11
10
9
8
7
6
–30
–5
20
45
70
95
120
Temp [°C]

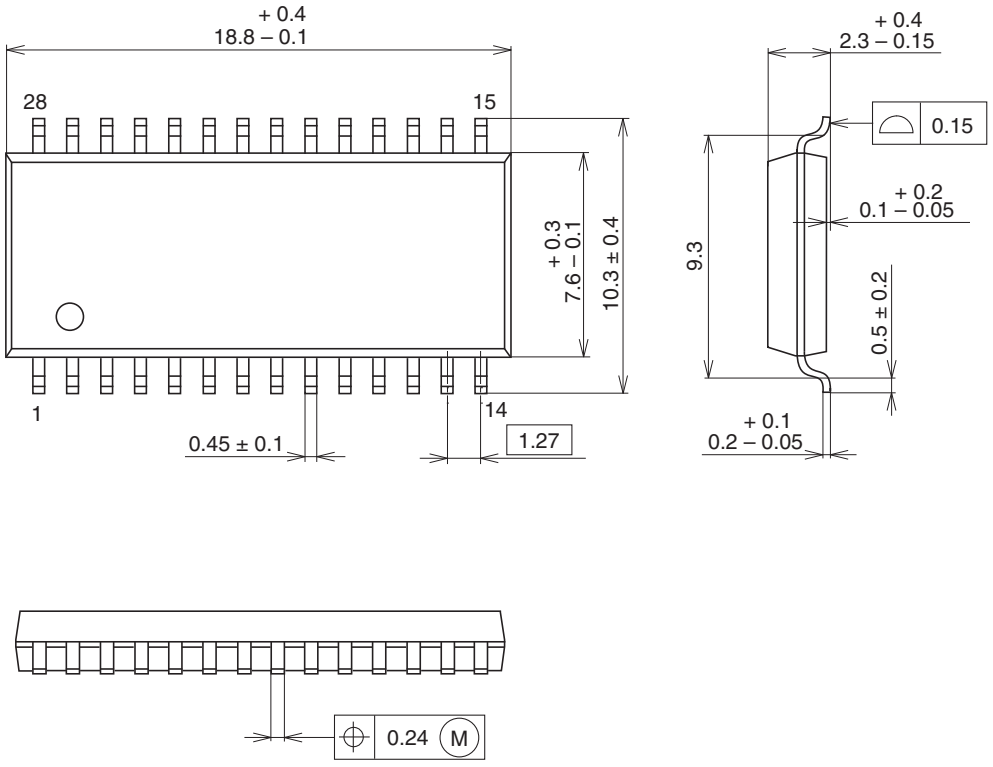

1ms clock
1ms clock [µs]
1100
1080
1060
1040
1020
1000
980
960
–30
–5
20
45
70
95
120
Temp [°C]

Package Outline

(Unit : mm)

SDT: 875336312

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L04
EIAJ CODE	SOP028-P-0375
JEDEC CODE	————

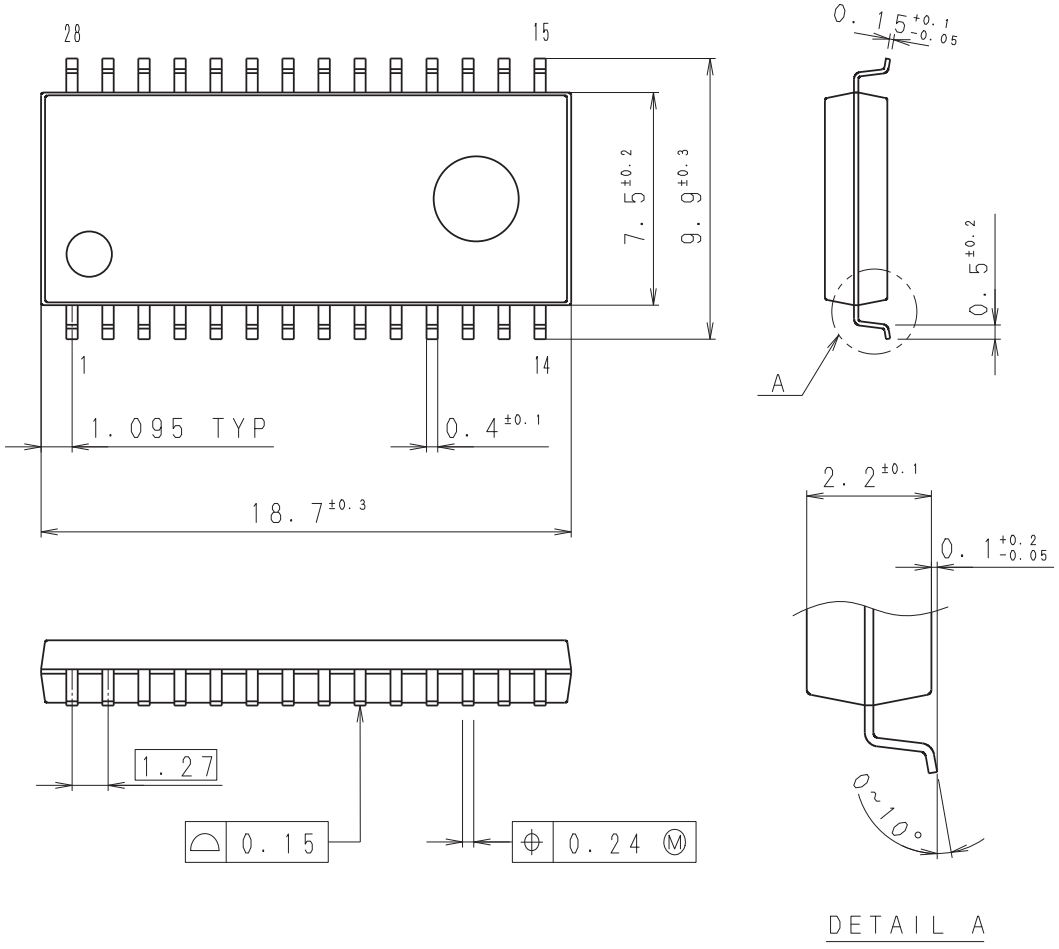
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

The height of mounted package

The maximum value of height of mounted package is 2.7 mm (2.3+0.4) in the Package Outline shown above. It has been confirmed that CPK is 3.5 or more and there is no problem even if the maximum value is changed to 2.4 mm (2.3+0.1).

AOI: 875337224

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L391
JEITA CODE	P-SOP28-18.7X7.5-1.27
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER
PACKAGE MASS	0.67g

AP-2000-28MAN1 Rev. 0