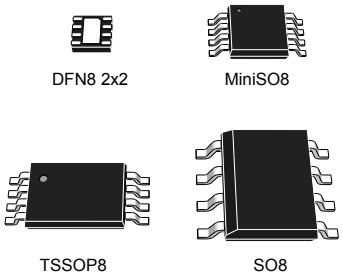
LM2904, LM2904A
LM2904W, LM2904AW

Datasheet

Low-power dual operational amplifier



Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current/amplifier, essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to [(V_{CC} $^{+}$) -1.5 V]

Description

This circuit consists of two independent, high gain operational amplifiers (op amps) that have frequency compensation implemented internally. They are designed specifically for automotive and industrial control systems. The circuit operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied from the standard 5 V which is used in logic systems and easily provides the required electronic interfaces without requiring any additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from a single power supply.

Maturity status link		
	Enhanced V_{IO}	Enhanced ESD
LM2904		
LM2904A	✓	
LM2904W		✓
LM2904AW	✓	✓

Related products	
TSB572	Dual op-amps for low-power consumption (380 µA with 2.5 MHz GBP)
LM2902 LM2902W	Quad op-amps version
LM2904WH LM2904AH	High temperature version (150 °C)

1 Schematic diagram

Figure 1. **Schematic diagram (LM2904, LM2904A)**

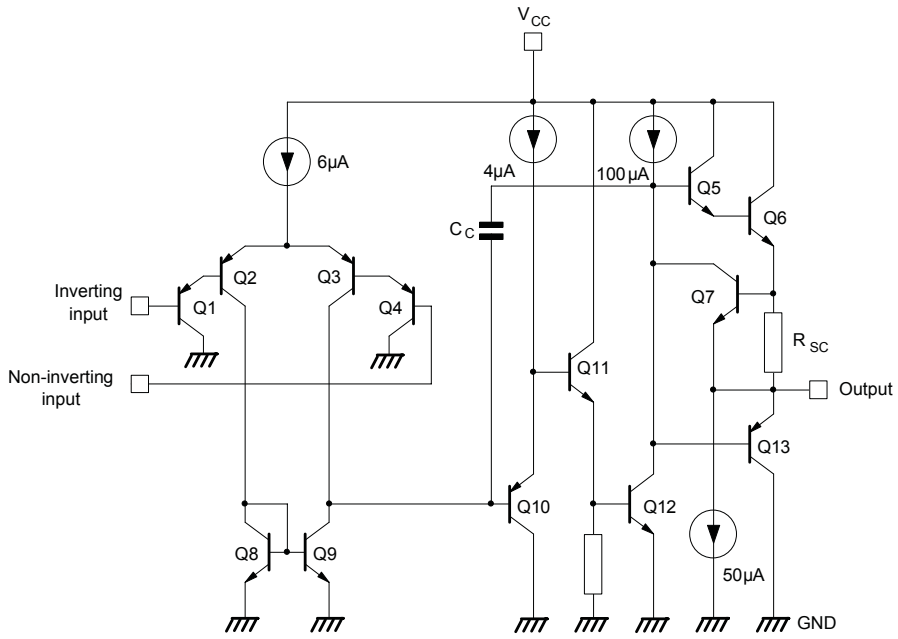
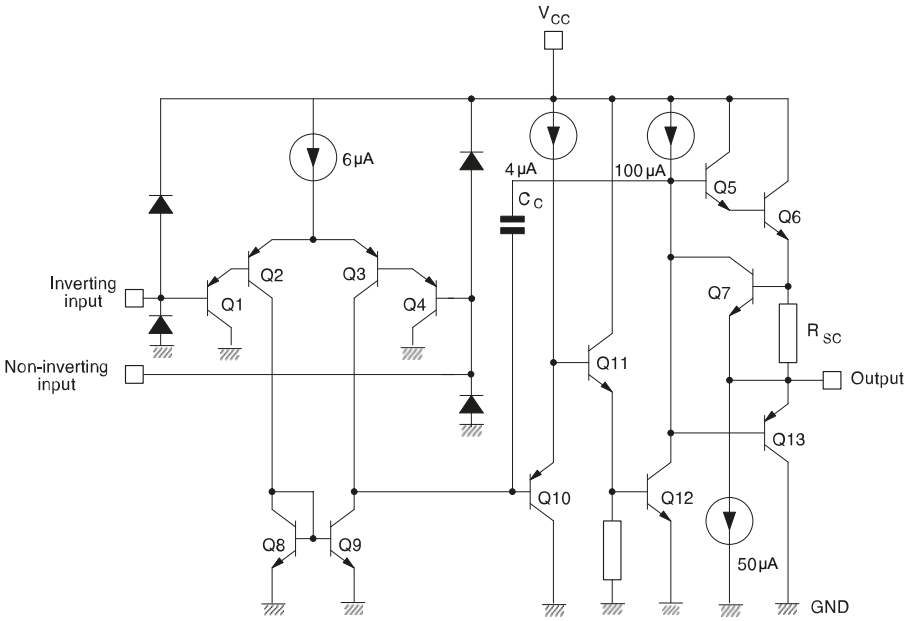
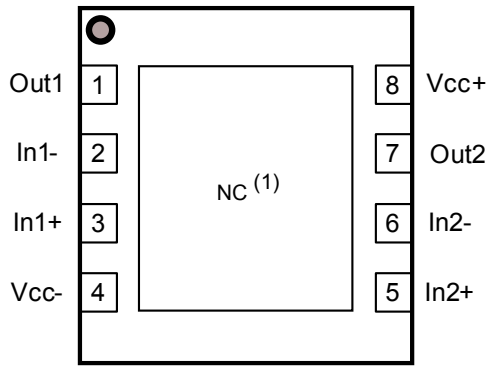


Figure 2. **Schematic diagram (LM2904W, LM2904AW)**



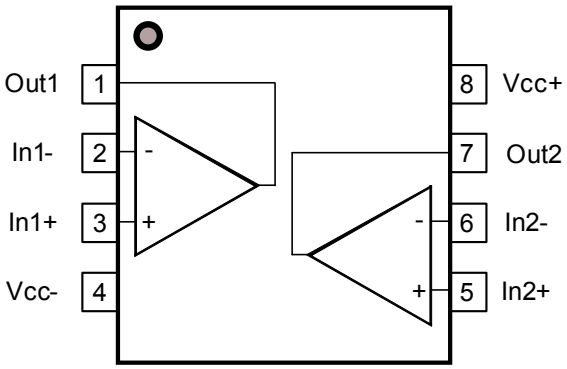
2 Package pin connections

Figure 3. DFN8 2x2 package pin connections (top view)



1. The exposed pad of the DFN8 2x2 can be connected to (VCC-) or left floating.

Figure 4. MiniSO8, TSSOP8, and SO8 package pin connections (top view)



3 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		±16 or 32	V
V_{id}	Differential input voltage (LM2904, LM2904A) (2)		±32	
	Differential input voltage (LM2904W, LM2904AW) (2)		-0.3 to V_{CC} +0.3	
V_{in}	Input voltage (LM2904, LM2904A)		-0.3 to 32	
	Input voltage (LM2904W, LM2904AW)		-0.3 to V_{CC} +0.3	
	Output short-circuit duration (3)		Infinite	s
I_{in}	Input current : V_{in} driven negative		5 mA in DC or 50 mA in AC, (duty cycle = 10 %, T = 1 s)	mA
	Input current : V_{in} driven positive above V_{CC} + 0.3 V (LM2904W, LM2904AW)		5 mA in DC or 50 mA in AC, (duty cycle = 10 %, T = 1 s)	
	Input current : V_{in} driven positive above 32 V (5)		0.4	
T_{oper}	Operating free-air temperature range		-40 to 125	°C
T_{stg}	Storage temperature range		-65 to 150	
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction to ambient (6)	DFN8 2x2	57	°C/W
		MiniSO8	190	
		TSSOP8	120	
		SO8	125	
R_{thjc}	Thermal resistance junction to case (6)	MiniSO8	39	
		TSSOP8	37	
		SO8	40	
ESD	HBM: human body model (LM2904, LM2904A) (7)		300	V
	HBM: human body model (LM2904W, LM2904AW) (7)		2000	
	MM: machine model (8)		200	
	CDM: charged device model (9)		1.5	kV

1. *All voltage values, except differential voltage are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.*
3. *Short-circuits from the output to V_{CC} can cause excessive heating if (V_{cc} $^+$) > 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.*
4. *This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as an input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.*
5. *The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max ($R = (V_{in} - 32\ V)/400\ \mu A$).*
6. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*

7. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*
8. *Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.*
9. *Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common mode input voltage range T_{amb} = 25 °C	V_{CC-} to V_{CC+} - 1.5	
	Common mode input voltage range $T_{min} \leq T_{amb} \leq T_{max}$	V_{CC-} to V_{CC+} - 2	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

4 Electrical characteristics

Table 3. V_{CC}^+ = 5 V, V_{CC-} = ground, V_O = 1.4 V, R_L connected to GND, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage, T_{amb} = 25 °C, LM2904, LM2904W (1)		2	7	mV
	Input offset voltage, T_{amb} = 25 °C, LM2904A, LM2904AW (1)		1	2	
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$, LM2904, LM2904W (1)			9	
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$, LM2904A, LM2904AW (1)			4	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		7	30	µV/°C
I_{io}	Input offset current, T_{amb} = 25 °C		2	30	nA
	Input offset current, $T_{min} \le T_{amb} \le T_{max}$			40	
$\Delta I_{io}/\Delta T$	Input offset current drift		10	300	pA/°C
I_{ib}	Input bias current, T_{amb} = 25 °C (2)		20	150	nA
	Input bias current, $T_{min} \le T_{amb} \le T_{max}$ (2)			200	
A_{vd}	Large signal voltage gain, V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, T_{amb} = 25 °C	50	100		V/mV
	Large signal voltage gain, V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, $T_{min} \le T_{amb} \le T_{max}$	25			
SVR	Supply voltage rejection ratio, V_{CC}^+ = 5 V to 30 V, V_{icm} = 0 V, T_{amb} = 25 °C	65	100		dB
	Supply voltage rejection ratio, V_{CC}^+ = 5 V to 30 V, V_{icm} = 0 V, $T_{min} \le T_{amb} \le T_{max}$	65			
I_{CC}	Supply current, all amp, no load, T_{amb} = 25 °C, V_{CC}^+ = 5 V		0.7	1.2	mA
	Supply current, all amp, no load, $T_{min} \le T_{amb} \le T_{max}$, V_{CC}^+ = 30 V			2	
CMR	Common-mode rejection ratio, V_{CC}^+ = 30 V, V_{icm} = 0 V to 28.5 V, T_{amb} = 25 °C	70	85		dB
	Common-mode rejection ratio, V_{CC}^+ = 30 V, V_{icm} = 0 V to 28 V, $T_{min} \le T_{amb} \le T_{max}$	60			
I_{source}	Output short-circuit current, V_{CC}^+ = 15 V, V_o = 2 V, V_{id} = 1 V	20	40	60	mA
I_{sink}	Output sink current, V_O = 2 V, V_{CC+} = 15 V	10	20		
	Output sink current, V_O = 0.2 V, V_{CC+} = 15 V	12	50		µA
V_{OH}	High-level output voltage (V_{CC}^+ = 30 V), T_{amb} = 25 °C, R_L = 2 kΩ	26			V
	High-level output voltage (V_{CC}^+ = 30 V), $T_{min} \le T_{amb} \le T_{max}$	26	27		
	High-level output voltage (V_{CC}^+ = 30 V), T_{amb} = 25 °C, R_L = 10 kΩ	27			
	High-level output voltage (V_{CC}^+ = 30 V), $T_{min} \le T_{amb} \le T_{max}$	27	28		
V_{OL}	Low-level output voltage (R_L = 10 kΩ), T_{amb} = 25 °C		5	20	mV
	Low-level output voltage (R_L = 10 kΩ), $T_{min} \le T_{amb} \le T_{max}$			20	

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR	Slew rate, V_{CC}^+ = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L =100 pF, unity gain, T_{amb} = 25 °C	0.3	0.6		V/µs
	Slew rate, V_{CC}^+ = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L =100 pF, unity gain, $T_{min} \le T_{amb} \le T_{max}$	0.2			
GBP	Gain bandwidth product, f = 100 kHz, V_{CC}^+ = 30 V, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF	0.7	1.1		MHz
THD	Total harmonic distortion, f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC}^+ = 30 V		0.02		%
e_n	Equivalent input noise voltage, f = 1 kHz, R_S = 100 Ω, V_{CC}^+ = 30 V		55		nV/√Hz
V_{O1}/V_{O2}	Channel separation, 1 kHz ≤ f ≤ 20 kHz (3)		120		dB

1. *V_O = 1.4 V, 5 V < V_{CC}^+ < 30 V, 0 V < V_{ic} < (V_{CC}^+) - 1.5 V*
2. *The direction of the input current is out of the IC. This current is essentially constant as long as the output is not saturated, so there is no change in the loading charge on the input lines.*
3. *Due to the proximity of external components, ensure that the stray capacitance does not cause coupling between these external parts. This can typically be detected at higher frequencies because this type of capacitance increases.*

5 Electrical characteristic curves

Figure 5. Open-loop frequency response

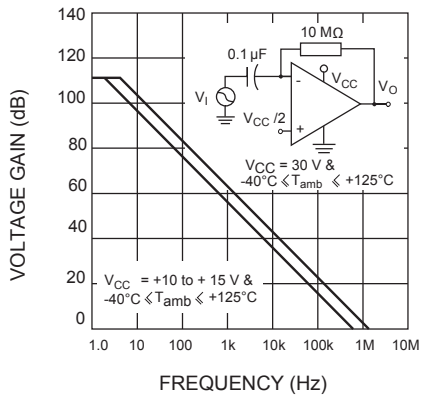


Figure 6. Large signal frequency response

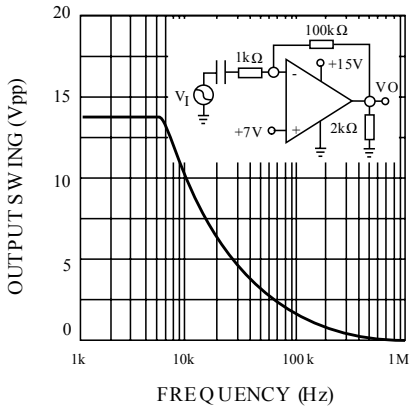


Figure 7. Voltage follower large signal response

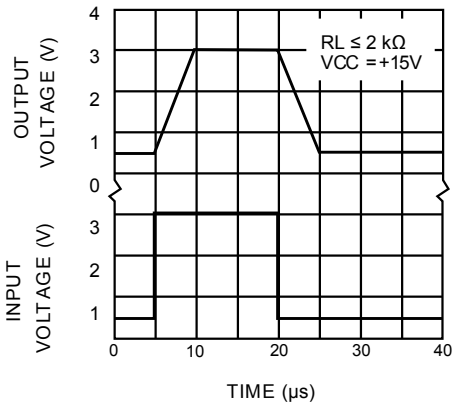


Figure 8. Current sinking output characteristics

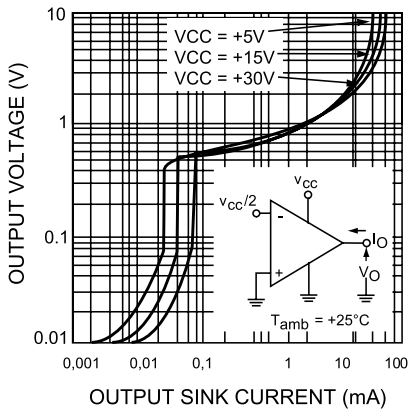


Figure 9. Voltage follower small signal response

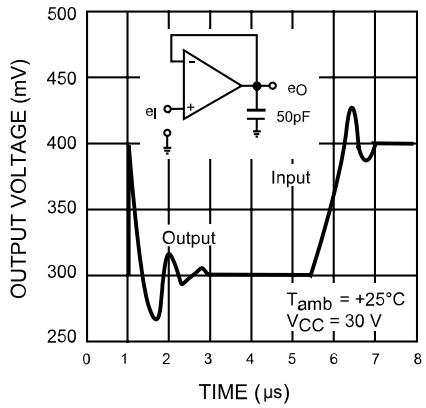


Figure 10. Current sourcing output characteristics

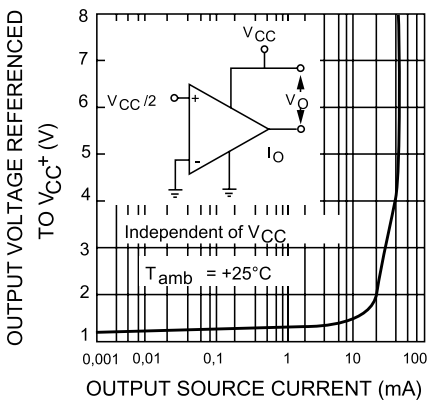


Figure 11. Input current vs. temperature

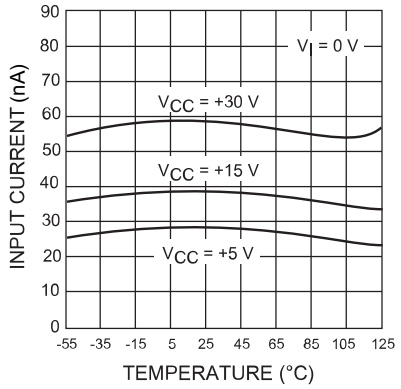


Figure 12. Current limiting

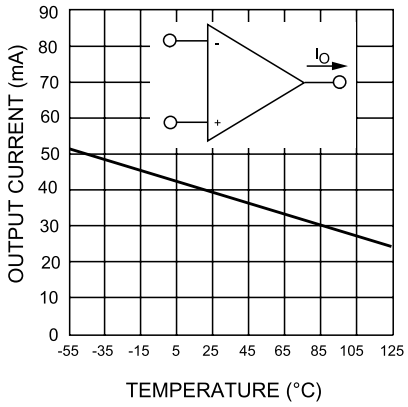


Figure 13. Input voltage range

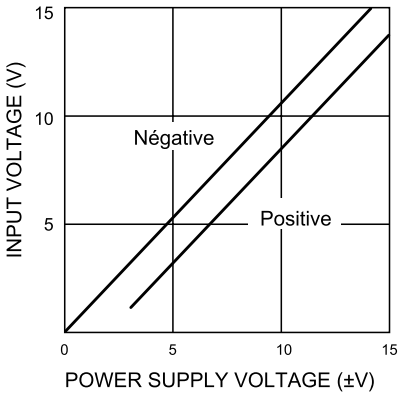


Figure 14. Supply current

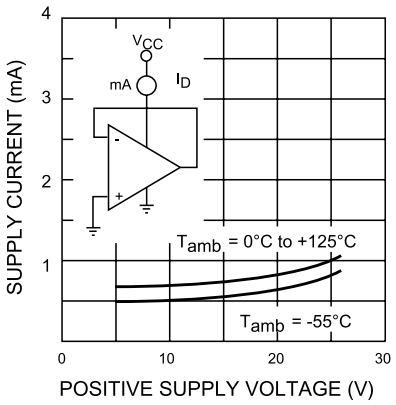


Figure 15. Voltage gain

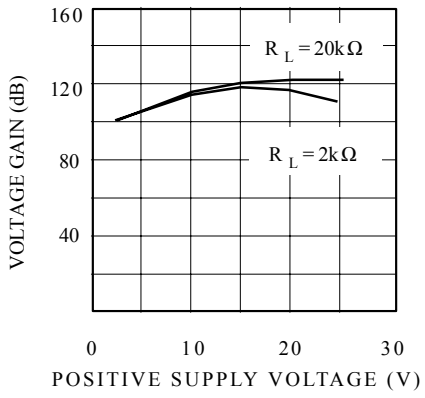


Figure 16. Input current vs. supply voltage

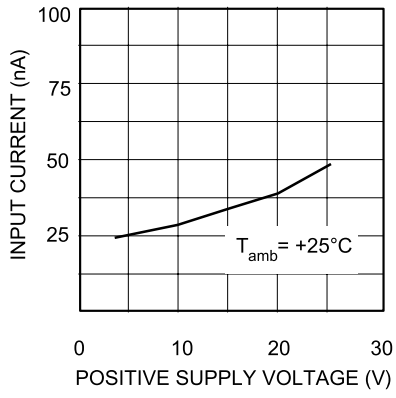


Figure 17. Gain bandwidth product

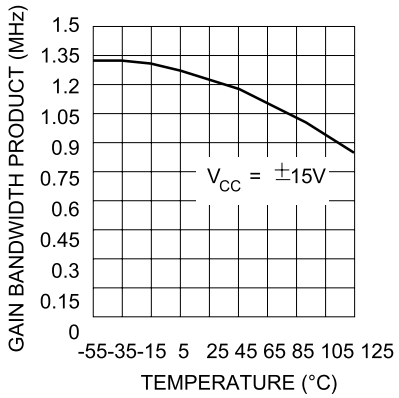


Figure 18. Power supply rejection ratio

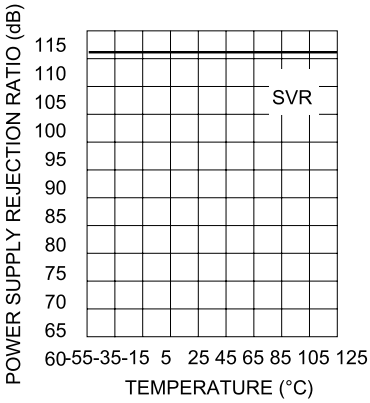


Figure 19. Common-mode rejection ratio

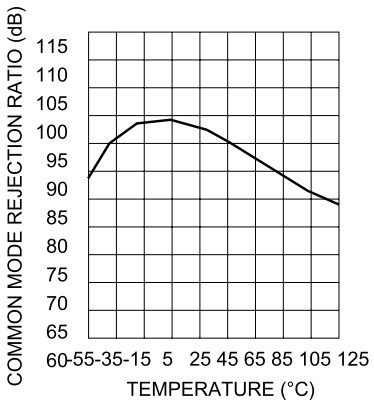
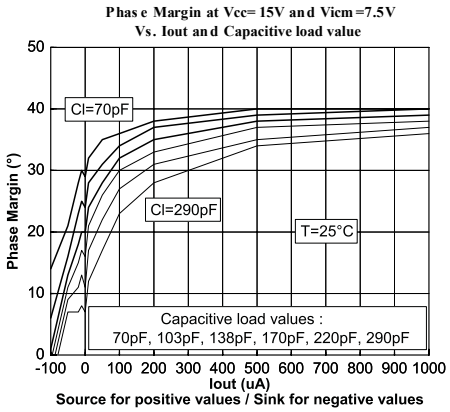


Figure 20. Phase margin vs. capacitive load



6 Typical single-supply applications

Figure 21. AC coupled inverting amplifier

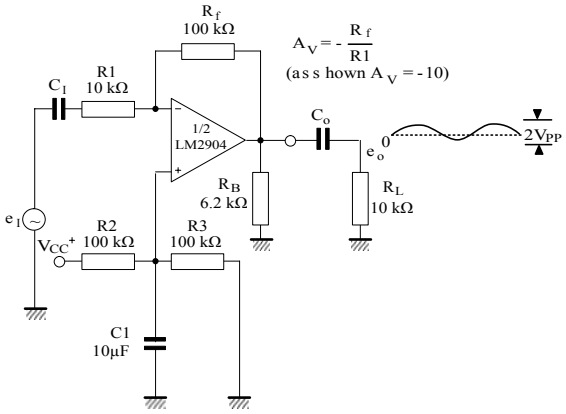


Figure 22. AC coupled non-inverting amplifier

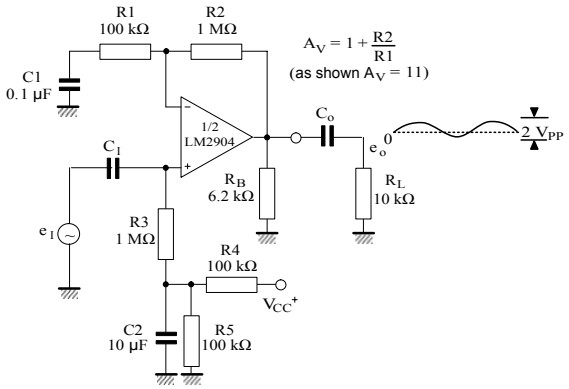


Figure 23. Non-inverting DC gain

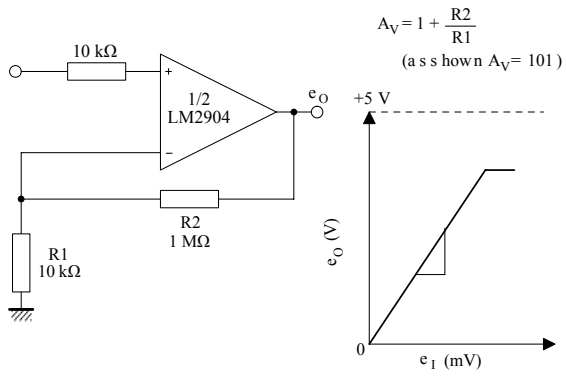


Figure 24. DC summing amplifier

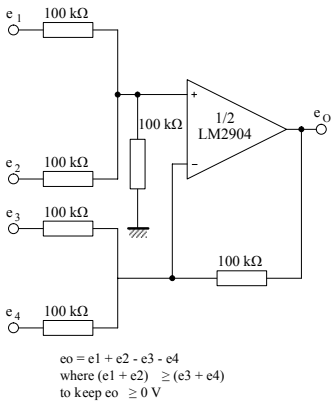
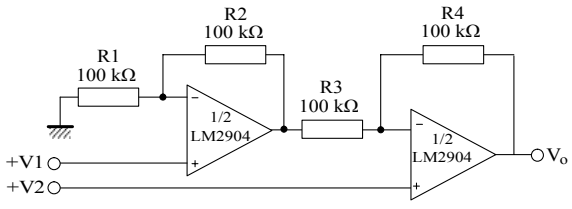


Figure 25. High input Z, DC differential amplifier



If R1 = R5 and R3 = R4 = R6 = R7

$eo = [1 + \frac{2R1}{R2}] (e2 - e1)$

As shown eo = 101 (e2 - e1)

Figure 26. Using symmetrical amplifiers to reduce input current

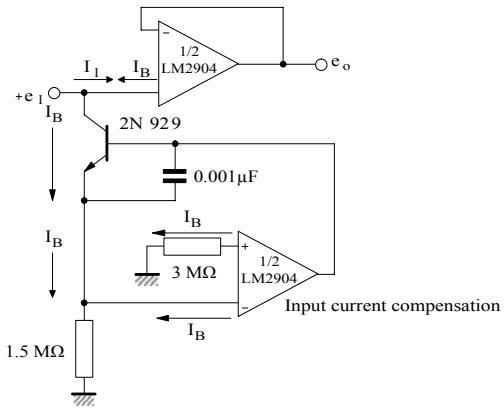


Figure 27. Low drift peak detector

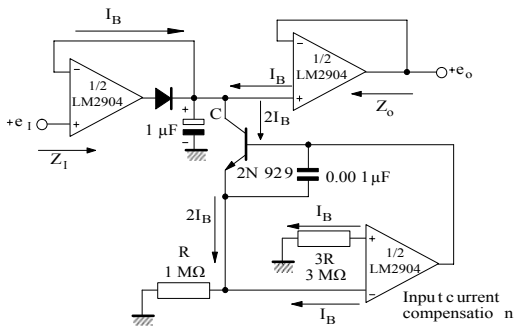
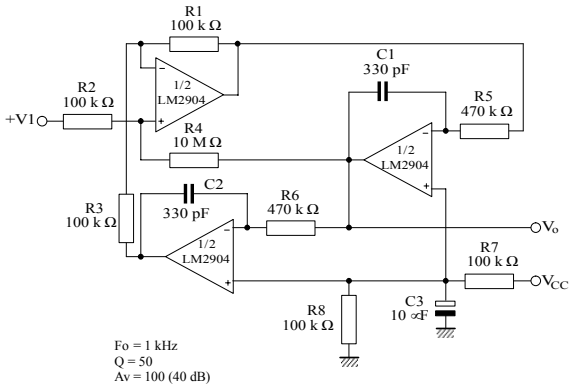


Figure 28. Active bandpass filter



7 Macromodel

An accurate macromodel of the LM2904, LM2904A is available on STMicroelectronics' web site at: ***www.st.com*** . This model is a trade-off between accuracy and complexity (that is, time simulation) of the LM2904, LM2904A operational amplifier. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN8 2 x 2 package information

Figure 29. **DFN8 2 x 2 package outline**

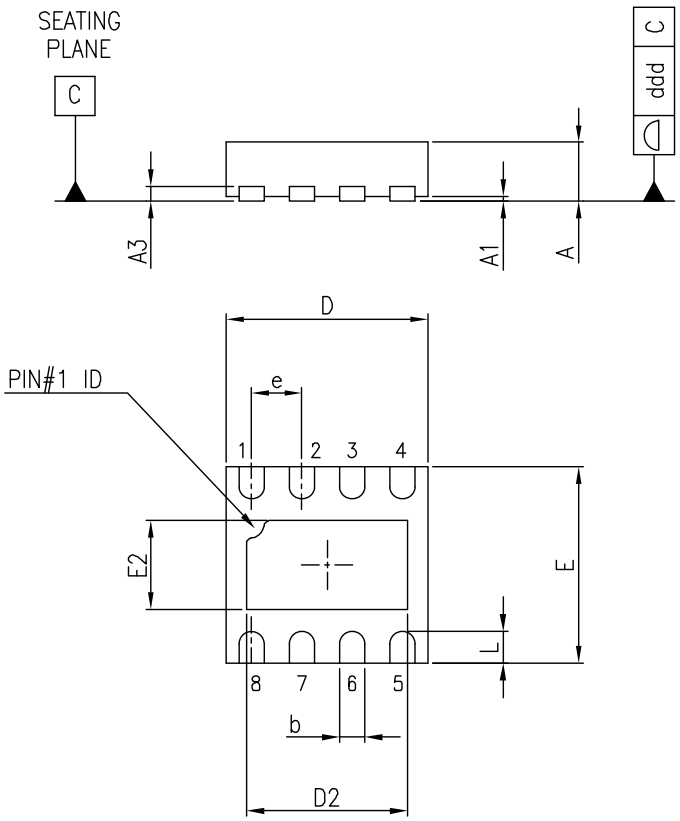
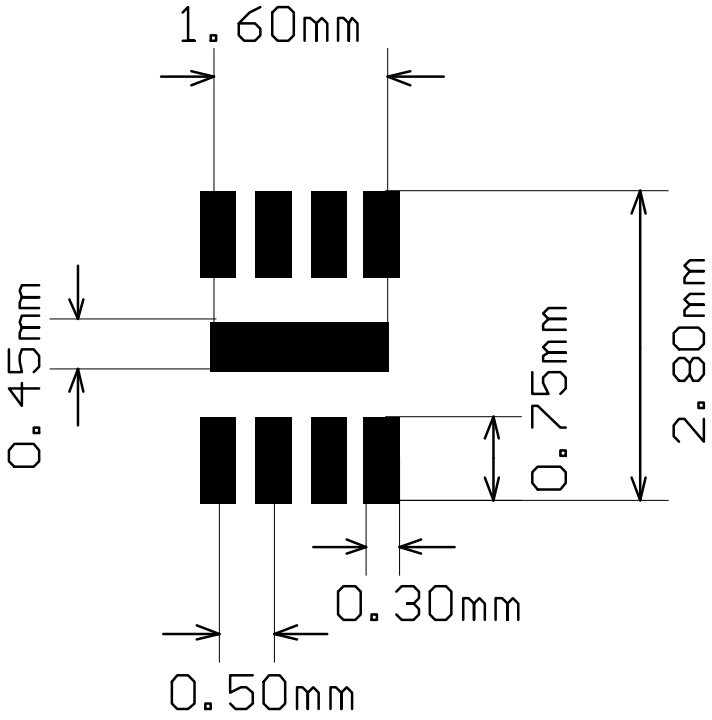


Table 4. **DFN8 2 x 2 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 30. **DFN8 2 x 2 recommended footprint**



8.2 MiniSO8 package information

Figure 31. **MiniSO8 package outline**

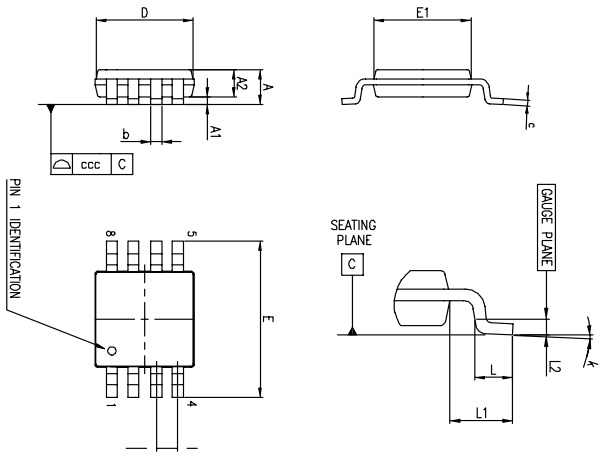


Table 5. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

8.3 TSSOP8 package information

Figure 32. **TSSOP8 package outline**

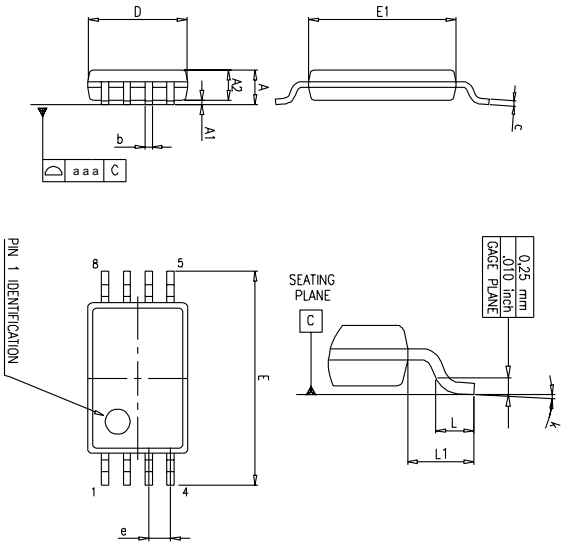


Table 6. **TSSOP8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

8.4 SO8 package information

Figure 33. **SO8 package outline**

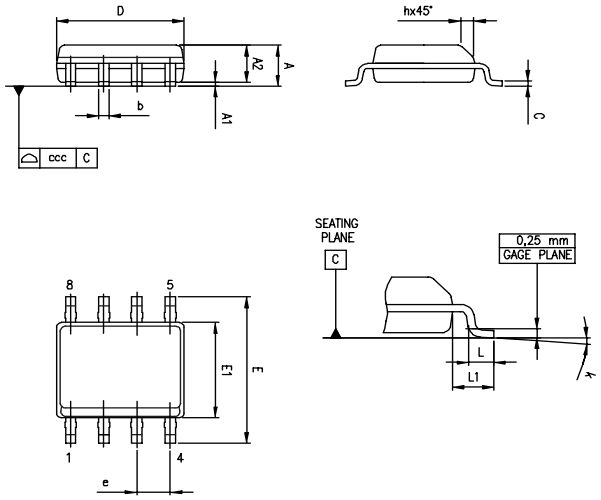


Table 7. **SO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

9 Ordering information

Table 8. Order codes

Order code	Temperature range	Package	Packing	Marking
LM2904D	-40 °C to 125 °C	SO8	Tube	2904
LM2904DT		SO8	Tape and reel	
LM2904PT		TSSOP8		
LM2904ST		MiniSO8		K403
LM2904Q2T		DFN8 2x2		K1Y
LM2904YDT (1)		SO8 (automotive grade level)		2904Y
LM2904AYDT(1)				2904AY
LM2904YPT(1)		TSSOP8 (automotive grade level)		2904Y
LM2904AYPT (1)				904AY
LM2904YST (1)		MiniSO8 (automotive grade level)		K409
LM2904WDT		SO8		2904W
LM2904WYDT (1)		SO8 (automotive grade level)		2904WY
LM2904WYPT (1)		TSSOP8 (automotive grade level)		K04WY
LM2904AWYPT (1)				K05WY

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Jan-2002	1	Initial release.
20-Jun-2005	2	PPAP references inserted in the datasheet, see Table 9 on page 21. ESD protection inserted in Table 1 on page 5.
10-Oct-2005	3	PPAP part numbers added in Table 9 on page 21.
12-Dec-2005	4	Pin connections identification added on cover page figure. Thermal resistance junction to case information added see Table 1 on page 5.
01-Feb-2006	5	Maximum junction temperature parameter added in Table 1 on page 5.
02-May-2006	6	Minimum slew rate parameter in temperature Table 3 on page 7.
13-Jul-2006	7	Modified ESD values and added explanation on V_{CC}, V_{id} in Table 1 on page 5. Added macromodel information.
28-Feb-2007	8	Modified ESD/HBM values in Table 1 on page 5. Updated MiniSO8 package information. Added note relative to automotive grade level part numbers in Table 9 on page 21.
18-Jun-2007	9	Power dissipation value corrected in Table 1: Absolute maximum ratings. Table 2: Operating conditions added. Equivalent input noise voltage parameter added in Table 3. Electrical characteristics curves updated. Figure 19: Phase margin vs capacitive load added. Section 6: Package information updated.
18-Dec-2007	10	Removed power dissipation parameter from Table 1: Absolute maximum ratings. Removed V_{opp} from electrical characteristics in Table 3. Corrected MiniSO8 package mechanical data in Section 6.4: MiniSO8 package information.
08-Apr-2008	11	Added table of contents. Corrected the scale of Figure 7 (mA not µA). Corrected SO8 package information.
02-Jun-2009	12	Added input current information in Table 1: Absolute maximum ratings. Added L1 parameters in Table 6: SO8 package mechanical data. Added new order codes, LM2904AYD/DT, LM2904AYPT and LM2904AYST in Table 9: Order codes.
13-Apr-2010	13	Added LM2904A on cover page. Corrected footnote (5) in Table 1: Absolute maximum ratings. Removed order code LM2904AYST from Table 9: Order codes.
24-Jan-2012	14	Removed macromodel from Chapter 5 (now available on www.st.com). Added DFN8 2 x 2 mm package information in Chapter 6 and related order codes in Chapter 7. Removed LM2904YD and LM2904AYD order codes from Table 9. Changed note for LM2904YST order code in Table 9.
24-Jan-2014	15	Updated: marking info for LM2904AYPT, package silhouette drawings in the cover page, $\Delta V_{io}/\Delta T$ and $\Delta I_{io}/\Delta T$ symbols in Table 3 on page 7 Added: ESD info in Features section and Section 2: Package pin connections Removed: LM2904N from Table 9: Order codes.
02-Oct-2015	16	Figure 1: Schematic diagram (1/2 LM2904, LM2904A): updated

Date	Revision	Changes
16-Feb-2016	17	Updated layout Removed “plastic micropackage” from SO8 and DFN8 2x2 package silhouettes; removed “thin shrink small outline package” from TSSOP8 package silhouette Table 3: unit of V_{OL} parameter changed from “V” to ‘mV” DFN8 2x2 package information: updated “L” TSSOP8 package information: “aaa” is a typ. value not a max value
15-Feb-2019	18	Added new part numbers LM2904W, LM2904AW, Figure 2. Schematic diagram (LM2904W, LM2904AW) and Table 2. Operating conditions. Updated: Table 1. Absolute maximum ratings, Section 4 Electrical characteristics and Section 9 Ordering information
26-Apr-2021	19	Added new I_{in} row parameter in Table 1. Absolute maximum ratings.

Contents

List of tables

List of figures