

HCD80R650E

800V N-Channel Super Junction MOSFET

Features

- ❑ Very Low FOM ($R_{DS(on)} \times Q_g$)
- ❑ Extremely low switching loss
- ❑ Excellent stability and uniformity
- ❑ 100% Avalanche Tested

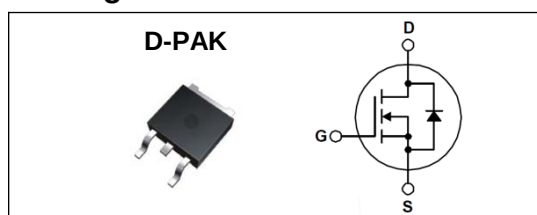
Application

- ❑ Switch Mode Power Supply (SMPS)
- ❑ Uninterruptible Power Supply (UPS)
- ❑ Power Factor Correction (PFC)
- ❑ Motor Control & LED Lighting Power
- ❑ DC-DC Converters

Key Parameters

Parameter	Value	Unit
$BV_{DSS} @ T_{J,max}$	850	V
I_D	8	A
$R_{DS(on), max}$	0.65	Ω
Q_g, Typ	12	nC

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	800	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	8	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	5	A
I_{DM}	Drain Current – Pulsed (Note 1)	24	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	240	mJ
dv/dt	MOSFET dv/dt ruggedness, $V_{DS}=0\dots 640\text{V}$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS}=0\dots 640\text{V}$, $I_{DS}\leq I_D$	15	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	83	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (minimum pad of 2 oz copper)	--	110	
$R_{\theta JA}$	Junction-to-Ambient (* 1 in ² pad of 2 oz copper)	--	50	

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.5	--	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 4\ \text{A}$	--	0.55	0.65	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	800	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	10	μA
		$V_{DS} = 800\ \text{V}, T_J = 150^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	750	--	pF
C_{oss}	Output Capacitance		--	38	--	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 400\ \text{V}, I_D = 8\ \text{A},$ $R_G = 25\ \Omega$	--	32	--	ns
t_r	Turn-On Rise Time		--	24	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	44	--	ns
t_f	Turn-Off Fall Time		--	20	--	ns
Q_g	Total Gate Charge	$V_{DS} = 640\ \text{V}, I_D = 8\ \text{A}$ $V_{GS} = 10\ \text{V}$	--	12	16	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	3.2	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I _S	Continuous Source-Drain Diode Forward Current		--	--	8	A
I _{SM}	Pulsed Source-Drain Diode Forward Current		--	--	24	
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 8 A, V _{GS} = 0 V	--	--	1.3	V
trr	Reverse Recovery Time	I _S = 4 A, V _R = 400 V di _F /dt = 100 A/μs	--	194	--	ns
Qrr	Reverse Recovery Charge		--	1.7	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=2.4\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Characteristics

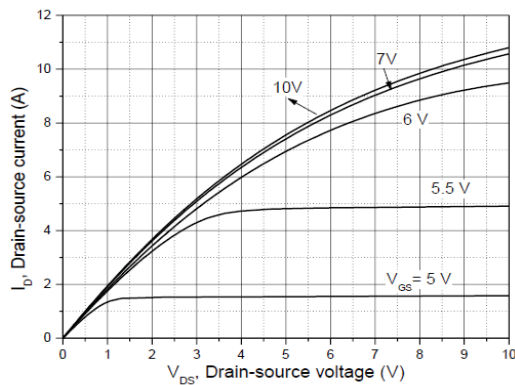


Figure 1. On Region Characteristics

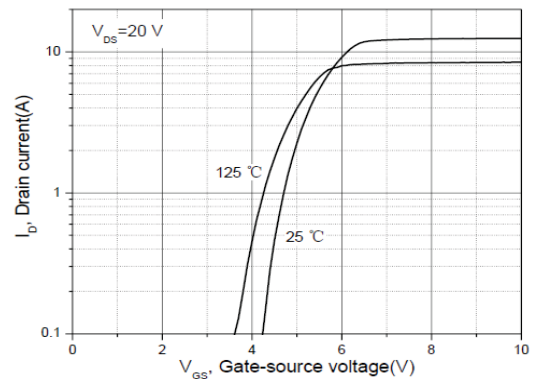


Figure 2. Transfer Characteristics

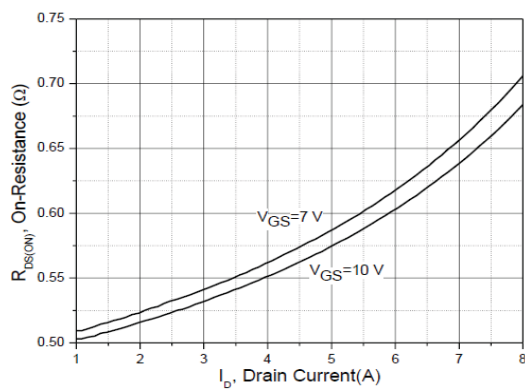


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

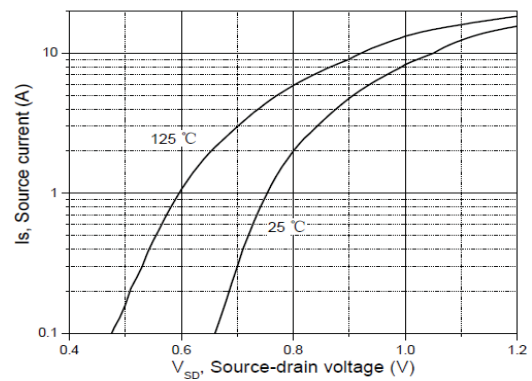


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

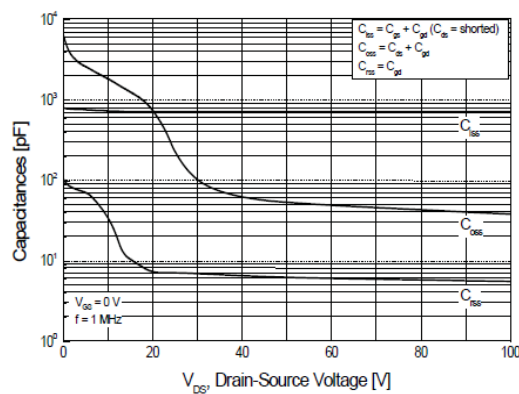


Figure 5. Capacitance Characteristics

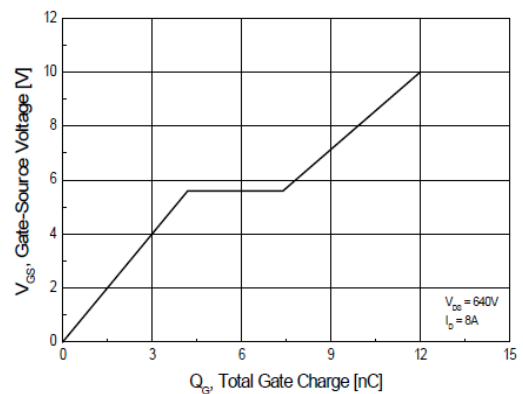


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

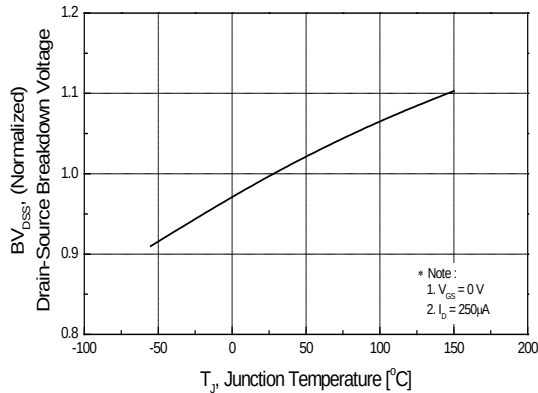


Figure 7. Breakdown Voltage Variation vs Temperature

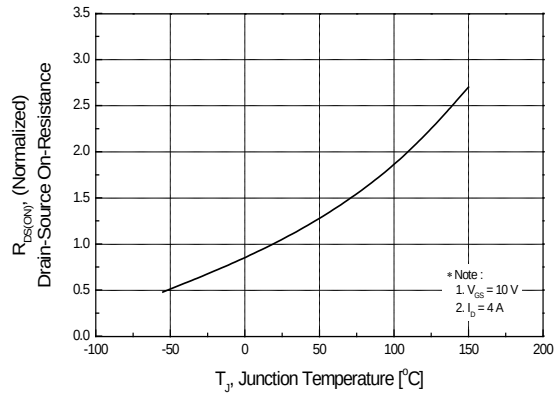


Figure 8. On-Resistance Variation vs Temperature

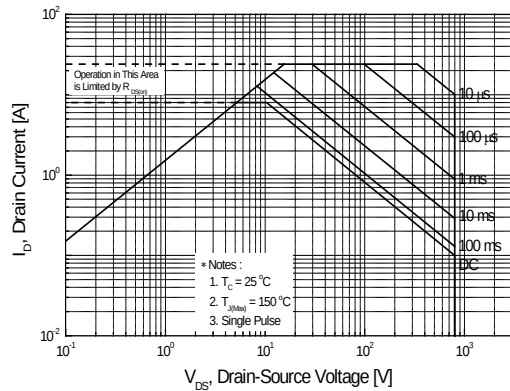


Figure 9. Maximum Safe Operating Area

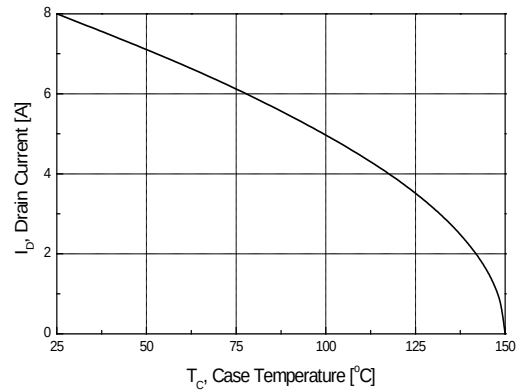


Figure 10. Maximum Drain Current vs Case Temperature

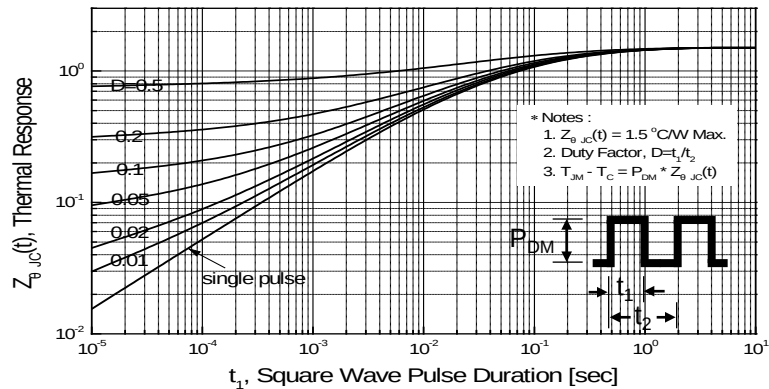


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

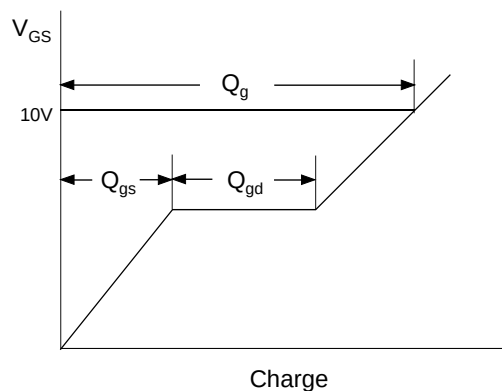
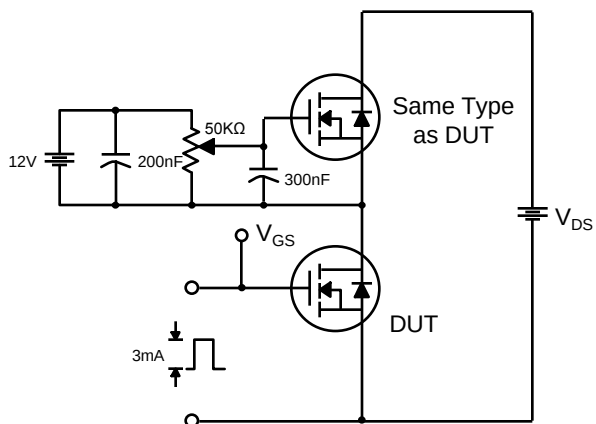


Fig 13. Resistive Switching Test Circuit & Waveforms

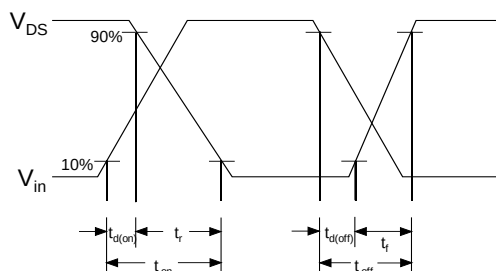
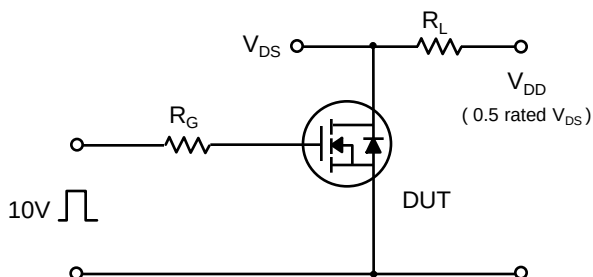


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

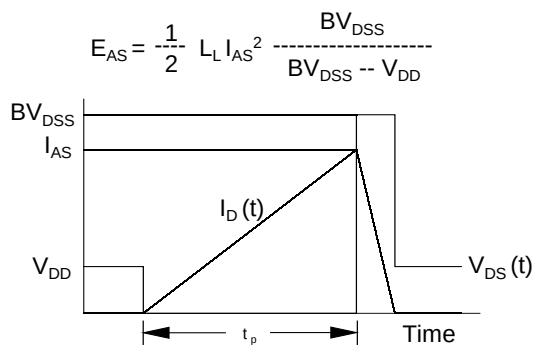
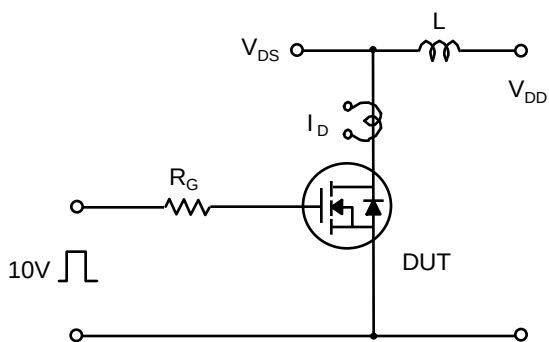
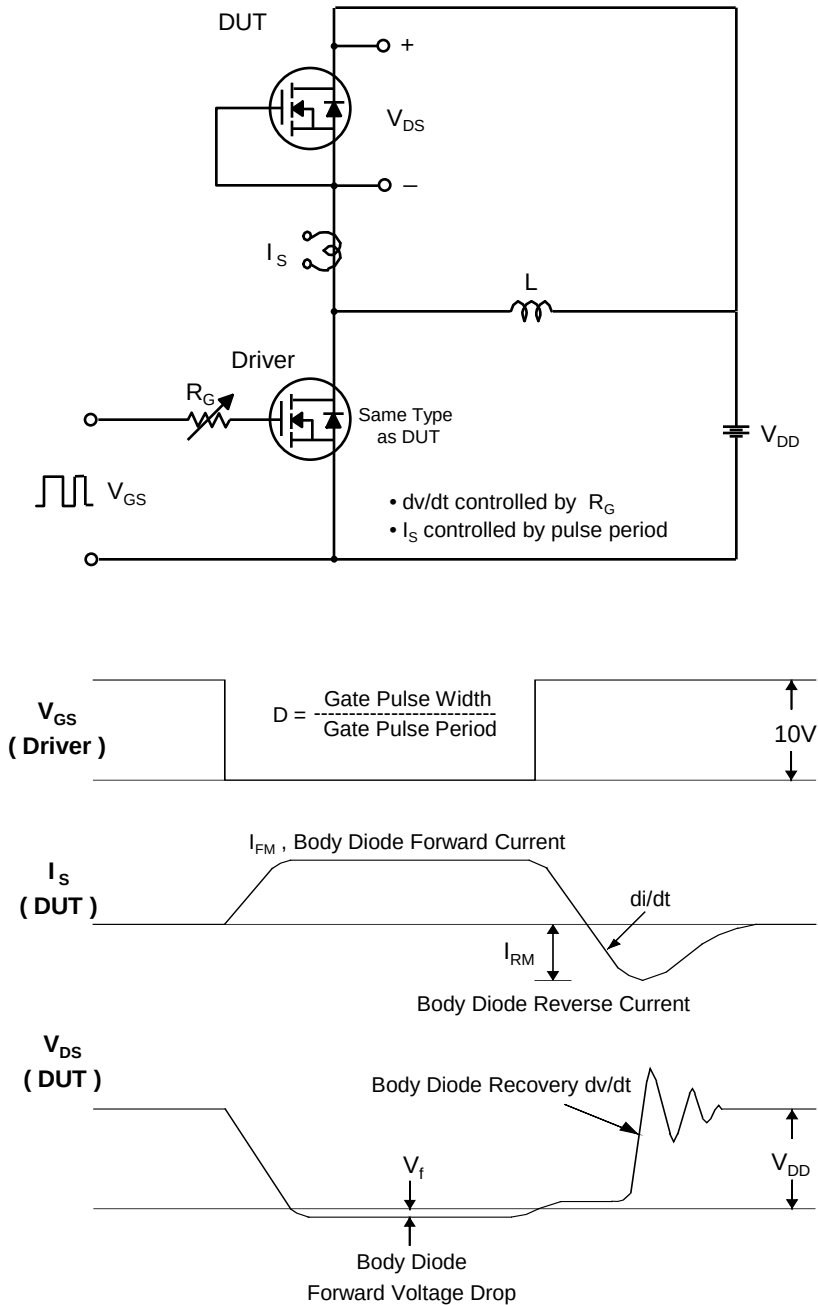
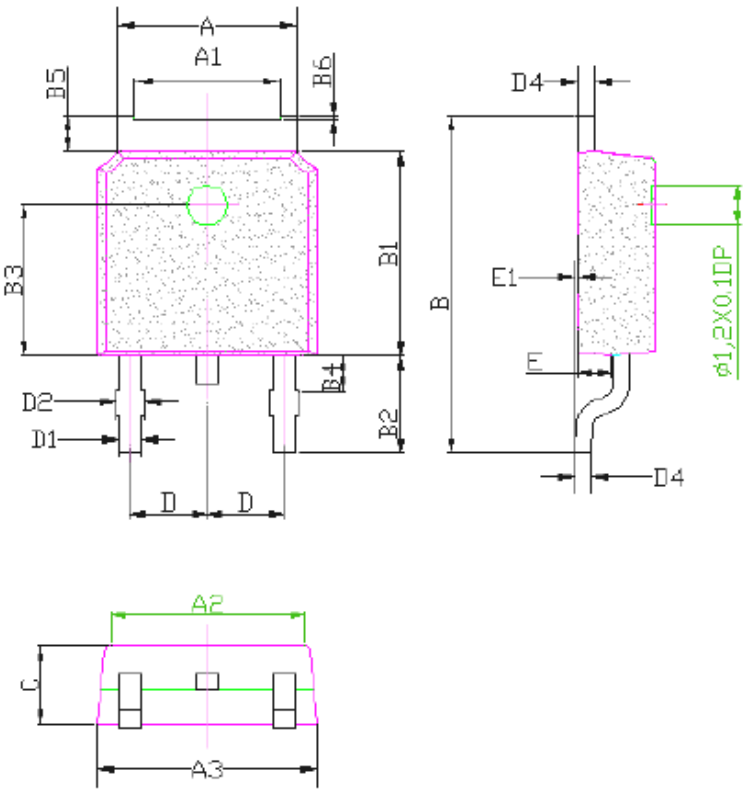


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252L)



DIM	MILLIMETERS
A	5.33 ± 0.2
A1	4.33 ± 0.2
A2	5.78 ± 0.1
A3	6.6 ± 0.2
B	10 ± 0.5
B1	6.1 ± 0.3
B2	2.85 ± 0.5
B3	4.5 ± 0.25
B4	1.0 ± 0.1
B5	1.05 ± 0.1
B6	0.1 ± 0.05
C	2.3 ± 0.2
D	2.286 ± 0.05
D1	0.62 ± 0.15
D2	0.75 ± 0.15
D3	0.5 ± 0.15
D4	0.5 ± 0.15
E	1.01 ± 0.2
E1	0.1 ± 0.05
DIA	$\odot 1.2$ (deep 0.1)

Unit :mm