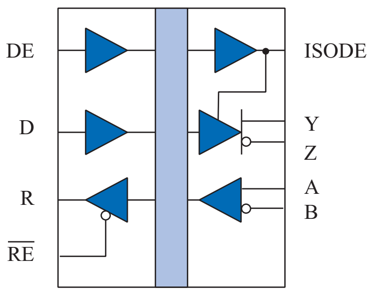
High Speed Isolated RS485/RS422 Transceiver

Functional Diagram



IL3522

IL3522 Receiver

RE	R	$V_{(A-B)}$
H	Z	X
L	H	≥ 200 mV
L	L	≤−200 mV
L	H	Open

IL3522 Driver

DE	D	$V_{(Y-Z)}$
L	X	Z
H	H	≥ 200 mV
H	L	≤−200 mV

H = High Level, L = Low Level
X = Irrelevant, Z = High Impedance

Features

- 40 Mbps data rate
- 20 ns propagation delay
- 1 ns pulse skew
- 6 kV_{RMS} Reinforced Isolation / 12.8 kV surge / 1 kV_{RMS} WV (V-Series)
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- 3 V to 5 V power supplies
- 44000 year barrier life
- 15 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- −40°C to +85°C temperature range
- VDE V 0884-10 certified; UL 1577 recognized
- 16-pin JEDEC-standard True 8™ mm SOIC packages

Applications

- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

The IL3522 is a galvanically isolated, high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The IL3522 delivers an exceptional 2.3 V differential output into a 54 Ω load over the supply range of 4.5 V to 5.5 V. This provides better data integrity over longer cable lengths, even at data rates as high as 40 Mbps. The device is also compatible with 3 V supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. S

Absolute Maximum Ratings[11]

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature	T_A	−40		85	°C	
Voltage Range at any Bus Pin		−7		12	V	
Supply Voltage [1]	V_{DD1}, V_{DD2}	−0.5		7	V	
Digital Input Voltage		−0.5		V_{DD} + 0.5	V	
Digital Output Voltage		−0.5		V_{DD} + 1	V	
ESD (all bus nodes)		15			kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD1} V_{DD2}	3.0 4.5		5.5 5.5	V	
Input Voltage at any Bus Terminal (separately or common mode)	V_I V_{IC}			12 −7	V	
High-Level Digital Input Voltage	V_{IH}	2.4 3.0		V_{DD1}	V	V_{DD1} = 3.3 V V_{DD1} = 5.0 V
Low-Level Digital Input Voltage	V_{IL}	0		0.8	V	
Differential Input Voltage [2]	V_{ID}			+12/−7	V	
High-Level Output Current (Driver)	I_{OH}			60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}			8	mA	
Low-Level Output Current (Driver)	I_{OL}	−60			mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	−8			mA	
Ambient Operating Temperature	T_A	−40		85	°C	
Digital Input Signal Rise and Fall Times	t_{IR}, t_{IF}	DC Stable				

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Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)			8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.013	0.016		mm	
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		7		pF	f = 1 MHz
Leakage Current				0.2		μA_{RMS}	240 V_{RMS}, 60 Hz
Comparative Tracking Index		CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Surge Immunity ("V" Versions)		V_{IOSM}	12.8			kV_{PK}	Per IEC 61000-4-5
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending)

V-Series (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}) 1000 V_{RMS} (1415 V_{PK}); reinforced insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 6000 V_{RMS}
- Surge immunity (V_{IOSM}) 12.8 kV_{PK}
- Surge rating 8 kV
- Transient overvoltage (V_{IOTM}) 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}) 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-3	SOIC	150 V_{RMS}
None	Wide-body SOIC/True 8™	300 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)

Standard isolation grade

Each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute

V-Series isolation grade

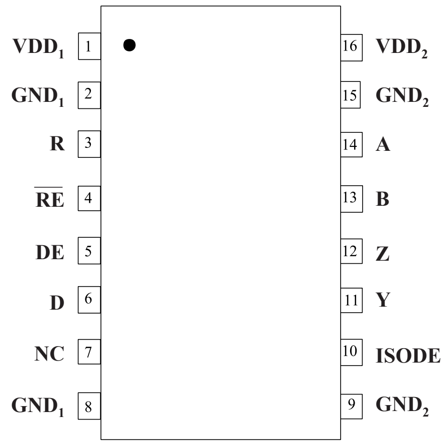
6 kV rating; tested at 7.2 kV_{RMS} (10.2 kV_{PK}) for 1 second; each lot sample tested at 6 kV_{RMS} (8485 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL3522 Pin Connections

1	V_{DD1}	Input Power Supply
2	GND_1	Input Power Supply Ground Return (pin 2 is internally connected to pin 8)
3	R	Output Data from Bus
4	$\overline{RE}$	Read Data Enable (if $\overline{RE}$ is high, R = high impedance)
5	DE	Drive Enable
6	D	Data Input to Bus
7	NC	No Internal Connection
8	GND_1	Input Power Supply Ground Return (pin 8 is internally connected to pin 2)
9	GND_2	Output Power Supply Ground Return (pin 9 is internally connected to pin 15)
10	ISODE	Isolated DE Output for use in Profibus applications where the state of the isolated drive enable node needs to be monitored
11	Y	Y Bus (Drive – True)
12	Z	Z Bus (Drive – Inverse)
13	B	B Bus (Receive – Inverse)
14	A	A Bus (Receive – True)
15	GND_2	Output Power Supply Ground Return (pin 15 is internally connected to pin 9)
16	V_{DD2}	Output Power Supply



IL3522

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Driver Section

Electrical Specifications are T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V, unless otherwise stated.

Parameters	Symbol	Min.	Typ.[5]	Max.	Units	Test Conditions
Input Clamp Voltage	V_{IK}			−1.5	V	$I_L = -18$ mA
Output voltage	V_O			V_{DD}	V	$I_O = 0$
Differential Output Voltage[12]	$\lvert V_{OD1}\rvert$			V_{DD}	V	$I_O = 0$
Differential Output Voltage[12]	$\lvert V_{OD2}\rvert$	2.5	3	5	V	R_L = 54 Ω, V_{DD} = 5 V
Differential Output Voltage[12, 6]	V_{OD3}	2.3		5	V	R_L = 54 Ω, V_{DD} = 4.5 V
Change in Magnitude of Differential Output Voltage[7]	$\Delta\lvert V_{OD}\rvert$			±0.2	V	R_L = 54 Ω or 100 Ω
Common Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω
Change in Magnitude of Common Mode Output Voltage[7]	$\Delta\lvert V_{OC}\rvert$			±0.2	V	R_L = 54 Ω or 100 Ω
Output Current[4]	I_O			1 −0.8	mA	Output Disabled, V_O = 12 $V_O = -7$
High Level Input Current	I_{IH}			10	µA	V_I = 3.5 V
Low Level Input Current	I_{IL}			−10	µA	V_I = 0.4 V
Absolute |Short-circuit Output Current|	I_{OS}			250	mA	−7 V > V_O < 12 V
Supply Current V_{DD1} = +5 V V_{DD1} = +3.3 V	I_{DD1} I_{DD1}		4 3	6 4	mA	No Load (Outputs Enabled)

Notes (apply to both driver and receiver sections):

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
4. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
5. All typical values are at V_{DD1},V_{DD2} = 5 V or V_{DD1}= 3.3 V and T_A = 25°C.
6. −7 V < V_{CM} < 12 V; 4.5 V < V_{DD} < 5.5 V.
7. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
8. This applies for both power on and power off, refer to ANSI standard RS-485 for exact condition. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.
9. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
10. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
11. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
12. Differential output voltage is measured at terminal Y with respect to Z.
13. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
14. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 6).

Receiver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**[5]	**Max.**	**Units**	**Test Conditions**
Positive-going Input Threshold Voltage[2]	V_{IT+}			0.2	V	−7 V > V_{CM} < 12 V
Negative-going Input Threshold Voltage[2]	V_{IT-}	−0.2			V	−7 V > V_{CM} < 12 V
Hysteresis Voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		40		mV	V_{CM} = 0 V, T = 25°C
High Level Digital Output Voltage	V_{OH}	V_{DD} − 0.2	V_{DD}		V	V_{ID} = 200 mV I_{OH} = −20 µA
Low Level Digital Output Voltage	V_{OL}			0.2	V	V_{ID} = −200 mV I_{OH} = 20 µA
High-impedance-state output current	I_{OZ}			±1	µA	V_O=0.4 to (V_{DD2}−0.5) V
Line Input Current[8]	I_I			1	mA	V_I = 12 V
				−0.8	mA	V_I = −7 V
Input Resistance	R_I	20			kΩ	
Supply Current	I_{DD2}		5	16	mA	No load (Outputs Enabled)

Switching Characteristics

V_{DD1} = 5 V, V_{DD2} = 5 V						
Parameters	**Symbol**	**Min.**	**Typ.**[5]	**Max.**	**Units**	**Test Conditions**
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay[2, 9]	t_{PD}		27	35	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew[2, 10]	$t_{SK}(P)$		1	6	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit[3]	$t_{SK}(LIM)$		2	12	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		15	25	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		15	25	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		15	25	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		15	25	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Parameters	**Symbol**	**Min.**	**Typ.**[5]	**Max.**	**Units**	**Test Conditions**
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay[2, 9]	t_{PD}		30	38	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew[2, 10]	$t_{SK}(P)$		1	6	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit[3]	$t_{SK}(LIM)$		4	12	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		17	27	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		17	27	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		17	27	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		17	27	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns

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Magnetic Field Immunity[13]

V_{DD1} = 5 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	4000	4500		A/m	t_p = 8μs
Damped Oscillatory Magnetic Field	H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[14]	K_X		2.5			
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	1800	2000		A/m	t_p = 8μs
Damped Oscillatory Magnetic Field	H_{OSC}	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[14]	K_X		2.5			

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Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on frequency and time.

Data Rate (Mbps)	I_{DD1}	I_{DD2}
1	100 µA	100 µA
10	1 mA	1 mA
20	2 mA	2 mA
40	4 mA	4 mA

Table 2. Typical Dynamic Supply Currents.

Power Supply Decoupling

Both V_{DD1} and V_{DD2} must be bypassed with 47 nF ceramic capacitors. These should be placed as close as possible to V_{DD} pins for proper operation. Additionally, V_{DD2} should be bypassed with a 10 µF tantalum capacitor.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

DC Correctness

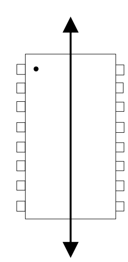
The IL3522 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

Electromagnetic Compatibility

The IL3522 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

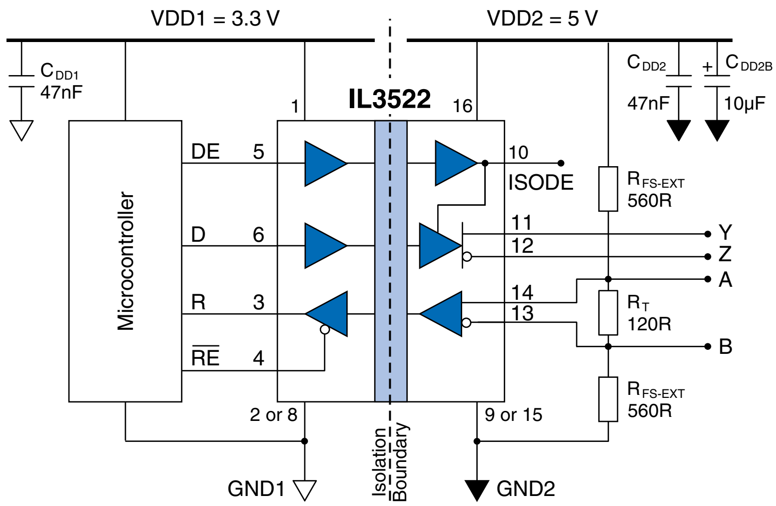
EN50081-1
    Residential, Commercial & Light Industrial
    Methods EN55022, EN55014
EN50082-2: Industrial Environment
    Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)
ENV50204
    Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown in the diagram at right.



Application Information

The following figure shows typical connections to a microcontroller. The schematic includes typical termination and fail-safe resistors, and power supply decoupling capacitors:



Typical IL3522 connections.

Receiver Features
The receiver includes a "fail-safe if open" function that guarantees a high level output if the receiver inputs are unconnected (floating). The receiver output "R" has tri-state capability via the active low $\overline{RE}$ input.

Driver Features
The RS-422 driver is differential output and delivers at least 1.5 V across a 54 Ω load. Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

Receiver Data Rate, Cables and Terminations
The IL3522 is intended for networks up to 4,000 feet (1,200 m), but the maximum data rate decreases as cable length increases. Twisted pair cable should be used in all networks since they tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers.

Fail-Safe Operation

"Fail-safe operation" is defined here as the forcing of a logic high state on the "R" output in response to an open-circuit condition between the "A" and "B" lines of the bus, or when no drivers are active on the bus.

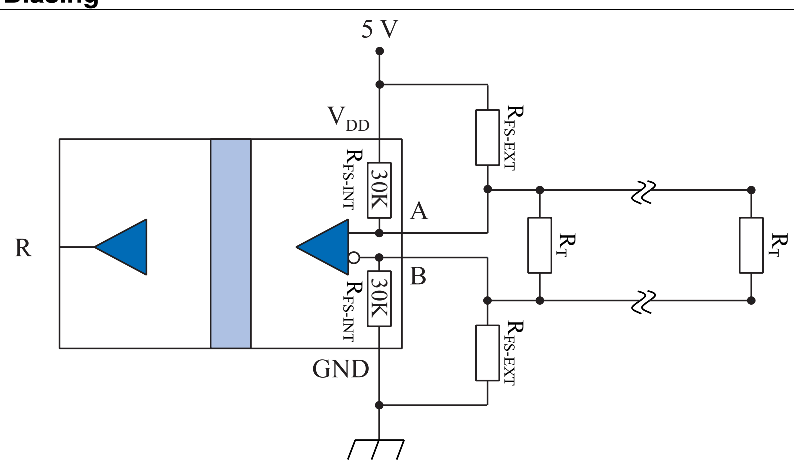
Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL3000-Series Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 kΩ in the receiver section (R_{FS-INT}; see figure below). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire V_{DD} will appear between inputs "A" and "B" if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-422 worst-case Unit Loads of 12 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors, however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors (R_T) on each end of the cable, and four Unit Loads (12 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs "A" and "B" of only about 5 mV. This is not nearly enough to ensure a known state. External fail-safe biasing resistors (R_{FS-EXT}) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-422 standard.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 32 Unit Loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

In the example with two 120 Ω termination resistors and four Unit Loads, 560 Ω external biasing resistors provide more than 200 mV between "A" and "B" with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the table below:

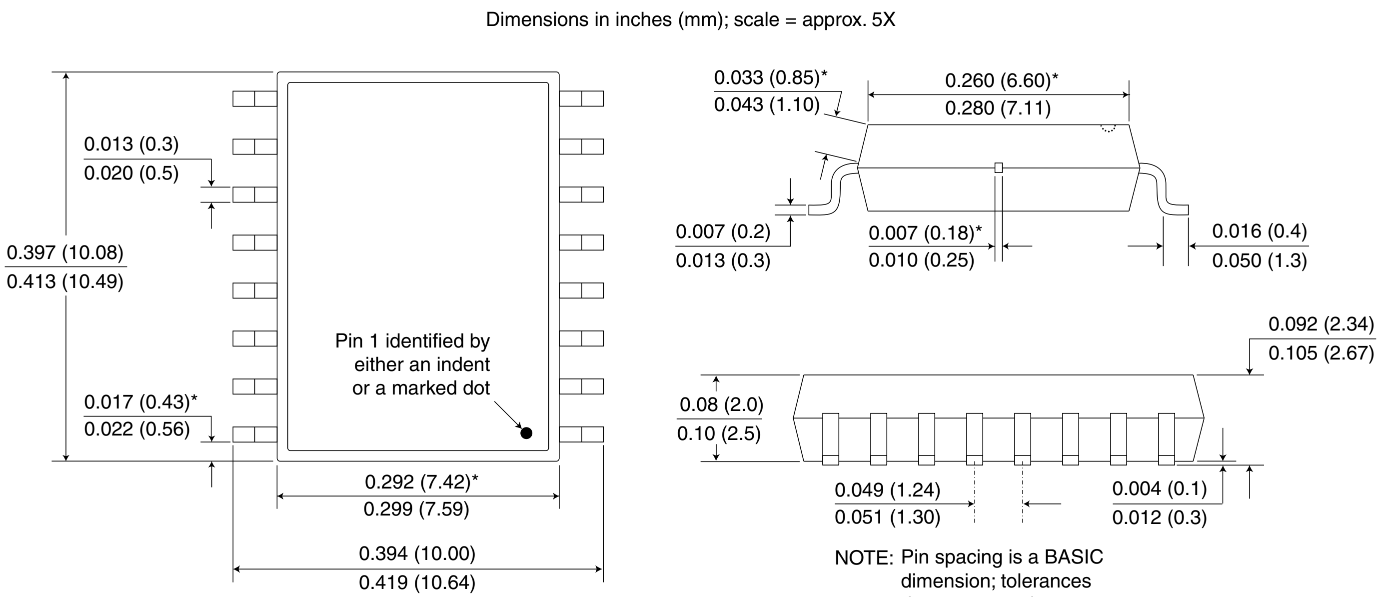
Fail-Safe Biasing



R_{FS-EXT}	R_T	Loading	Nominal V_{A-B} (inactive)	Fail-Safe Operation?
Internal Only	None	Four unit loads (12 kΩ ea.)	238 mV	Yes
Internal Only	120 Ω	Four unit loads (12 kΩ ea.)	5 mV	No
560 Ω	120 Ω	Four unit loads (12 kΩ ea.)	254 mV	Yes
510 Ω	120 Ω	32 unit loads (12 kΩ ea.)	247 mV	Yes

Package Drawing

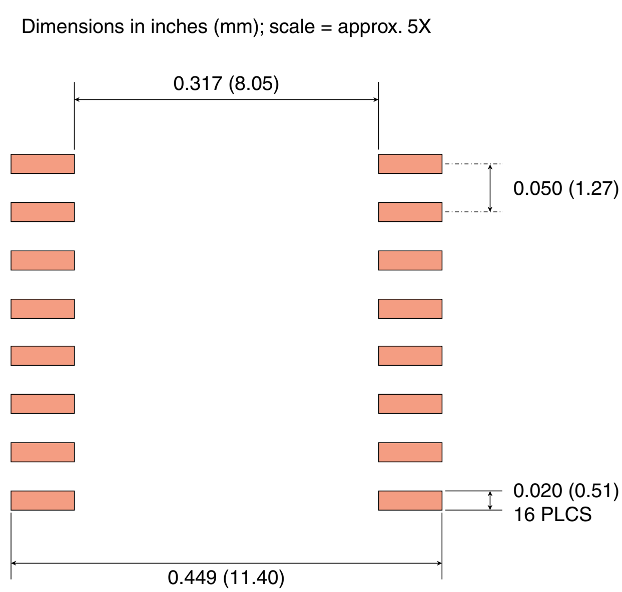
0.3" 16-pin SOIC Package



*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layout

0.15" 16-pin SOIC Pad Layout



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Ordering Information and Valid part Numbers

IL 35 22 V E TR13

Bulk Packaging
Blank = Tube
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Sn/Pb Plating
E = RoHS Compliant

Isolation Grade
Blank = 2.5 kV Isolation / 600 WV
V = 6 kV Isolation / 1 kV WV

Channel Configuration
22 = RS-422

Base Part Number
35 = Digital-In, 40 Mbps Transceiver

Product Family
IL = Isolators

Valid Part Numbers
IL3522
IL3522E
IL3522TR13
IL3522E TR13

IL3522VE
IL3522VE TR13

RoHS COMPLIANT

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Revision History

ISB-DS-001-IL3522-S
- Updated VDE Reinforced Isolation file number and description.

ISB-DS-001-IL3522-R
- Updated VDE certification standard to VDE V 0884-10.
- Upgraded "V" Version Surge Immunity specification to 12.8 kV.
- Upgraded "V" Version VDE 0884-10 rating to reinforced insulation.

ISB-DS-001-IL3522-Q
- Increased V-Series isolation voltage to 6 kV_{RMS}.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 V_{RMS}.

ISB-DS-001-IL3522-P
- Increase V-Series surge voltage specification to 10 kV.
- Upgraded V-Series safety and approval from IEC 60747-5-5 (VDE 0884) to VDE 0884-10.

ISB-DS-001-IL3522-O
- Added V-Series versions (5 kVrms isolation / 1000 Vrms working voltage).

ISB-DS-001-IL3522-N
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.

ISB-DS-001-IL3522-M
- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added transient immunity specifications.
- Added high voltage endurance specification.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

ISB-DS-001-IL3522-L
- Changed title to "Very High Speed Isolated RS485/RS422 Transceiver."
- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DS-001-IL3522-K
- Update terms and conditions.

ISB-DS-001-IL3522-J
- Added clarification of internal ground connections (p. 3).

ISB-DS-001-IL3522-I
- Revised maximum Receiver Section Supply Current to 16 mA.

ISB-DS-001-IL3522-G
- Added bus-protection ESD specification (15 kV).

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NVE Corporation
11409 Valley View Road
Eden Prairie, MN 55344-3617 USA
Telephone: (952) 829-9217
Fax: (952) 829-9189
www.nve.com
e-mail: iso-info@nve.com

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