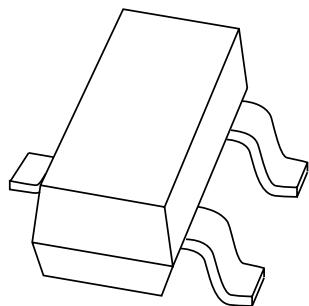


DATA SHEET



PMBT5550 NPN high-voltage transistor

Product data sheet
Supersedes data of 1999 Apr 15

2004 Jan 21

NPN high-voltage transistor**PMBT5550****FEATURES**

- Low current (max. 300 mA)
- Low voltage (max. 140 V).

APPLICATIONS

- Telephony.

DESCRIPTION

NPN high-voltage transistor in a SOT23 plastic package.
PNP complement: PMBT5401.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PMBT5550	*1F

Note

1. * = p : Made in Hong Kong.
- * = t : Made in Malaysia.
- * = W : Made in China.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector

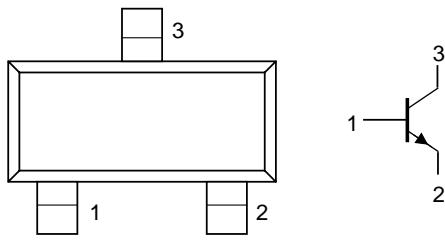


Fig.1 Simplified outline (SOT23) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PMBT5550	–	plastic surface mounted package; 3 leads	SOT23

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	160	V
V_{CEO}	collector-emitter voltage	open base	–	140	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	300	mA
I_{CM}	peak collector current		–	600	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25^\circ\text{C}$; note 1	–	250	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		-65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

NPN high-voltage transistor

PMBT5550

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	500	K/W

Note

- Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$I_E = 0; V_{CB} = 100 \text{ V}$	–	50	nA
		$I_E = 0; V_{CB} = 100 \text{ V}; T_{amb} = 100^\circ\text{C}$	–	50	μA
I_{EBO}	emitter-base cut-off current	$I_C = 0; V_{EB} = 4 \text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}; (\text{see Fig.2})$			
		$I_C = 1 \text{ mA}$	60	–	
		$I_C = 10 \text{ mA}$	60	250	
		$I_C = 50 \text{ mA}$	20	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 1 \text{ mA}$	–	150	mV
		$I_C = 50 \text{ mA}; I_B = 5 \text{ mA}$	–	250	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 1 \text{ mA}$	–	1	V
		$I_C = 50 \text{ mA}; I_B = 5 \text{ mA}$	–	1.2	V
C_c	collector capacitance	$I_E = I_e = 0; V_{CB} = 10 \text{ V}; f = 1 \text{ MHz}$	–	6	pF
C_e	emitter capacitance	$I_C = I_c = 0; V_{EB} = 0.5 \text{ V}; f = 1 \text{ MHz}$	–	30	pF
f_T	transition frequency	$I_C = 10 \text{ mA}; V_{CE} = 10 \text{ V}; f = 100 \text{ MHz}$	100	300	MHz
F	noise figure	$I_C = 200 \mu\text{A}; V_{CE} = 5 \text{ V}; R_S = 2 \text{ k}\Omega; f = 10 \text{ Hz to } 15.7 \text{ kHz}$	–	10	dB

NPN high-voltage transistor

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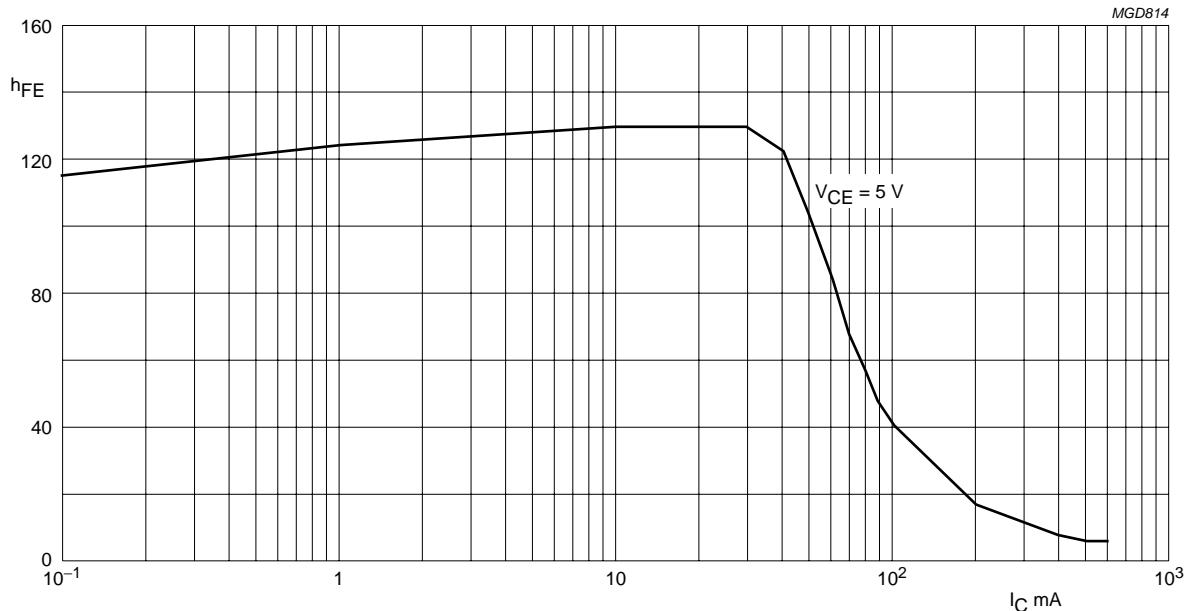


Fig.2 DC current gain; typical values.

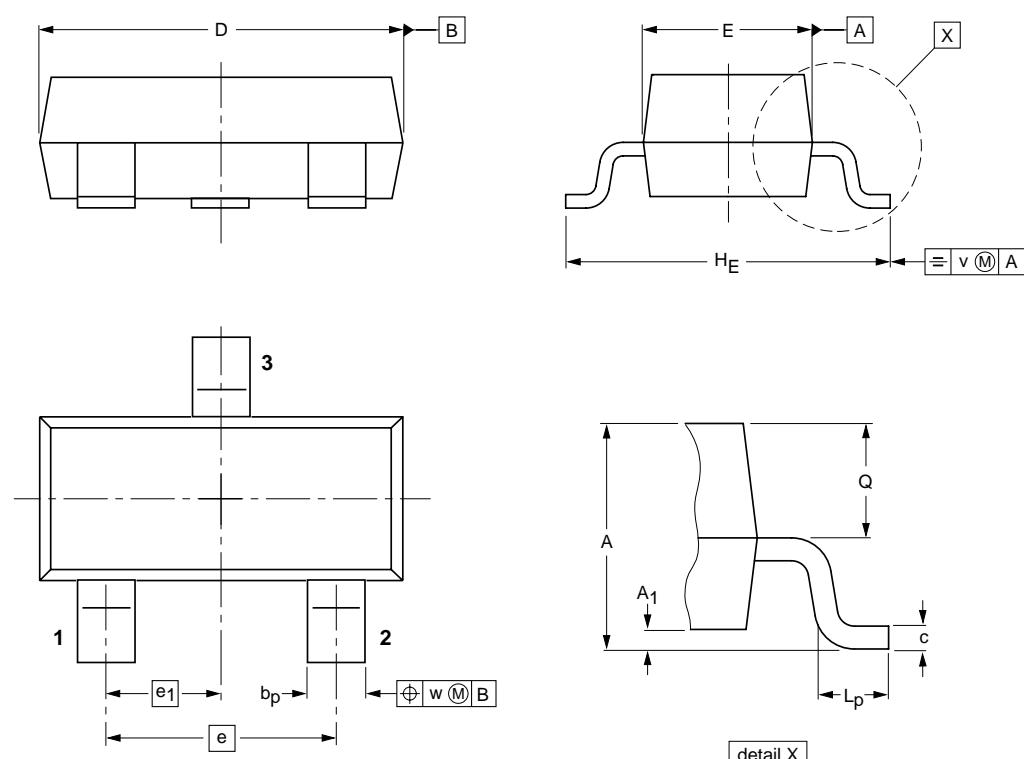
NPN high-voltage transistor

PMBT5550

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	l _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				-04-11-04- 06-03-16