

DATA SHEET

PDTC144W series

NPN resistor-equipped transistors;

$R1 = 47\text{ k}\Omega$, $R2 = 22\text{ k}\Omega$

Product data sheet
Supersedes data of 2004 Mar 23

2004 Aug 17

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FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	47	–	k Ω
R2	bias resistor	22	–	k Ω

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC144WE	SOT416	SC-75	42	PDTA144WE
PDTC144WEF	SOT490	SC-89	34	PDTA144WEF
PDTC144WK	SOT346	SC-59	41	PDTA144WK
PDTC144WM	SOT883	SC-101	DD	PDTA144WM
PDTC144WS	SOT54 (TO-92)	SC-43	TC144W	PDTA144WS
PDTC144WT	SOT23	–	*20 ⁽¹⁾	PDTA144WT
PDTC144WU	SOT323	SC-70	*20 ⁽¹⁾	PDTA144WU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC144WS	MAM364	1 2 3	base collector emitter
PDTC144WE PDTC144WEF PDTC144WK PDTC144WT PDTC144WU	Top view MDB269	1 2 3	base emitter collector
PDTC144WM	bottom view MHC506	1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC144WE	–	plastic surface mounted package; 3 leads	SOT416
PDTC144WEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC144WK	–	plastic surface mounted package; 3 leads	SOT346
PDTC144WM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC144WS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC144WT	–	plastic surface mounted package; 3 leads	SOT23
PDTC144WU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _i	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
	SOT416	note 1	–	150	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W
	SOT416	note 1	833	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	–	–	110	μ A
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	60	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	–	–	150	mV
V _{i(off)}	input-off voltage	I _C = 100 μ A; V _{CE} = 5 V	–	1.7	1.2	V
V _{i(on)}	input-on voltage	I _C = 2 mA; V _{CE} = 0.3 V	4	2.7	–	V
R1	input resistor		33	47	61	k Ω
$\frac{R_2}{R_1}$	resistor ratio		0.37	0.47	0.57	
C _c	collector capacitance	I _E = I _e = 0 A; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

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PACKAGE OUTLINES

Plastic surface-mounted package; 3 leads

SOT416

Technical drawing of the SOT416 package showing top, bottom, and side views with dimensions D, B, E, A, H_E, Q, A₁, c, L_p, v, w, e, e₁, b_p, and detail X.

0 0.5 1 mm
scale

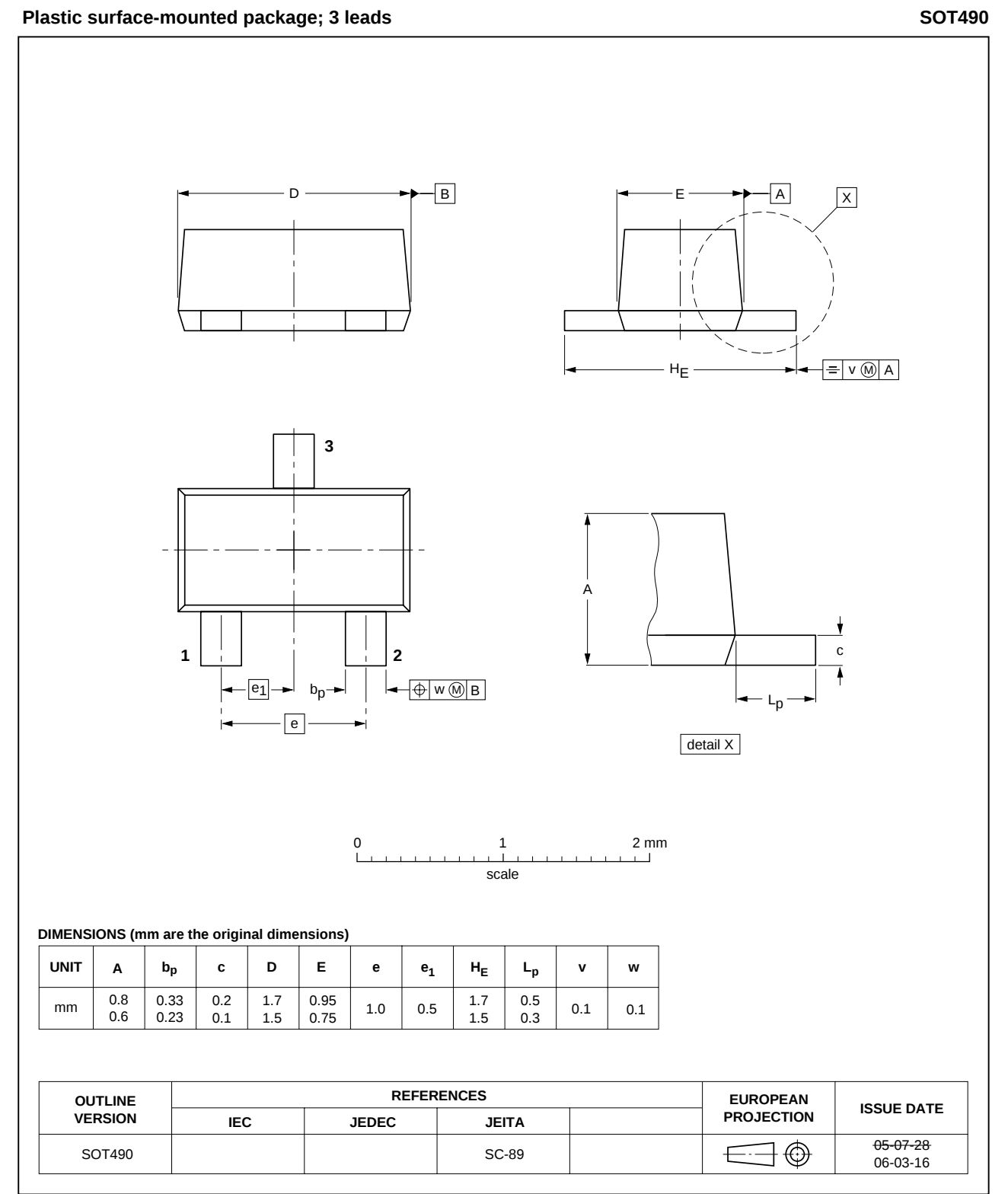
DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT416			SC-75			04-11-04 06-03-16

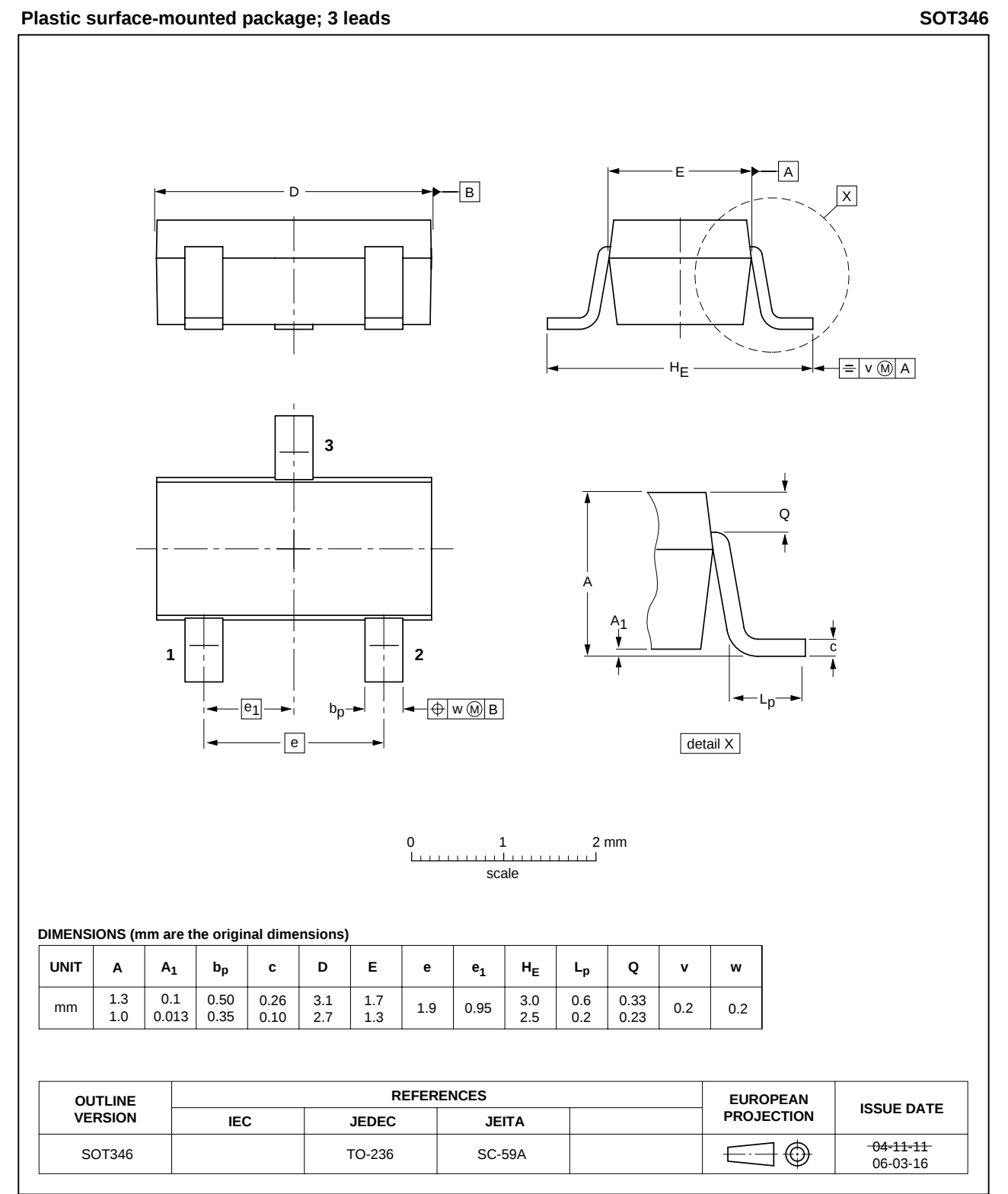
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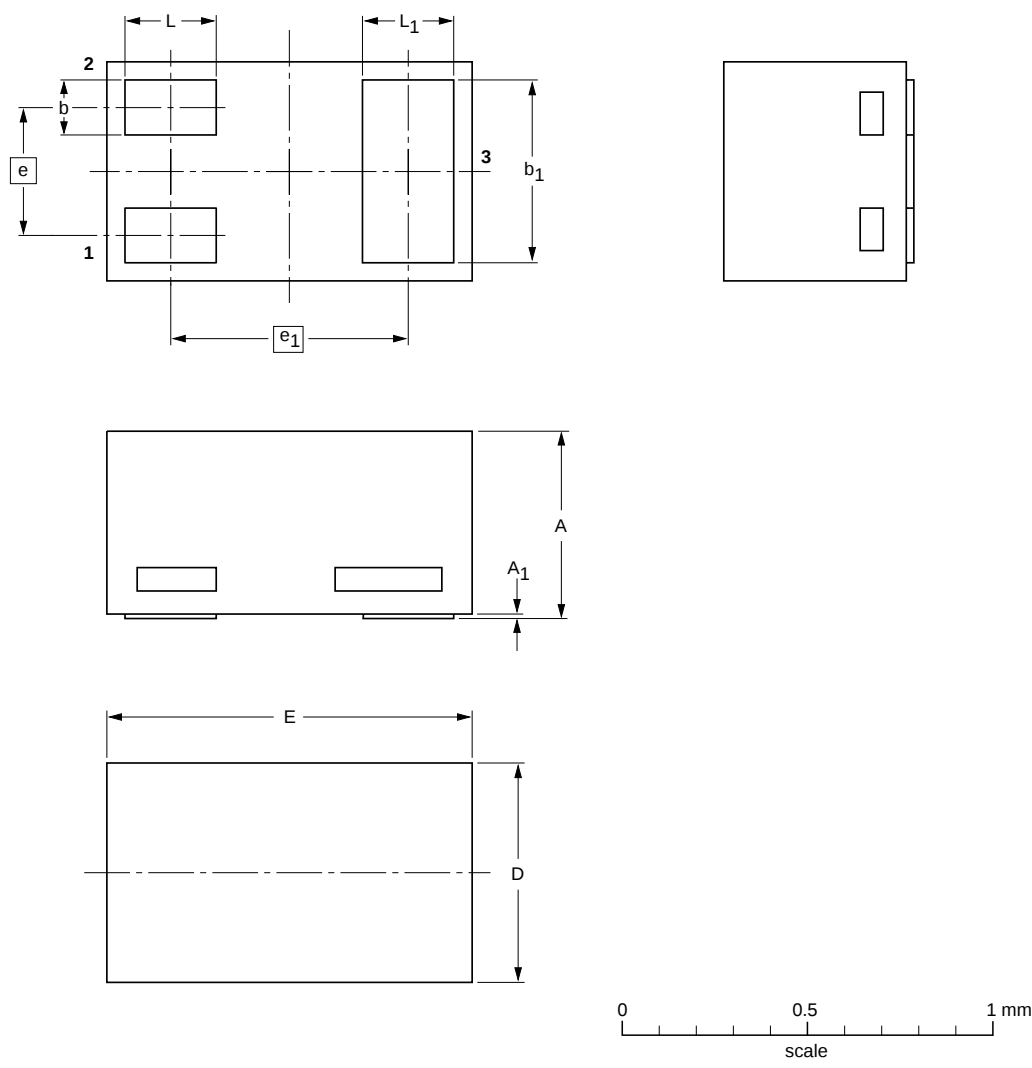


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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note
1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05 03-04-03

NPN resistor-equipped transistors;
R1 = 47 kΩ, R2 = 22 kΩ

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Plastic single-ended leaded (through hole) package; 3 leads

SOT54

Technical drawing of the SOT54 package showing top, side, and lead views with dimensions A, b, b₁, c, D, d, E, e, e₁, L, L₁.

0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

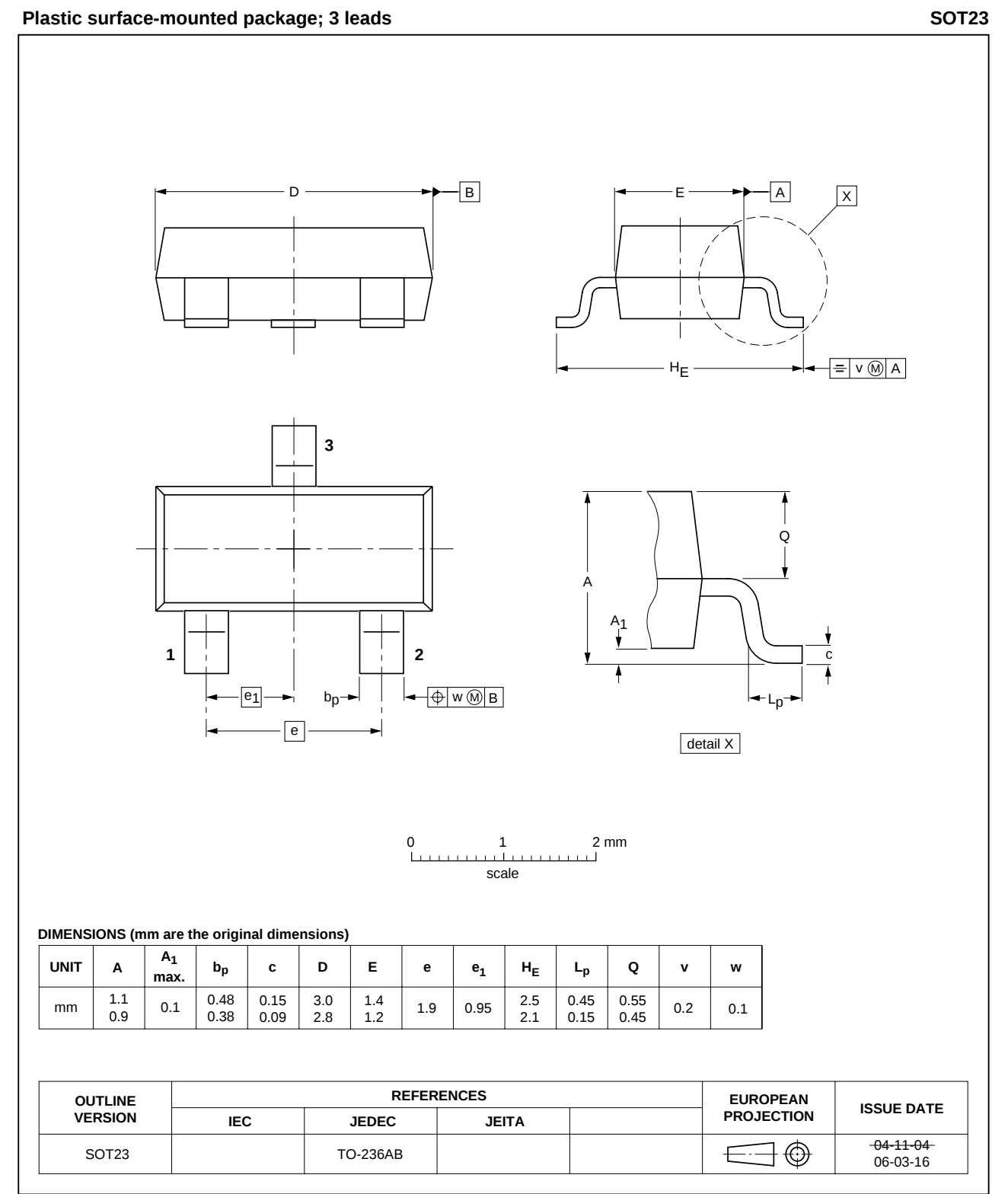
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			04-06-28 04-11-16

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