International
IOR Rectifier

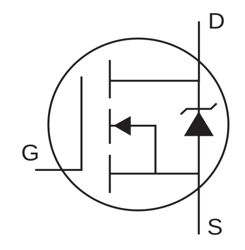
PD - 94754

AUTOMOTIVE MOSFET

IRFR120Z
IRFU120Z

HEXFET® Power MOSFET

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

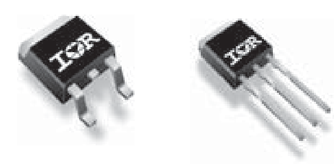


V_{DSS} = 100V

$R_{DS(on)}$ = 190mΩ

I_D = 8.7A

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



D-Pak IRFR120Z   I-Pak IRFU120Z

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	8.7	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	6.1	
I_{DM}	Pulsed Drain Current ①	35	
P_D @T_C = 25°C	Power Dissipation	35	W
	Linear Derating Factor	0.23	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy②	18	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	20	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	4.28	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ⑦	——	40	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

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10/3/03

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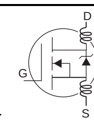
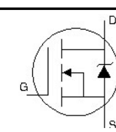
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.084	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	150	190	mΩ	V_{GS} = 10V, I_D = 5.2A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	16	–––	–––	S	V_{DS} = 25V, I_D = 5.2A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	µA	V_{DS} = 100V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-200		V_{GS} = -20V
Q_g	Total Gate Charge	–––	6.9	10	nC	I_D = 5.2A
Q_{gs}	Gate-to-Source Charge	–––	1.6	–––		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	3.1	–––		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	–––	8.3	–––	ns	V_{DD} = 50V
t_r	Rise Time	–––	26	–––		I_D = 5.2A
$t_{d(off)}$	Turn-Off Delay Time	–––	27	–––		R_G = 53 Ω
t_f	Fall Time	–––	23	–––		V_{GS} = 10V ③
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	–––	7.5	–––		from package and center of die contact
C_{iss}	Input Capacitance	–––	310	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	41	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	24	–––		f = 1.0MHz
C_{oss}	Output Capacitance	–––	150	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	26	–––		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	57	–––		V_{GS} = 0V, V_{DS} = 0V to 80V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	8.7	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	35		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 5.2A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	24	36	ns	T_J = 25°C, I_F = 5.2A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	–––	23	35	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

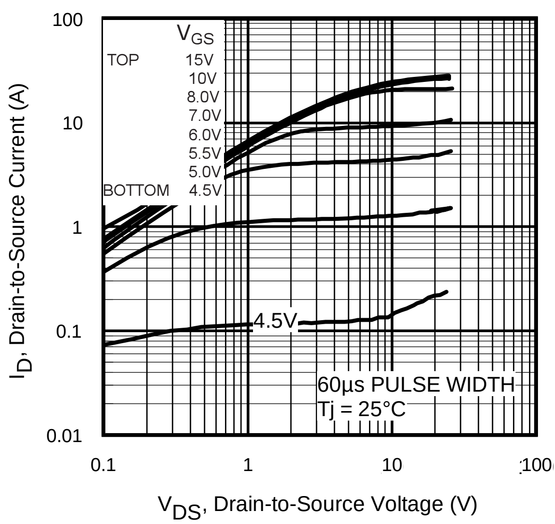


Fig 1. Typical Output Characteristics

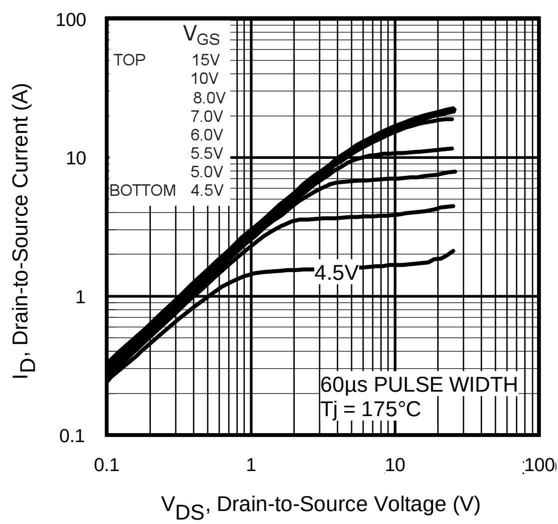


Fig 2. Typical Output Characteristics

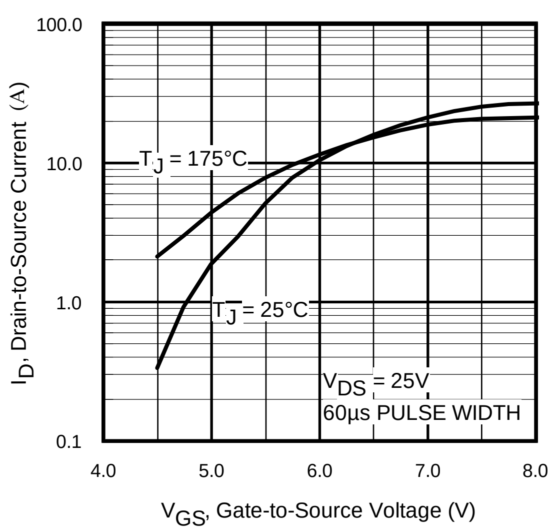


Fig 3. Typical Transfer Characteristics

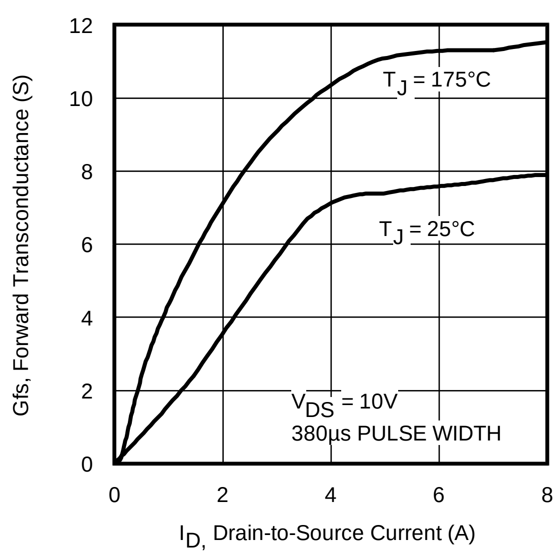


Fig 4. Typical Forward Transconductance
Vs. Drain Current

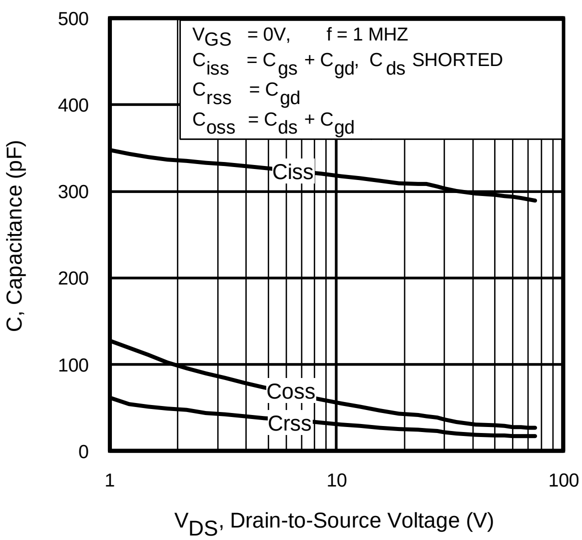


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

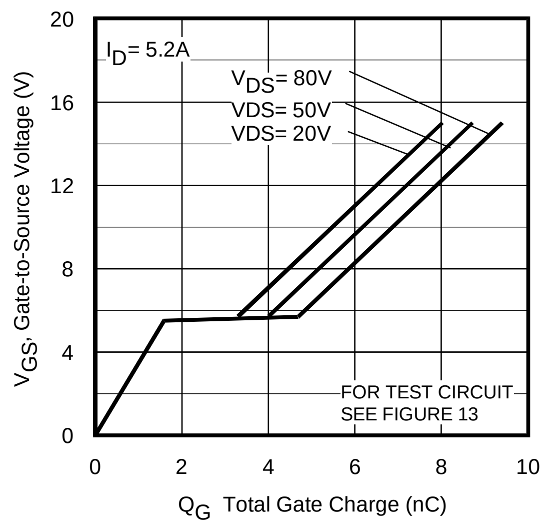


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

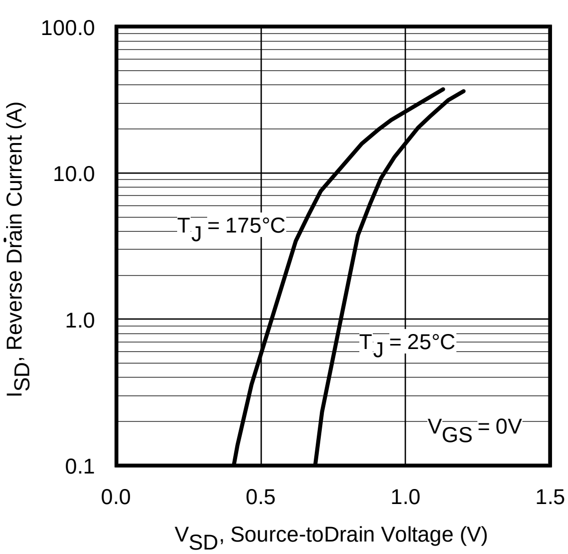


Fig 7. Typical Source-Drain Diode Forward Voltage

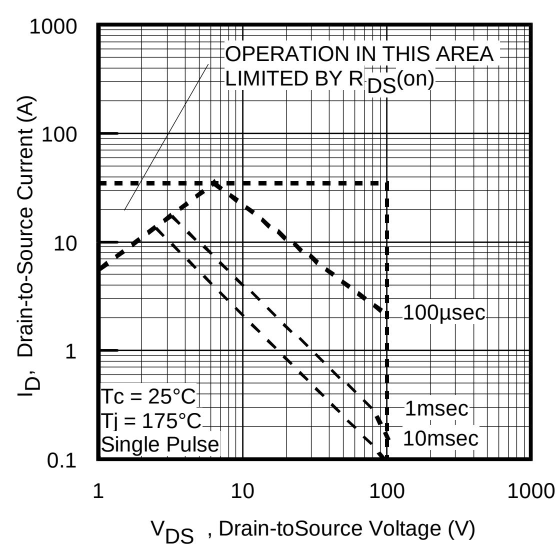


Fig 8. Maximum Safe Operating Area

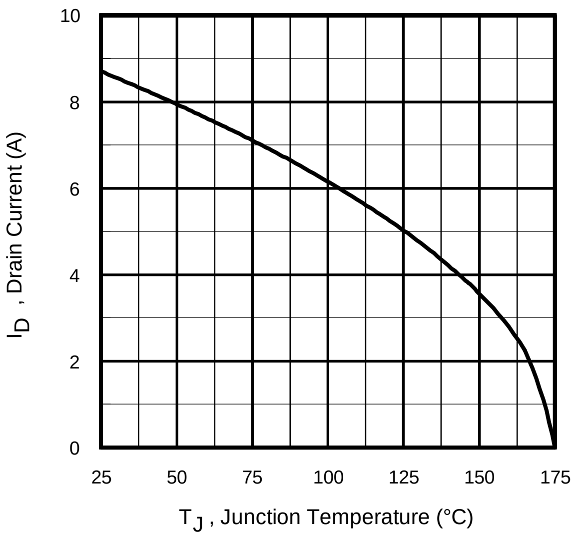


Fig 9. Maximum Drain Current Vs. Case Temperature

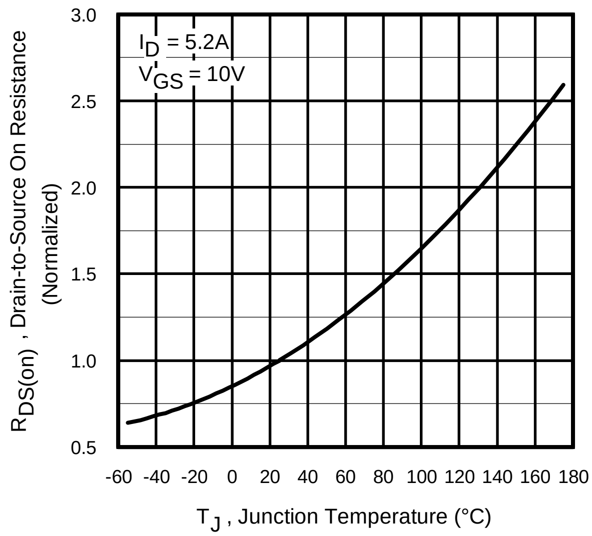
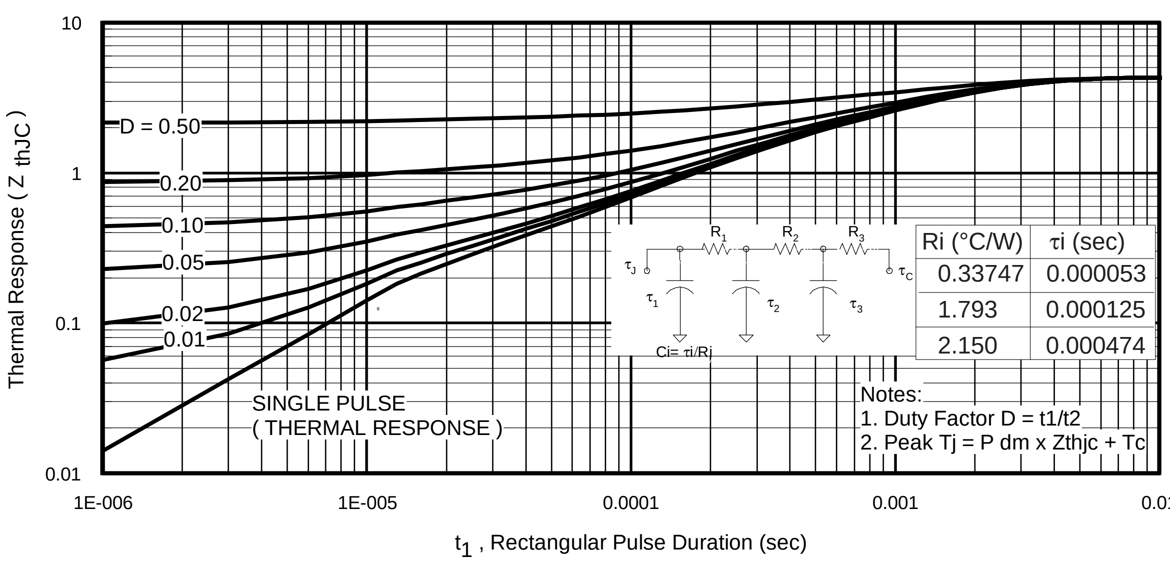


Fig 10. Normalized On-Resistance Vs. Temperature



Ri (°C/W)	τi (sec)
0.33747	0.000053
1.793	0.000125
2.150	0.000474

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

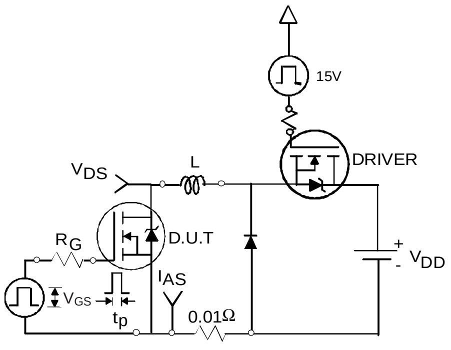


Fig 12a. Unclamped Inductive Test Circuit

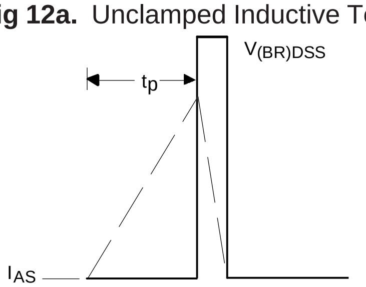


Fig 12b. Unclamped Inductive Waveforms

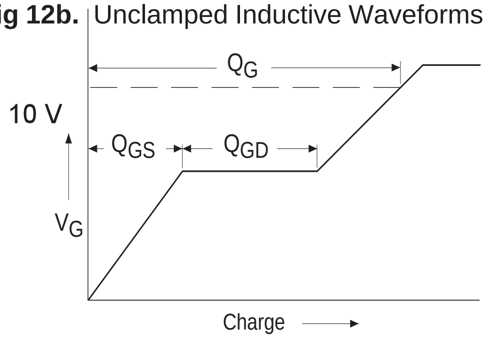


Fig 13a. Basic Gate Charge Waveform

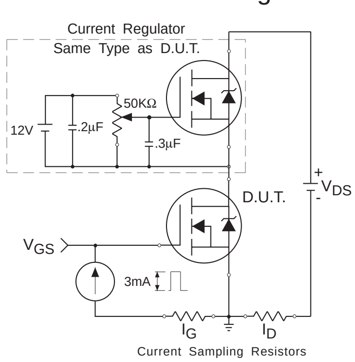


Fig 13b. Gate Charge Test Circuit

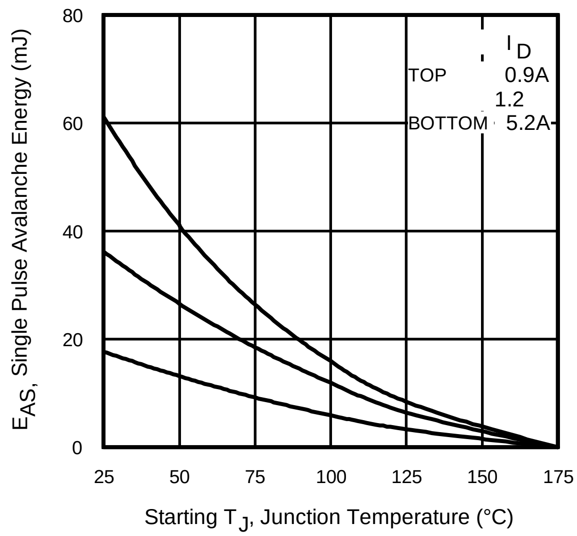


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

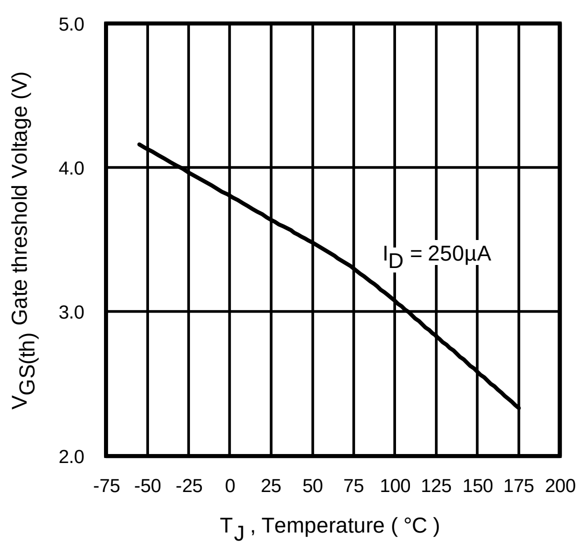


Fig 14. Threshold Voltage Vs. Temperature

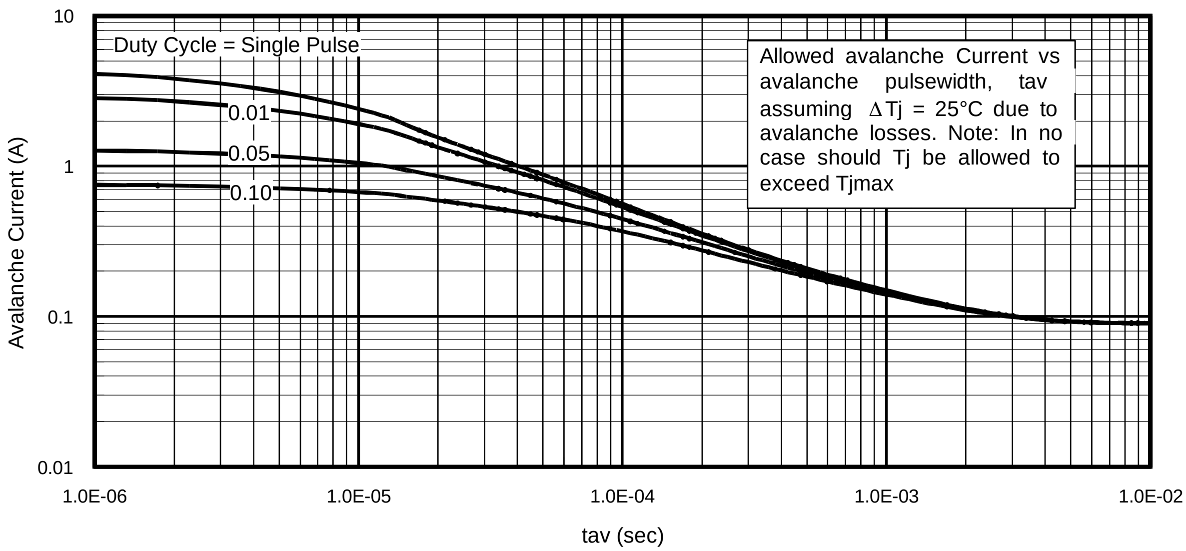


Fig 15. Typical Avalanche Current Vs.Pulsewidth

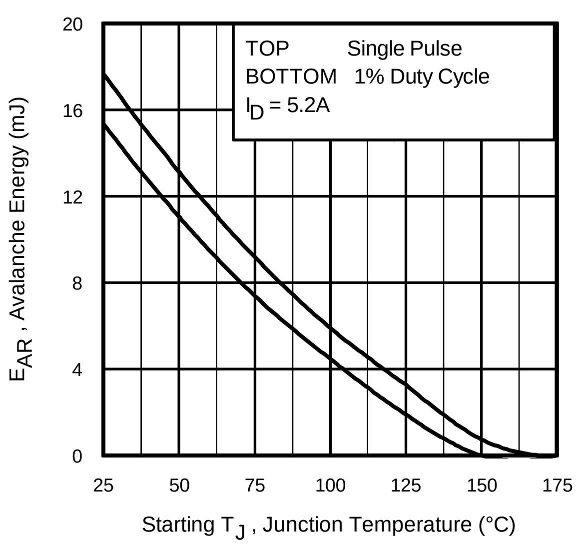


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

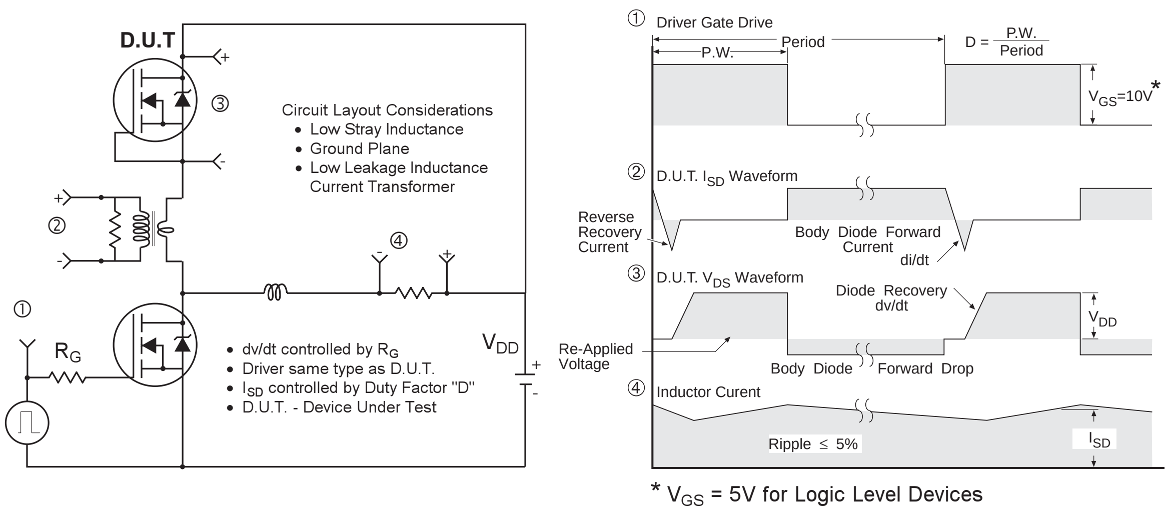


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

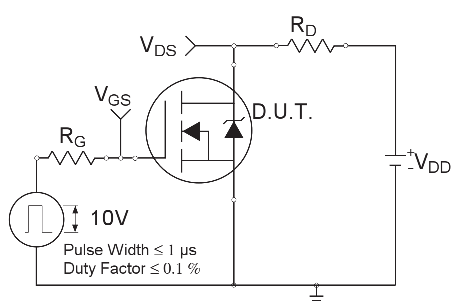


Fig 18a. Switching Time Test Circuit

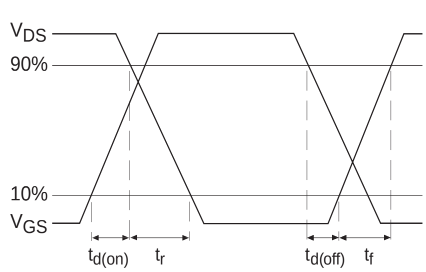
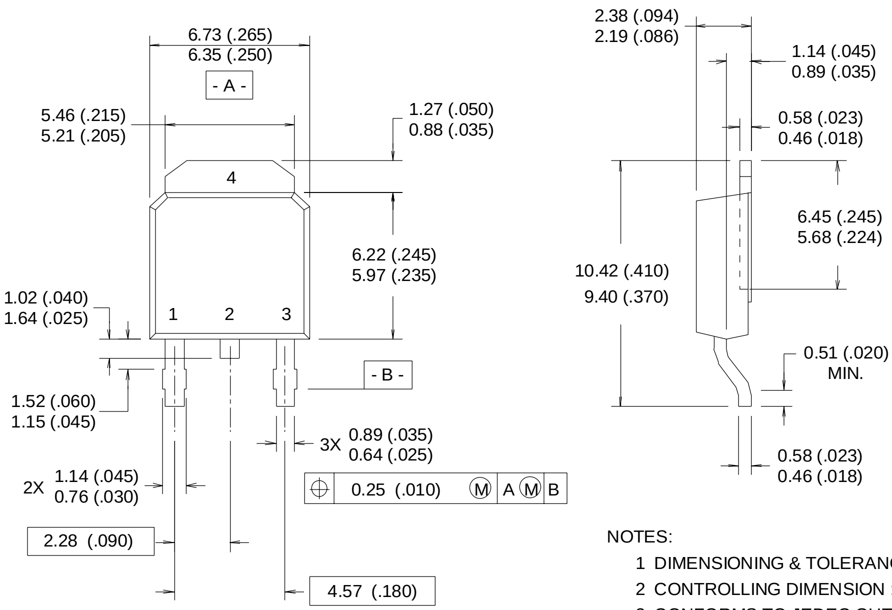


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

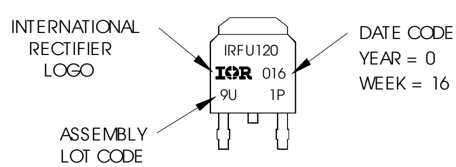
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

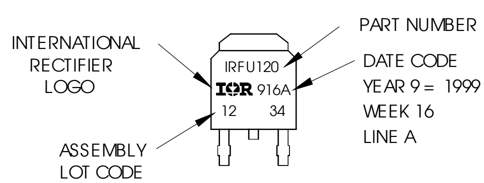
Notes : This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



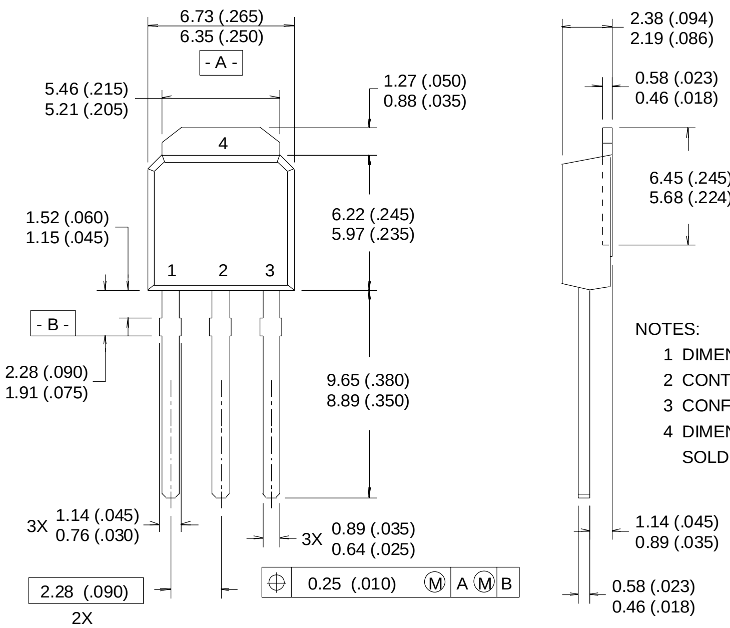
Notes : This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



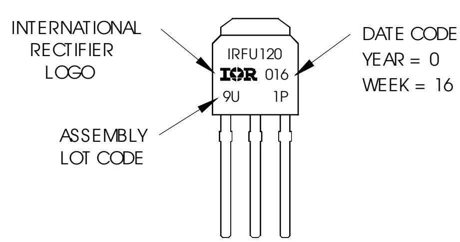
LEAD ASSIGNMENTS
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION : INCH.
3. CONFORMS TO JEDEC OUTLINE TO-252AA.
4. DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

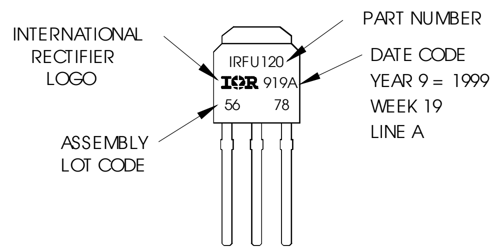
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



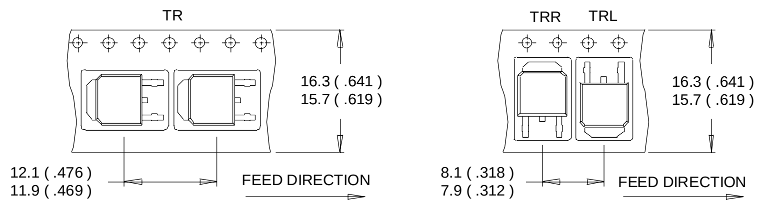
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

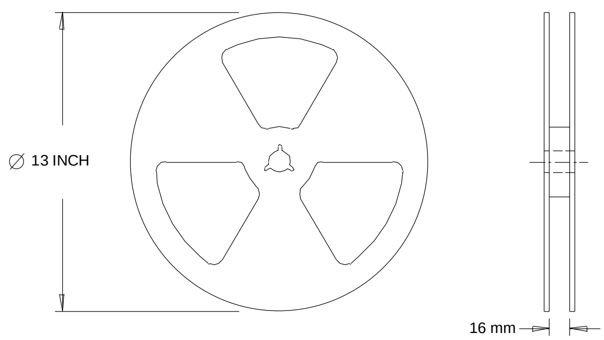


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 1.29mH R_G = 25Ω, I_{AS} = 5.2A, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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