International
IOR Rectifier

PD - 97782A

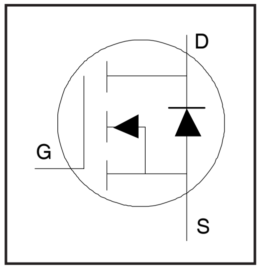
StrongIRFET™

IRFB7430PbF

HEXFET® Power MOSFET

Applications

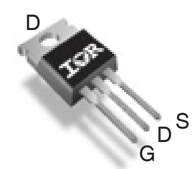
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}		40V
$R_{DS(on)}$	typ.	1.0mΩ
	max.	1.3mΩ
I_D (Silicon Limited)		409A①
I_D (Package Limited)		195A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



TO-220AB
IRFB7430PbF

G	D	S
Gate	Drain	Source

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRFB7430PbF	TO-220	Tube	50	IRFB7430PbF

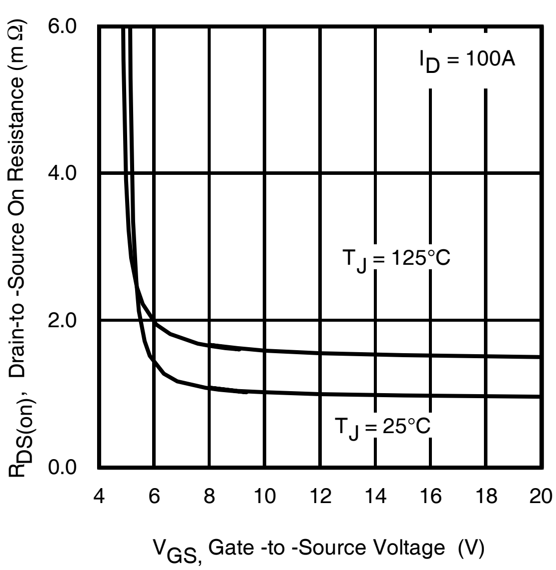


Fig 1. Typical On-Resistance vs. Gate Voltage

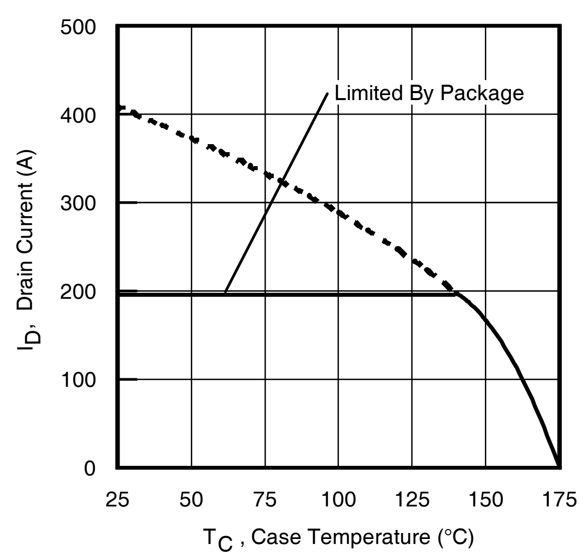


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	409 ①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	289 ①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	1524	
P_D @T_C = 25°C	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf· in (1.1N· m)	

Avalanche Characteristics

Symbol	Parameter	Max.	Units
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	760	mJ
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑨	1360	
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	–––	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.014	–––	V/°C	Reference to 25°C, I_D = 1.0mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	1.0	1.3	mΩ	V_{GS} = 10V, I_D = 100A ⑤
		–––	1.2	–––		V_{GS} = 6.0V, I_D = 50A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	–––	3.9	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		–––	–––	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	–––	2.1	–––	Ω	

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.15mH R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

④ I_{SD} ≤ 100A, di/dt ≤ 990A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

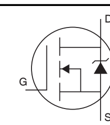
⑧ R_θ is measured at T_J approximately 90°C..

⑨ This value determined from sample failure population, starting T_J = 25°C, L= 0.15mH, R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	150	–––	–––	S	V_{DS} = 10V, I_D = 100A
Q_g	Total Gate Charge	–––	300	460	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	–––	77	–––		V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	98	–––		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	–––	202	–––		I_D = 100A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	–––	32	–––	ns	V_{DD} = 20V
t_r	Rise Time	–––	105	–––		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	–––	160	–––		R_G = 2.7Ω
t_f	Fall Time	–––	100	–––		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	–––	14240	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	2130	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	1460	–––		ƒ = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ⑦	–––	2605	–––		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥	–––	2920	–––		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	394①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	–––	–––	1576	A	
V_{SD}	Diode Forward Voltage	–––	0.86	1.2	V	T_J = 25°C, I_S = 100A, V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery ④	–––	2.7	–––	V/ns	T_J = 175°C, I_S = 100A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	–––	52	–––	ns	T_J = 25°C V_R = 34V,
		–––	52	–––		T_J = 125°C I_F = 100A
Q_{rr}	Reverse Recovery Charge	–––	97	–––	nC	T_J = 25°C di/dt = 100A/μs ⑤
		–––	97	–––		T_J = 125°C
I_{RRM}	Reverse Recovery Current	–––	2.3	–––	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

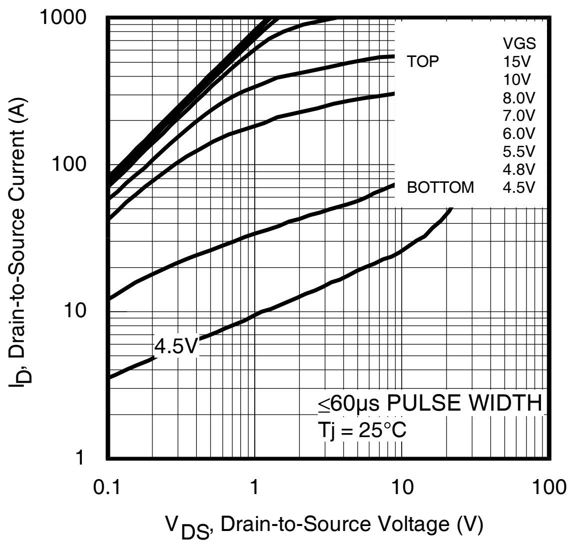


Fig 3. Typical Output Characteristics

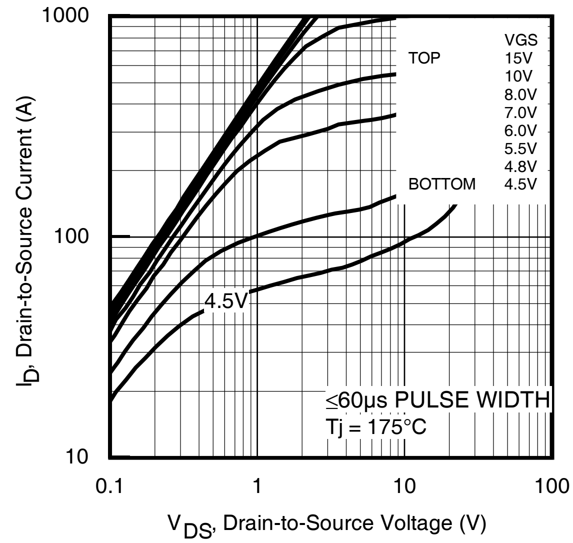


Fig 4. Typical Output Characteristics

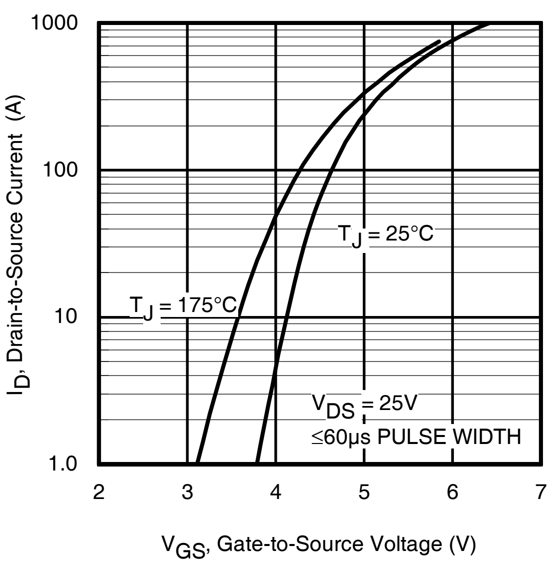


Fig 5. Typical Transfer Characteristics

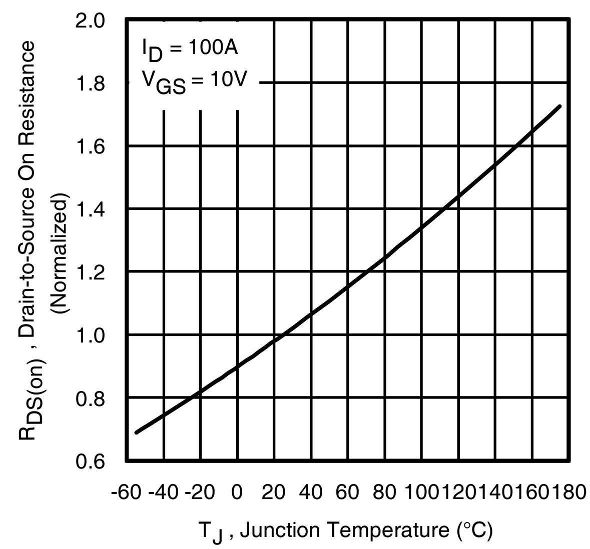


Fig 6. Normalized On-Resistance vs. Temperature

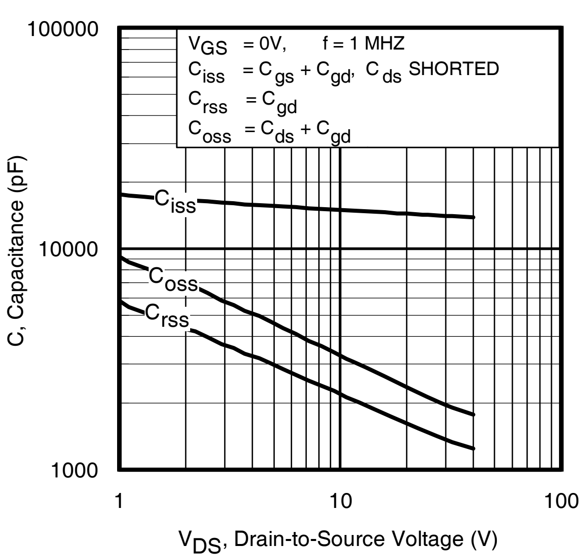


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

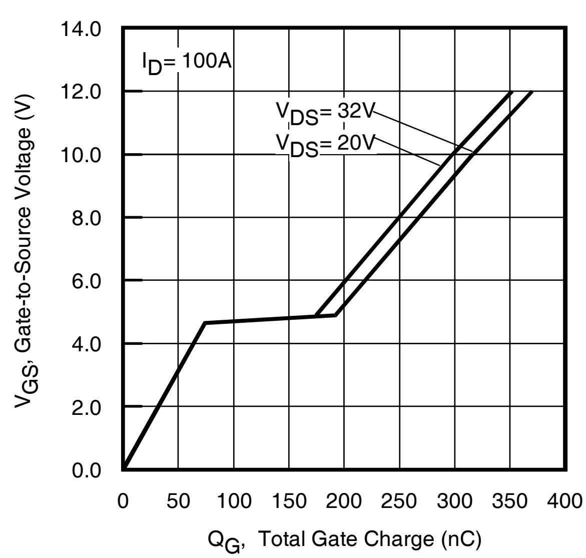


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

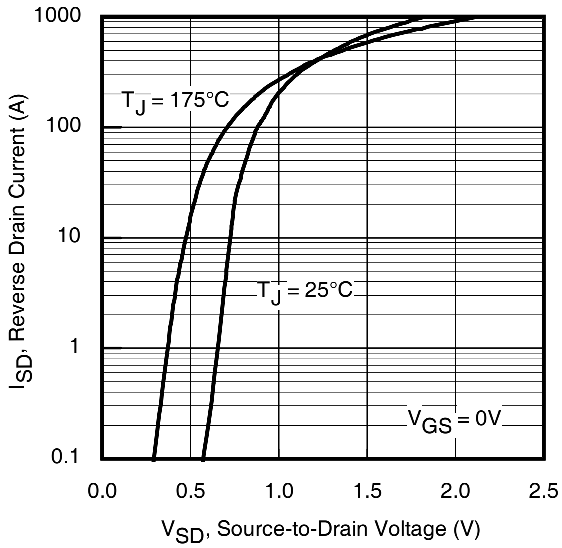


Fig 9. Typical Source-Drain Diode Forward Voltage

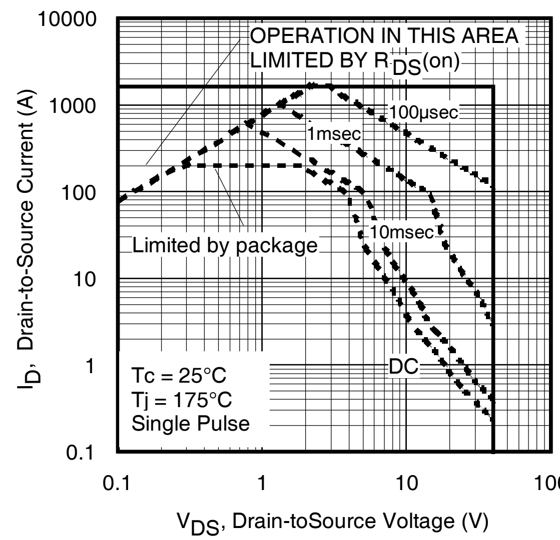


Fig 10. Maximum Safe Operating Area

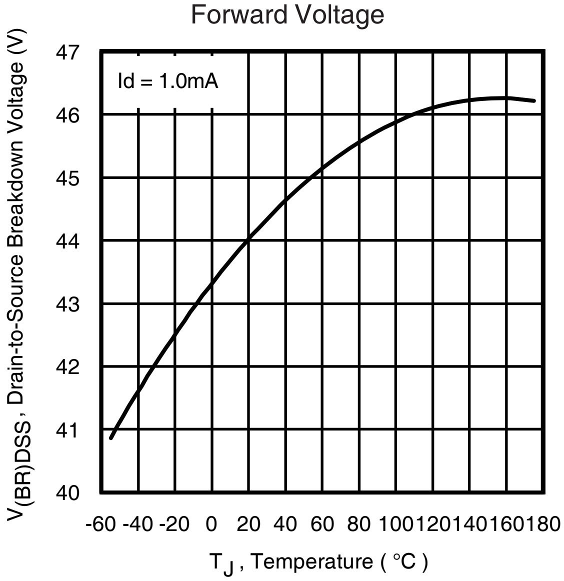


Fig 11. Drain-to-Source Breakdown Voltage

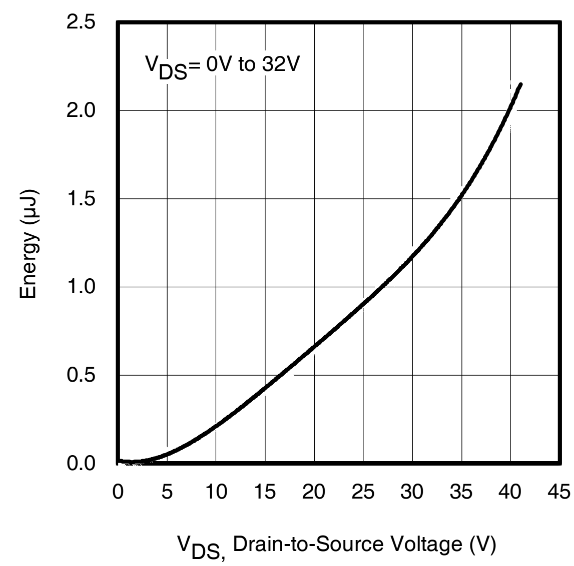


Fig 12. Typical C_{OSS} Stored Energy

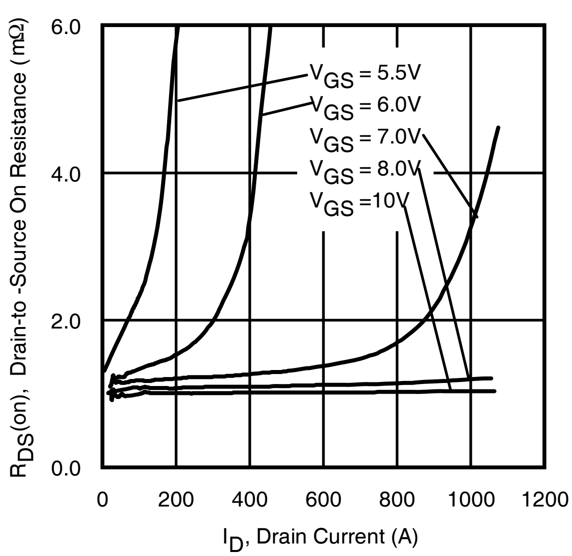


Fig 13. Typical On-Resistance vs. Drain Current

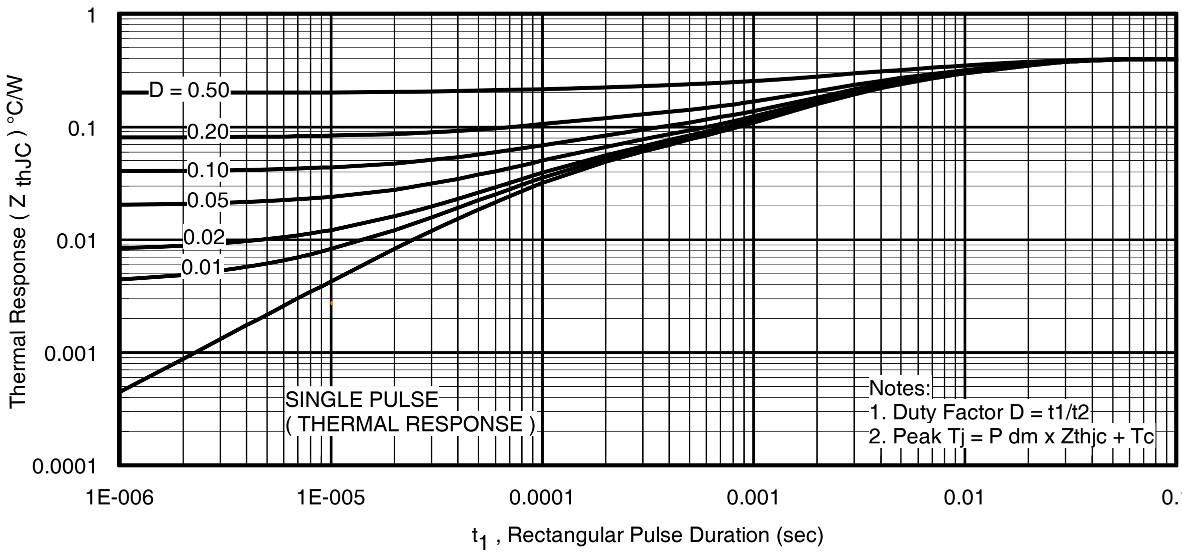


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

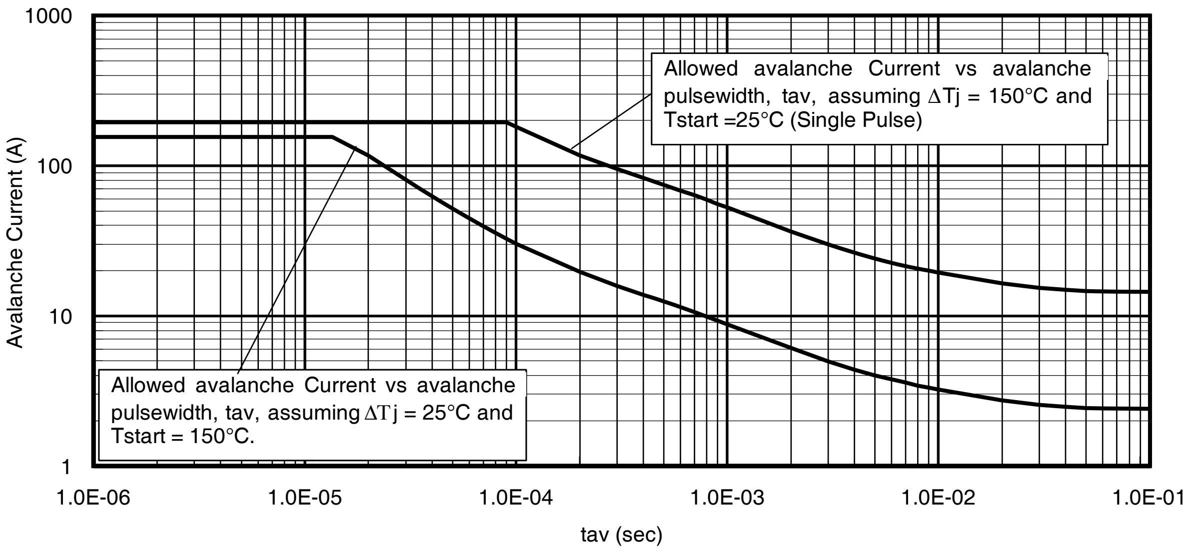


Fig 15. Typical Avalanche Current vs.Pulsewidth

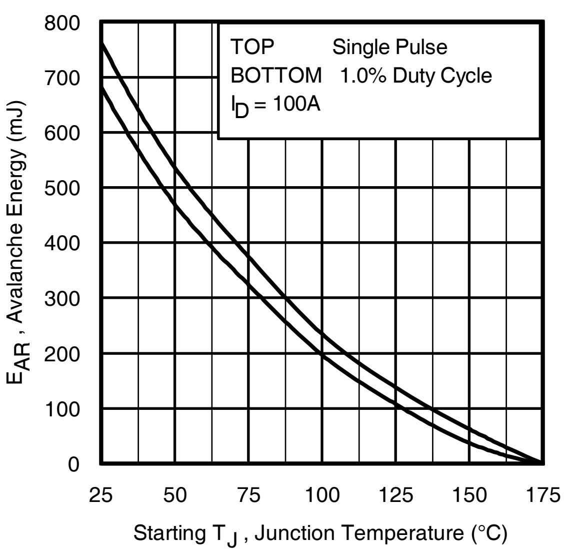


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

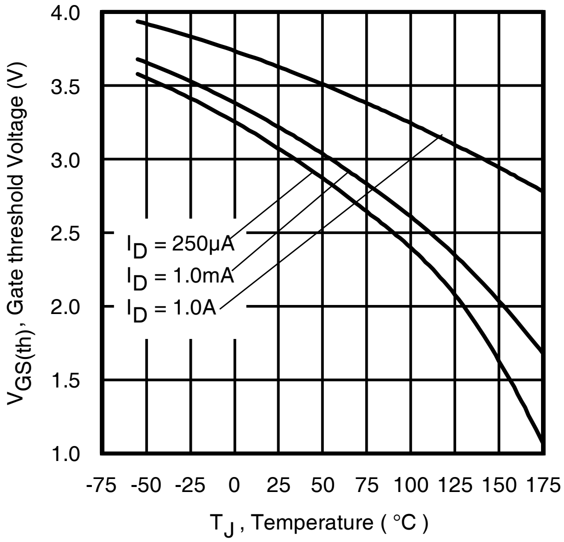


Fig 17. Threshold Voltage vs. Temperature

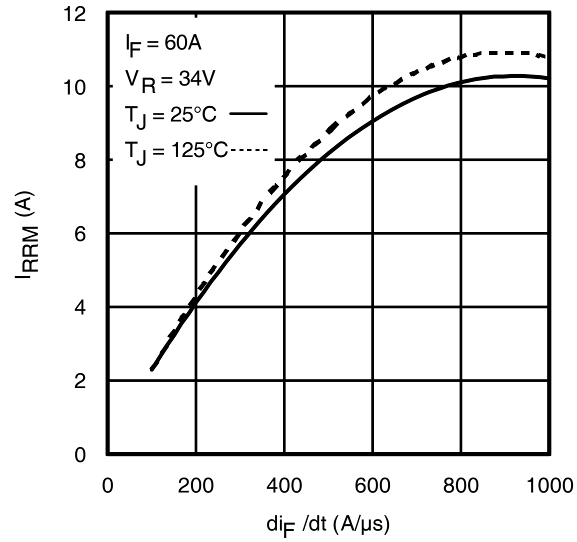


Fig. 18 - Typical Recovery Current vs. di_f/dt

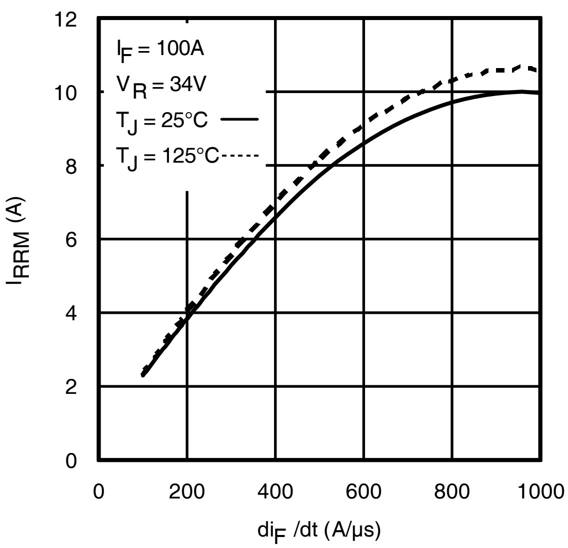


Fig. 19 - Typical Recovery Current vs. di_f/dt

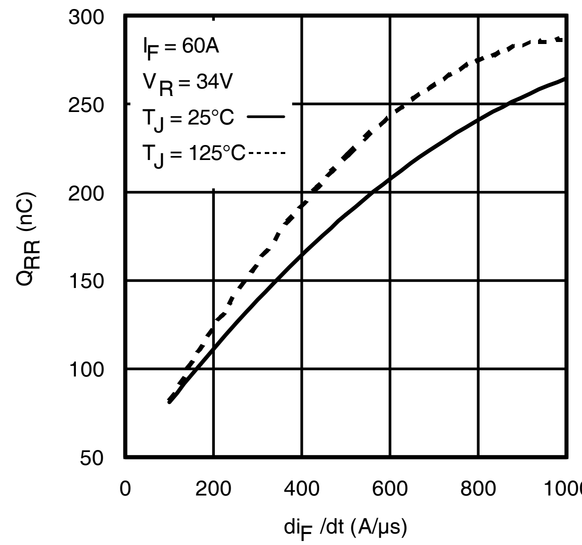


Fig. 20 - Typical Stored Charge vs. di_f/dt

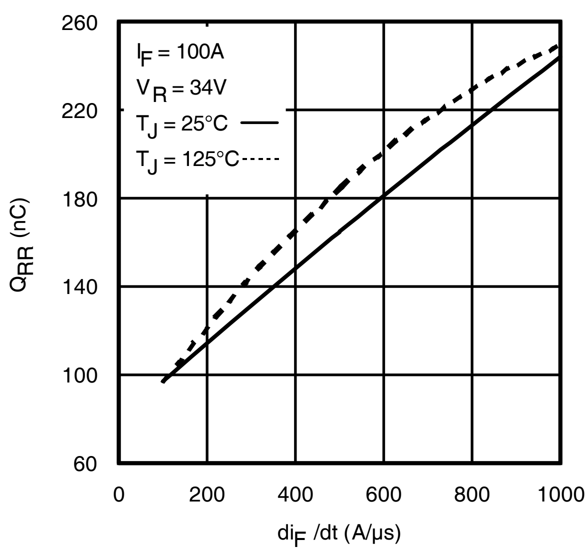
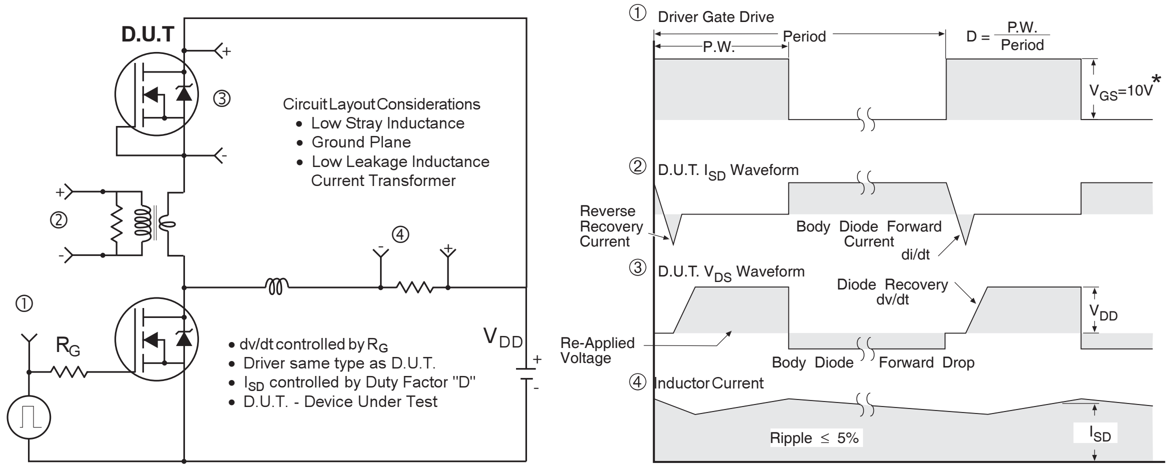


Fig. 21 - Typical Stored Charge vs. di_f/dt



* V_{GS} = 5V for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

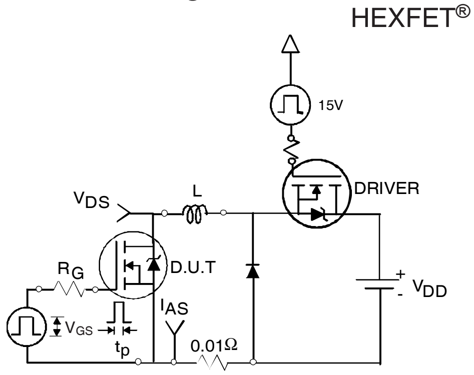


Fig 22a. Unclamped Inductive Test Circuit

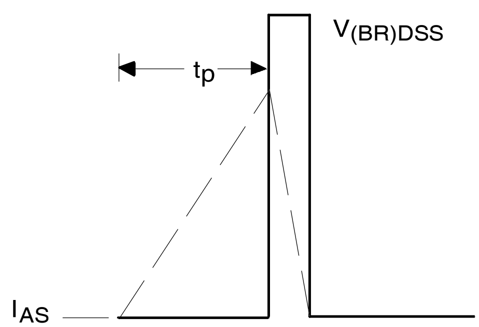


Fig 22b. Unclamped Inductive Waveforms

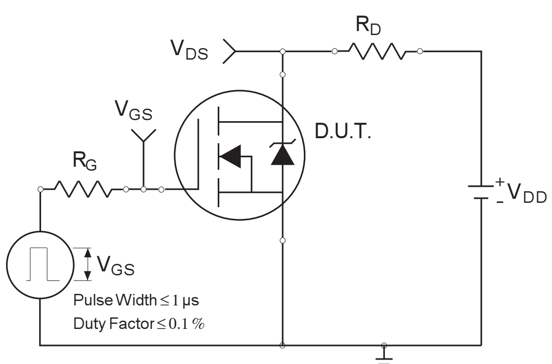


Fig 23a. Switching Time Test Circuit

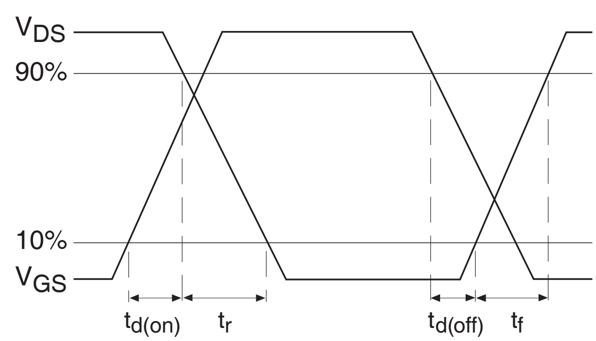


Fig 23b. Switching Time Waveforms

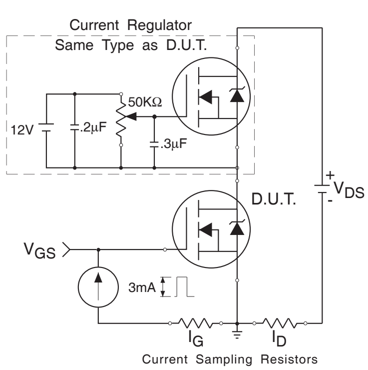


Fig 24a. Gate Charge Test Circuit

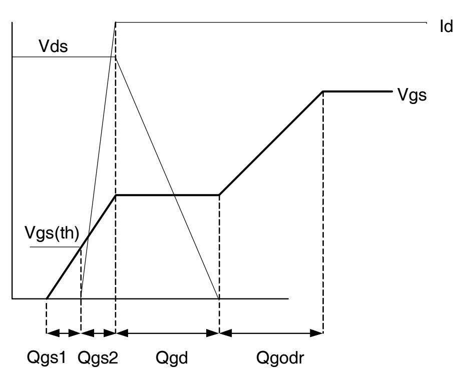
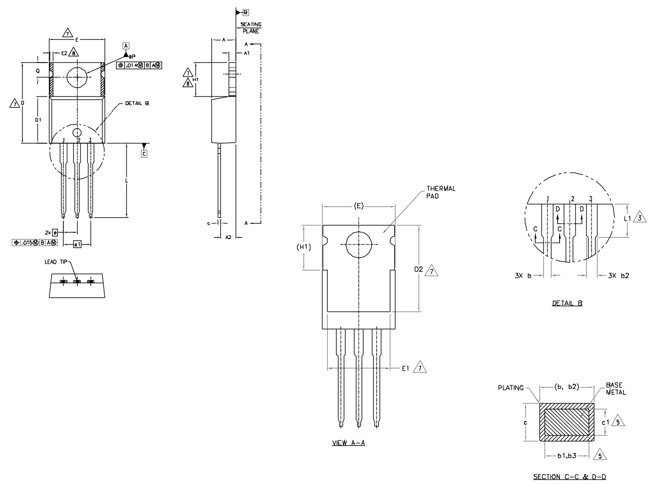


Fig 24b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.- CONTROLLING DIMENSION : INCHES.
7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

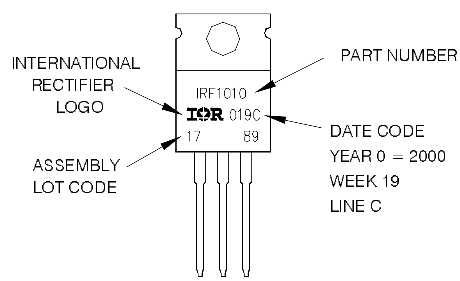
DIODES

1.- ANODE
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification information†

Qualification level	Industrial††	
	(per JEDEC JESD47F††† guidelines)	
	TO-220	Not applicable
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http:www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International
IOR Rectifier

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