

## IR2304(S) & (PbF)

### Features

- Floating channel designed for bootstrap operation to +600V. Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V, 5V, and 15V input logic input compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Internal 100ns dead-time
- Output in phase with input
- Available in Lead-Free

### Description

The IR2304(S) are a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

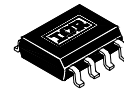
### HALF-BRIDGE DRIVER Product Summary

|                         |              |
|-------------------------|--------------|
| V <sub>OFFSET</sub>     | 600V max.    |
| I <sub>O+/-</sub> (min) | 60 mA/130 mA |
| V <sub>OUT</sub>        | 10 - 20V     |
| Delay Matching          | 50 ns        |
| Internal deadtime       | 100 ns       |
| ton/off (typ.)          | 220/220 ns   |

### Package



8-Lead PDIP

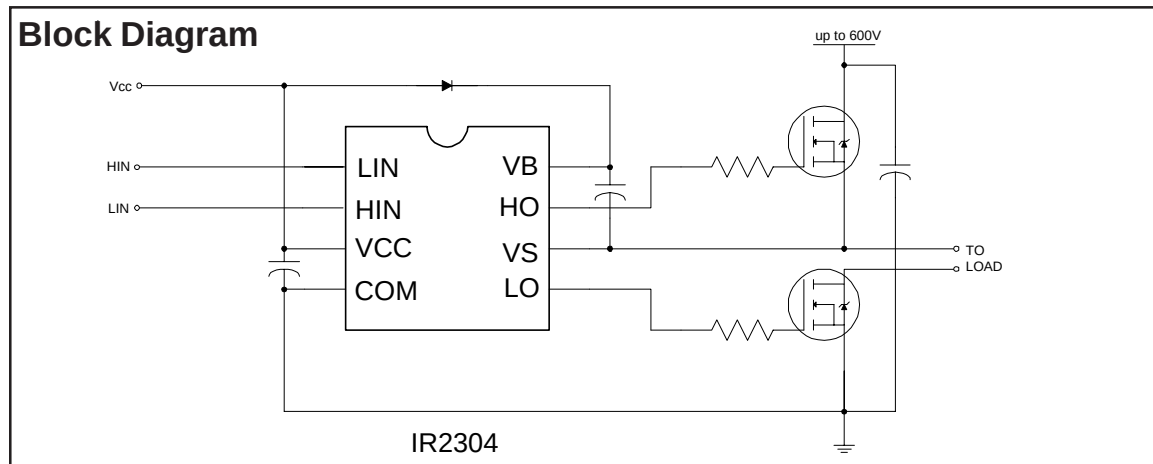


8 Lead SOIC

### 2106/2301/2108/2109/2302/2304 Feature Comparison

| Part      | Input logic | Cross-conduction prevention logic | Dead-Time             | Ground Pins |
|-----------|-------------|-----------------------------------|-----------------------|-------------|
| 2106/2301 | HIN/LIN     | no                                | none                  | COM         |
| 21064     |             |                                   |                       | VSS/COM     |
| 2108      | HIN/LIN     | yes                               | Internal 540ns        | COM         |
| 21084     |             |                                   | Programmable 0.54~5μs | VSS/COM     |
| 2109/2302 | IN/SD       | yes                               | Internal 540ns        | COM         |
| 21094     |             |                                   | Programmable 0.54~5μs | VSS/COM     |
| 2304      | HIN/LIN     | yes                               | Internal 100ns        | COM         |

### Block Diagram



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol              | Definition                                         | Min.                 | Max.                  | Units |      |
|---------------------|----------------------------------------------------|----------------------|-----------------------|-------|------|
| V <sub>S</sub>      | High side offset voltage                           | V <sub>B</sub> - 25  | V <sub>B</sub> + 0.3  | V     |      |
| V <sub>B</sub>      | High side floating supply voltage                  | -0.3                 | 625                   |       |      |
| V <sub>HO</sub>     | High side floating output voltage HO               | V <sub>S</sub> - 0.3 | V <sub>B</sub> + 0.3  |       |      |
| V <sub>CC</sub>     | Low side and logic fixed supply voltage            | -0.3                 | 25                    |       |      |
| V <sub>LO</sub>     | Low side output voltage LO                         | -0.3                 | V <sub>CC</sub> + 0.3 |       |      |
| V <sub>IN</sub>     | Logic input voltage (HIN, LIN)                     | -0.3                 | V <sub>CC</sub> + 0.3 |       |      |
| Com                 | Logic ground                                       | V <sub>CC</sub> -25  | V <sub>CC</sub> + 0.3 |       |      |
| dV <sub>S</sub> /dt | Allowable offset voltage SLEW RATE                 | —                    | 50                    | V/ns  |      |
| P <sub>D</sub>      | Package power dissipation @ T <sub>A</sub> ≤ +25°C | 8-Lead SOIC          | —                     | 0.625 | W    |
|                     |                                                    | 8-Lead PDIP          | —                     | 1.0   |      |
| R <sub>thJA</sub>   | Thermal resistance, junction to ambient            | 8-Lead SOIC          | —                     | 200   | °C/W |
|                     |                                                    | 8-Lead PDIP          | —                     | 125   |      |
| T <sub>J</sub>      | Junction temperature                               | —                    | 150                   | °C    |      |
| T <sub>S</sub>      | Storage temperature                                | -50                  | 150                   |       |      |
| T <sub>L</sub>      | Lead temperature (soldering, 10 seconds)           | —                    | 300                   |       |      |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

| Symbol          | Definition                               | Min.                | Max.                | Units |
|-----------------|------------------------------------------|---------------------|---------------------|-------|
| V <sub>B</sub>  | High side floating supply voltage        | V <sub>S</sub> + 10 | V <sub>S</sub> + 20 | V     |
| V <sub>S</sub>  | High side floating supply offset voltage | Note 1              | 600                 |       |
| V <sub>HO</sub> | High side (HO) output voltage            | V <sub>S</sub>      | V <sub>B</sub>      |       |
| V <sub>LO</sub> | Low side (LO) output voltage             | COM                 | V <sub>CC</sub>     |       |
| V <sub>IN</sub> | Logic input voltage (HIN, LIN)           | COM                 | V <sub>CC</sub>     |       |
| V <sub>CC</sub> | Low side supply voltage                  | 10                  | 20                  |       |
| T <sub>A</sub>  | Ambient temperature                      | -40                 | 125                 | °C    |

**Note 1:** Logic operational for V<sub>S</sub> of COM -5 to COM +600V. Logic state held for V<sub>S</sub> of COM -5V to COM -V<sub>BS</sub>.

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_S$  is applicable to HO and LO.

| Symbol                     | Definition                                                         | Min. | Typ. | Max. | Units   | Test Conditions     |
|----------------------------|--------------------------------------------------------------------|------|------|------|---------|---------------------|
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8    | 8.9  | 9.8  | V       |                     |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4  | 8.2  | 9    |         |                     |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | $V_{CC}$ supply undervoltage lockout hysteresis                    | 0.3  | 0.7  | —    |         |                     |
| $I_{LK}$                   | Offset supply leakage current                                      | —    | —    | 50   | $\mu A$ | $V_B = V_S = 600V$  |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                                  | 20   | 60   | 150  |         | $V_{IN} = 0V$ or 5V |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                                  | 50   | 120  | 240  |         | $V_{IN} = 0V$ or 5V |
| $V_{IH}$                   | Logic "1" input voltage                                            | 2.3  | —    | —    | V       |                     |
| $V_{IL}$                   | Logic "0" input voltage                                            | —    | —    | 0.8  |         |                     |
| $V_{OH}$                   | High level output voltage, $V_{BIAS} - V_O$                        | —    | —    | 2.8  |         | $I_O = 20mA$        |
| $V_{OL}$                   | Low level output voltage, $V_O$                                    | —    | —    | 1.2  |         |                     |
| $I_{IN+}$                  | Logic "1" input bias current                                       | —    | 5    | 40   | $\mu A$ | $V_{IN} = 5V$       |
| $I_{IN-}$                  | Logic "0" input bias current                                       | —    | 1.0  | 2.0  |         | $V_{IN} = 0V$       |
| $I_{O+}$                   | Output high short circuit pulse current                            | 60   | —    | —    | mA      | $V_O = 0V$          |
| $I_{O-}$                   | Output low short circuit pulsed current                            | 130  | —    | —    |         | $PW \leq 10 \mu s$  |

## Dynamic Electrical Characteristics

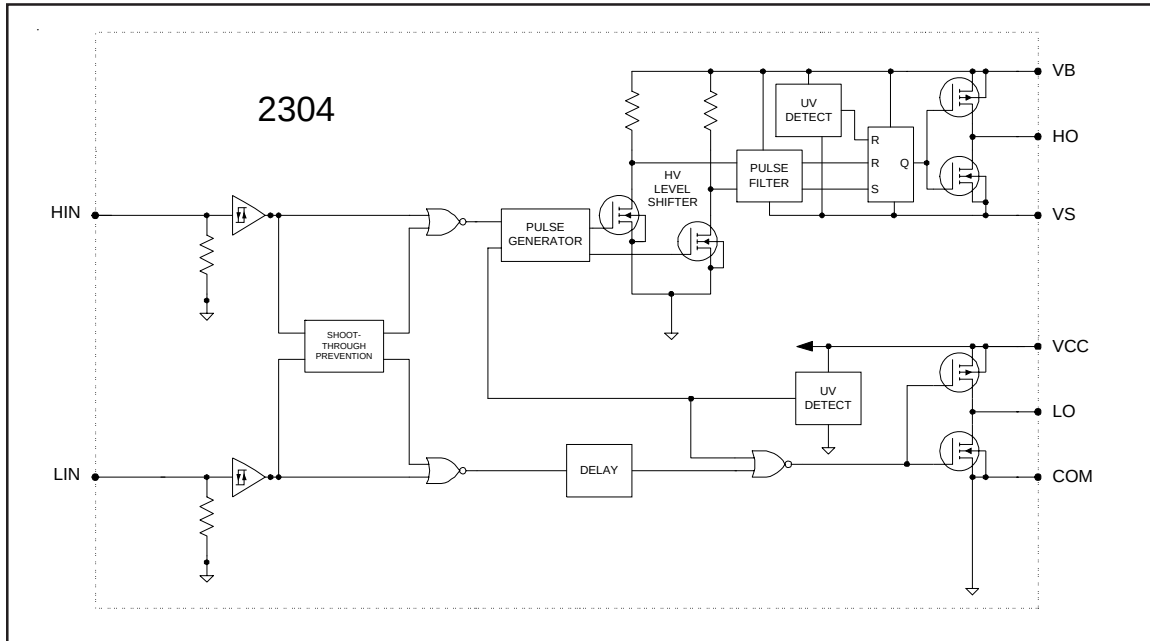
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $V_S$  = COM,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

| Symbol    | Definition                          | Min. | Typ. | Max. | Units | Test Conditions    |
|-----------|-------------------------------------|------|------|------|-------|--------------------|
| $t_{on}$  | Turn-on propagation delay           | 120  | 220  | 320  | ns    | $V_S = 0V$         |
| $t_{off}$ | Turn-off propagation delay          | 130  | 220  | 330  |       | $V_S = 0V$ or 600V |
| $t_r$     | Turn-on rise time                   | 60   | 200  | 300  |       |                    |
| $t_f$     | Turn-off fall time                  | 20   | 100  | 170  |       |                    |
| DT        | Dead time                           | 80   | 100  | 190  |       |                    |
| MT        | Delay matching, HS & LS turn-on/off | —    | —    | 50   |       |                    |

# IR2304(S)&(PbF)

International  
**IR** Rectifier

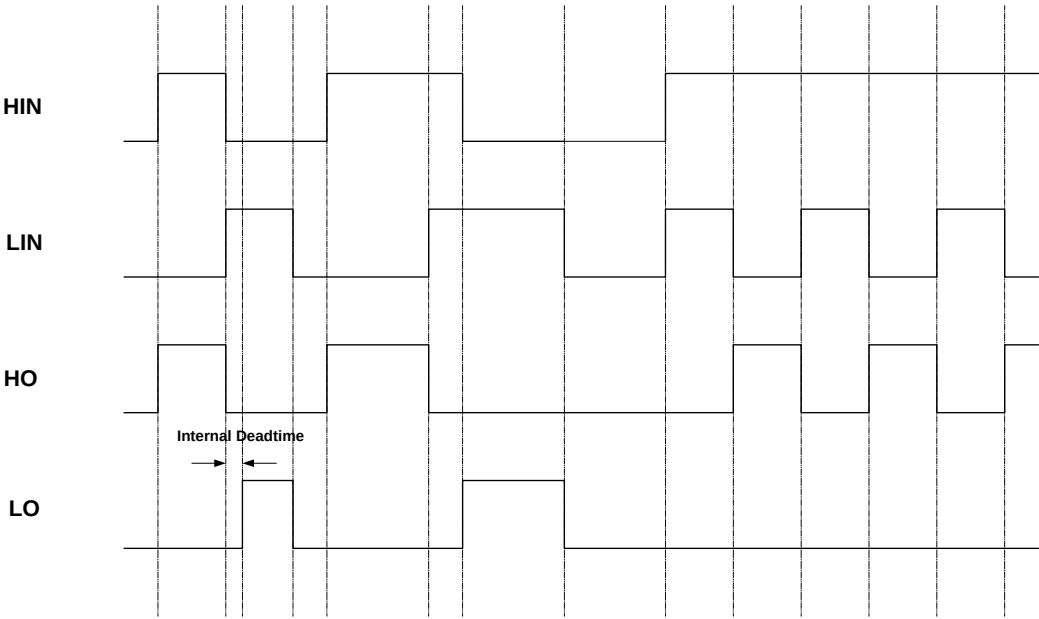
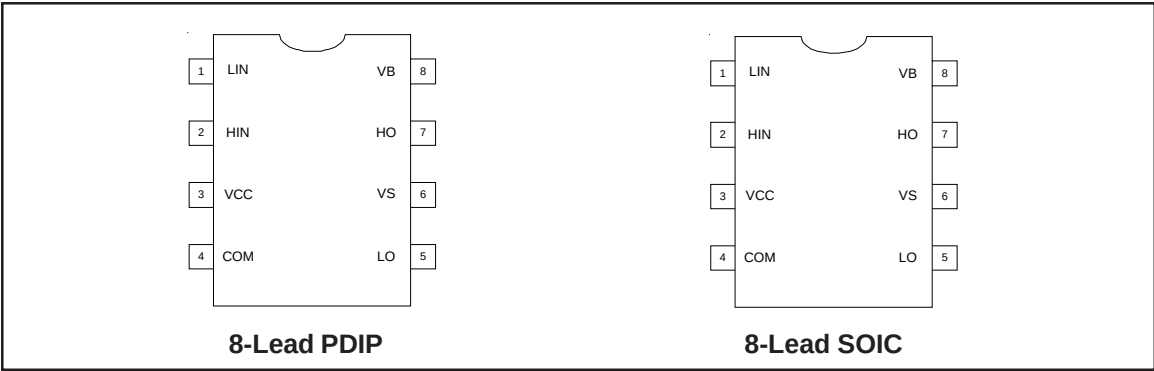
## Functional Block Diagram



## Lead Definitions

| Symbol | Description                                  |
|--------|----------------------------------------------|
| VCC    | Low side supply voltage                      |
| COM    | Logic ground and low side driver return      |
| HIN    | Logic input for high side gate driver output |
| LIN    | Logic input for low side gate driver output  |
| VB     | High side floating supply                    |
| HO     | High side driver output                      |
| VS     | High voltage floating supply return          |
| LO     | Low side driver output                       |

**Lead Assignments**



**Figure 1. Input/Output Functionality Diagram**

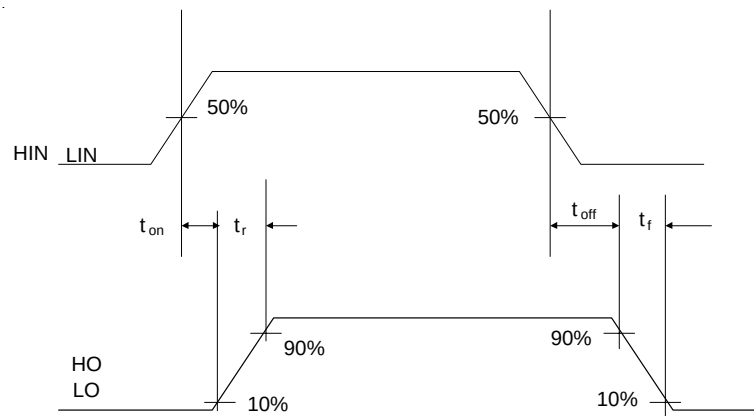


Figure 2. Switching Time Waveforms

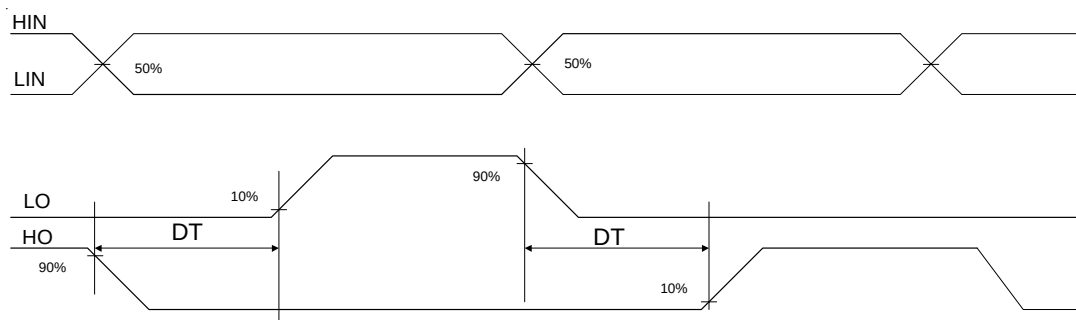
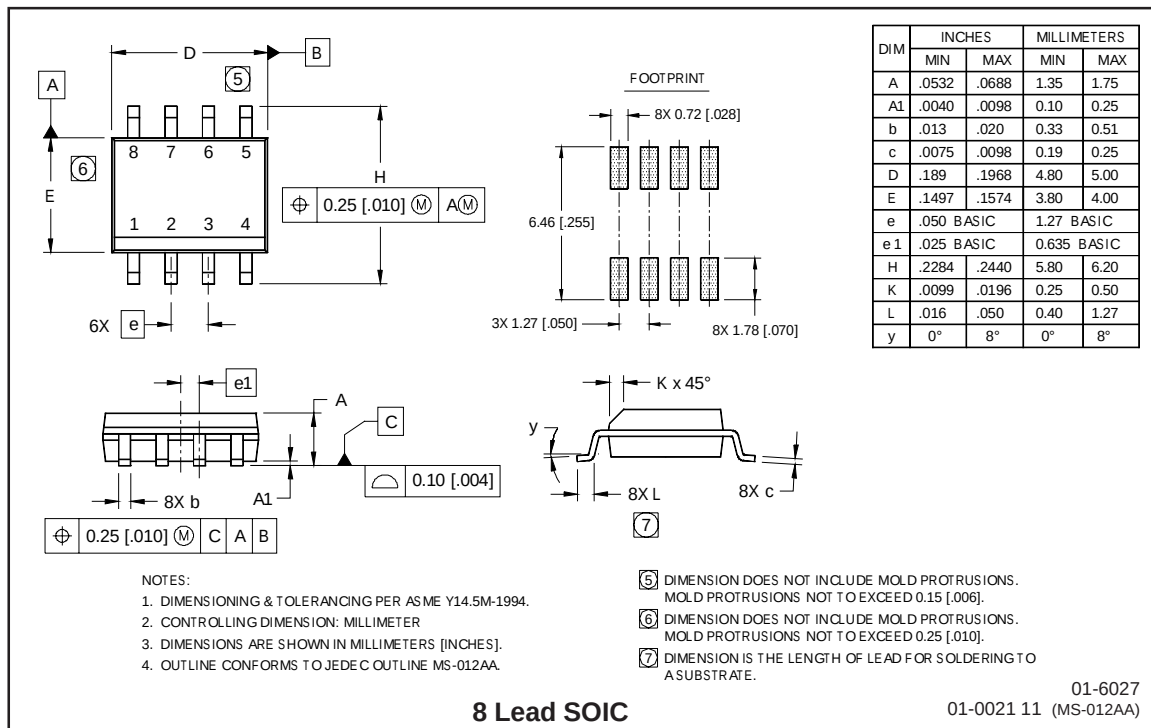
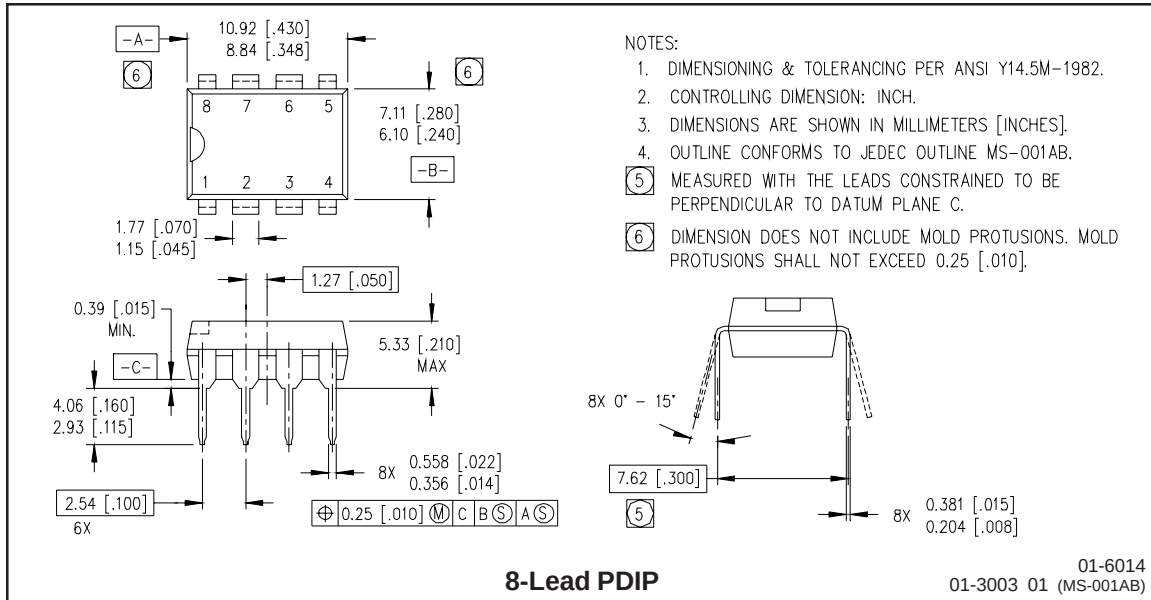


Figure 3. Internal Deadtime Timing

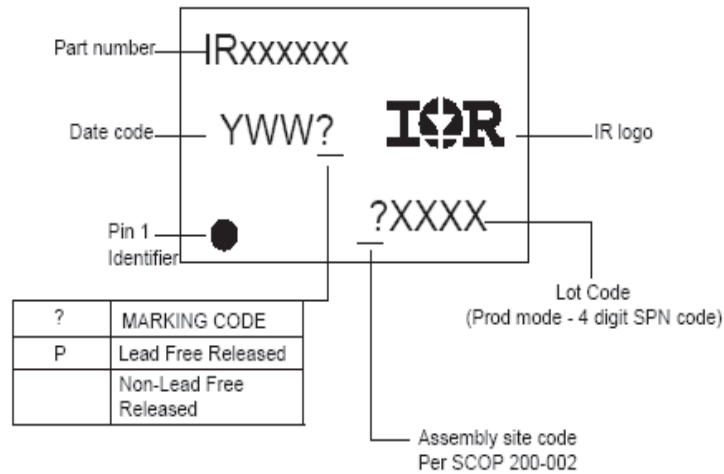
## Case outlines



# IR2304(S)&(PbF)

International  
**IR** Rectifier

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

8-Lead PDIP IR2304 order IR2304  
8-Lead SOIC IR2304S order IR2304S

### Lead-Free Part

8-Lead PDIP IR2304 order IR2304PbF  
8-Lead SOIC IR2304S order IR2304SPbF

International  
**IR** Rectifier

This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web Site.  
Data and specifications subject to change without notice.

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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