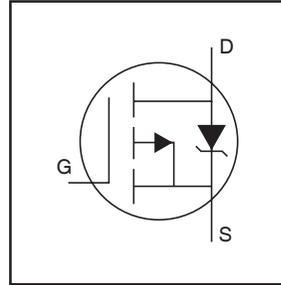


IRLML5103

Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- SOT-23 Footprint
- Low Profile (<1.1mm)
- Available in Tape and Reel
- Fast Switching
- Lead-Free
- Halogen-Free
- Marking: DK



$V_{DSS} = -30V$
$R_{DS(on)} = 0.60\Omega$

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-0.76	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-0.61	
I_{DM}	Pulsed Drain Current ①	-4.8	
$P_D @ T_A = 25^\circ C$	Power Dissipation	540	mW
	Linear Derating Factor	4.3	mW/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ③	—	230	°C/W

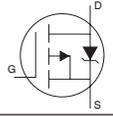
Electrical Characteristics @ $T_J = 25^\circ C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.029	—	V/°C	Reference to $25^\circ C, I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.60	Ω	$V_{GS} = -10V, I_D = -0.60A$ ③
		—	—	1.0		$V_{GS} = -4.5V, I_D = -0.30A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	0.44	—	—	S	$V_{DS} = -10V, I_D = -0.30A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	3.4	5.1	nC	$I_D = -0.60A$
Q_{gs}	Gate-to-Source Charge	—	0.52	0.78		$V_{DS} = -24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	1.1	1.7		$V_{GS} = -10V, \text{ See Fig. 6 and 9 } ③$
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = -15V$
t_r	Rise Time	—	8.2	—		$I_D = -0.60A$
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	16	—		$R_D = 25\Omega, \text{ See Fig. 10 } ③$
C_{iss}	Input Capacitance	—	75	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	37	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	18	—		$f = 1.0MHz, \text{ See Fig. 5}$

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Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.54	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-4.8		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}$, $I_S = -0.60\text{A}$, $V_{GS} = 0\text{V}$ ③
t_{rr}	Reverse Recovery Time	—	26	39	ns	$T_J = 25^\circ\text{C}$, $I_F = -0.60\text{A}$
Q_{rr}	Reverse Recovery Charge	—	20	30	nC	$di/dt = 100\text{A}/\mu\text{s}$ ③



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $I_{SD} \leq -0.60\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 5\text{sec}$.

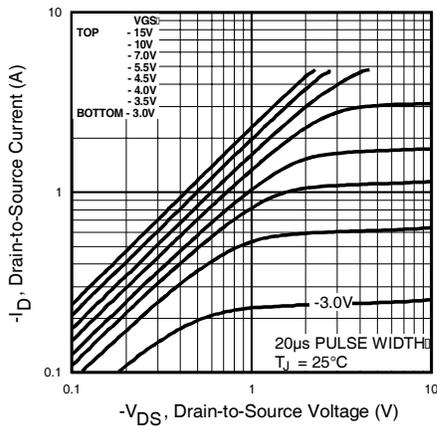


Fig 1. Typical Output Characteristics

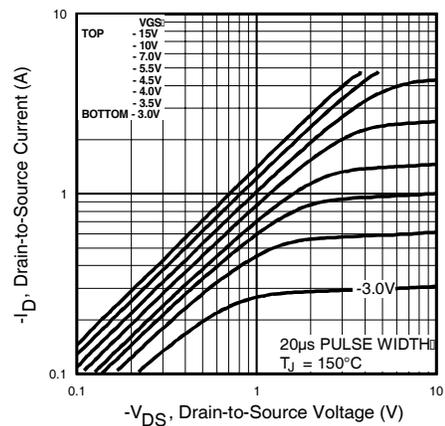


Fig 2. Typical Output Characteristics

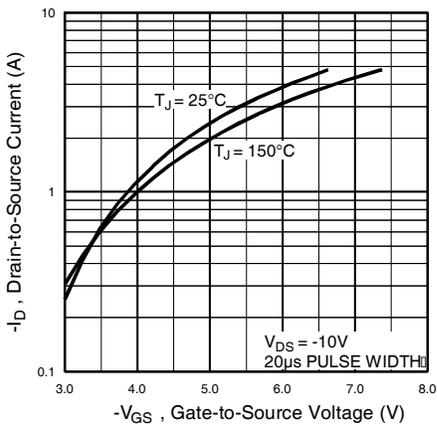


Fig 3. Typical Transfer Characteristics

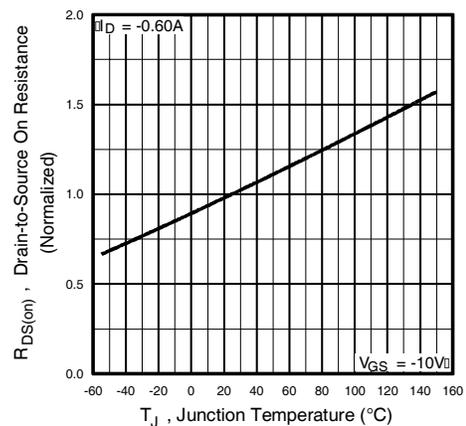


Fig 4. Normalized On-Resistance Vs. Temperature

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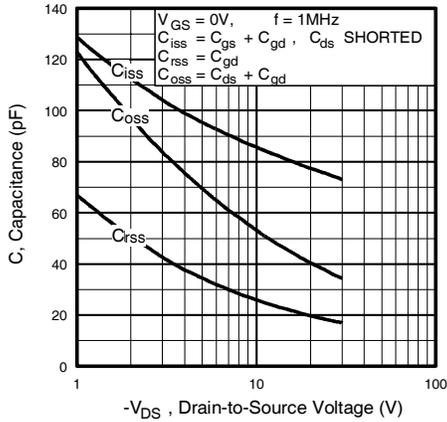


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

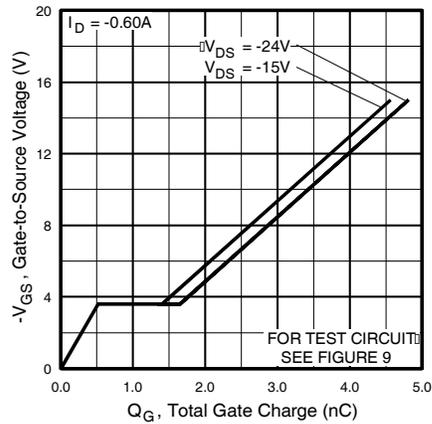


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

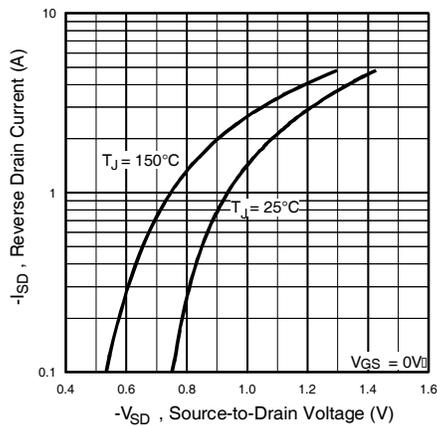


Fig 7. Typical Source-Drain Diode Forward Voltage

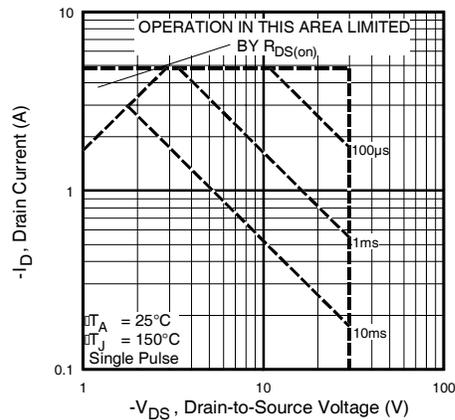


Fig 8. Maximum Safe Operating Area

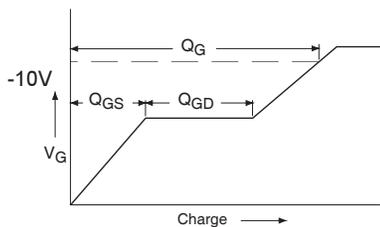


Fig 9a. Basic Gate Charge Waveform

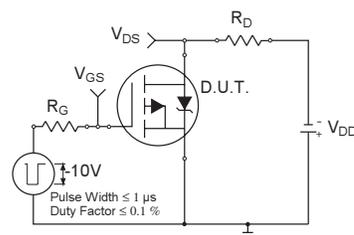


Fig 10a. Switching Time Test Circuit

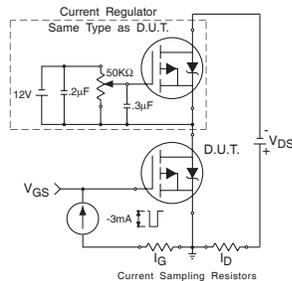


Fig 9b. Gate Charge Test Circuit

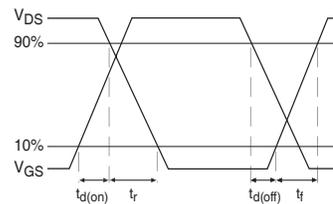


Fig 10b. Switching Time Waveforms

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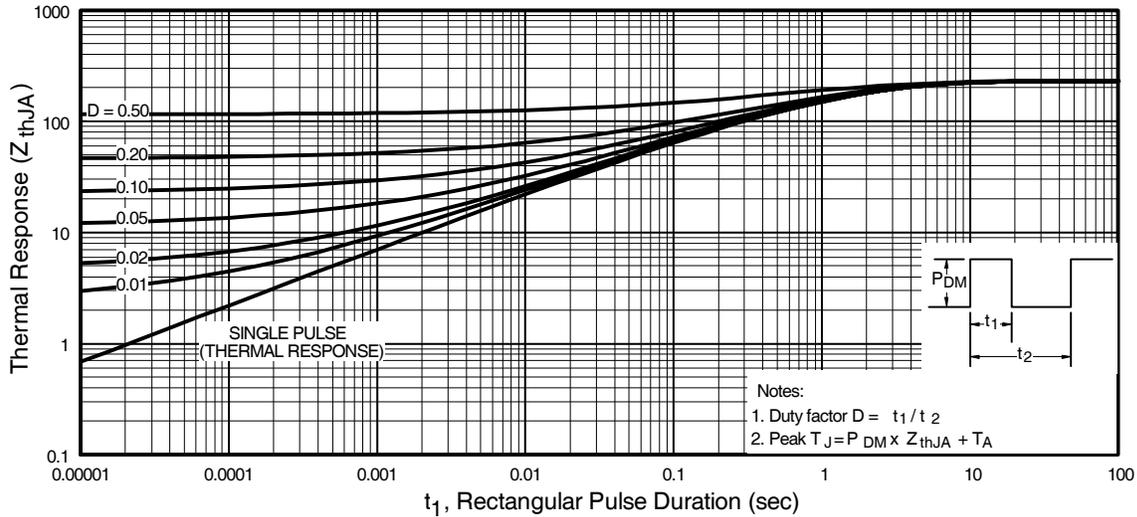
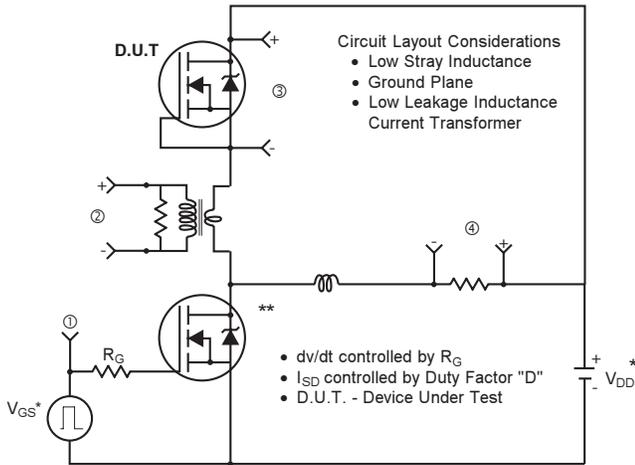
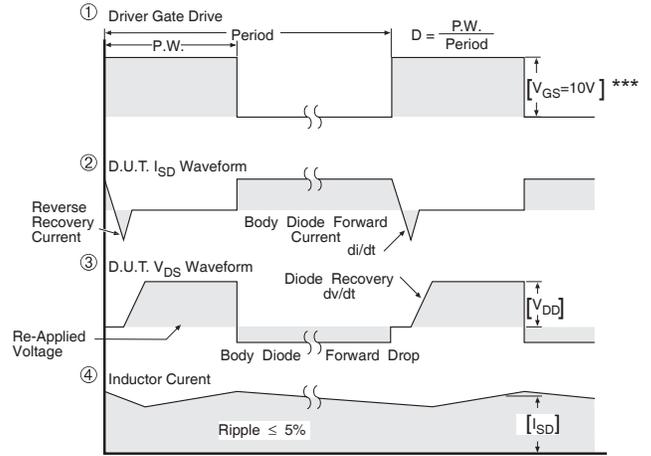


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 13. For P-Channel HEXFETS