



---

## PRODUCT SPECIFICATION

# Z86C21

## 8K ROM Z8<sup>®</sup> CMOS MICROCONTROLLER

---

### FEATURES

- 8-Bit CMOS MCU with 8 Kbytes of ROM
- 256 Byte Register File
  - 236 Bytes of General-Purpose RAM
  - 16 Bytes Control/Status Registers
  - 4 Bytes for Ports
- 40-Pin DIP, 44-Pin PLCC or 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low Power Consumption: 220 mW (max) @ 16 MHz
- Fast instruction pointer: 1.0  $\mu$ s @ 12 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds: 12 and 16 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

---

### GENERAL DESCRIPTION

The Z86C21 microcontroller is a member of the Z8 single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM. The device is packaged in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP with a ROMless pin option available on the 44-pin versions only. With the ROM/ROMless feature selectively, the Z86C21 offers both external memory and preprogrammed ROM, making it well-suited for high-volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C21 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications demanding powerful I/O capabilities, the Z86C21 provides 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory. There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

---

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C21 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART.

**Notes:**  
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V <sub>CC</sub> GND	V <sub>DD</sub> V <sub>SS</sub>

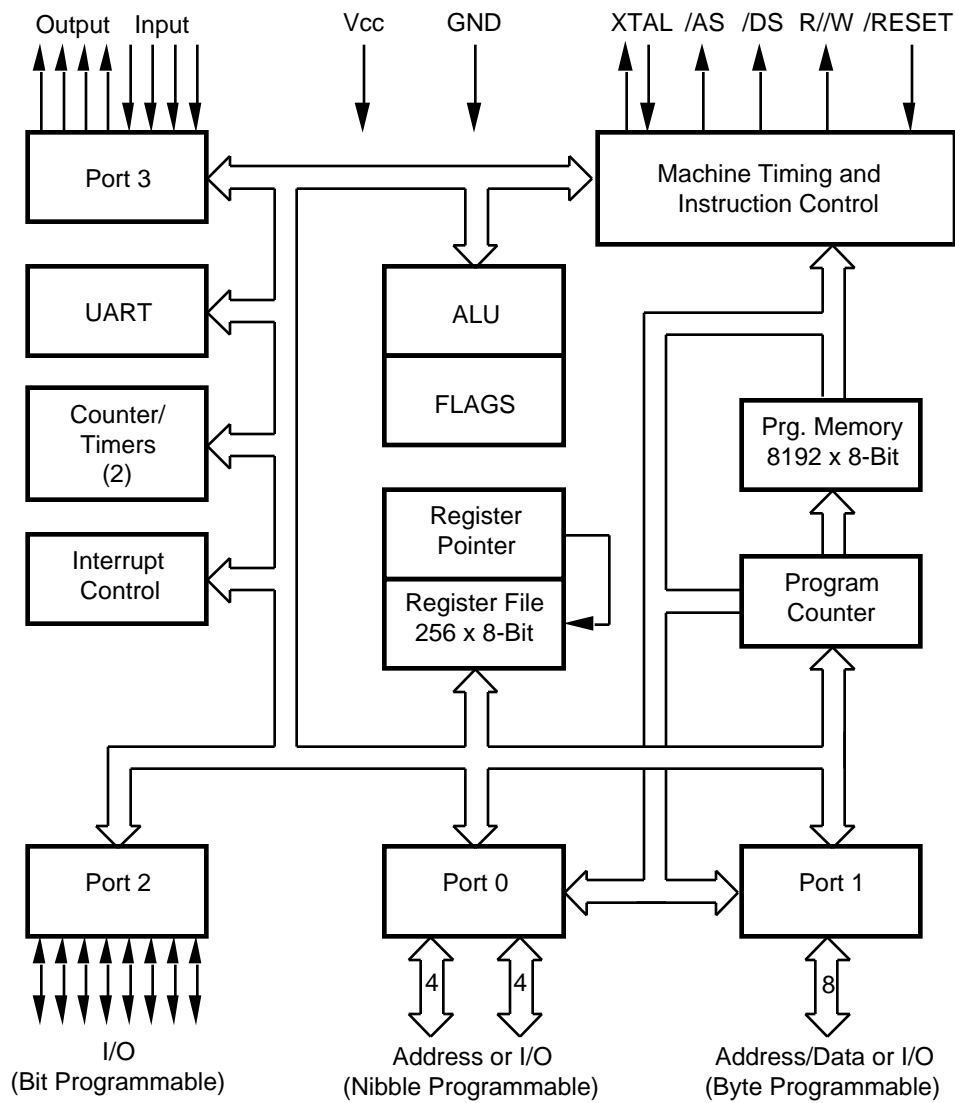


Figure 1. Z86C21 Functional Block Diagram

PIN DESCRIPTION

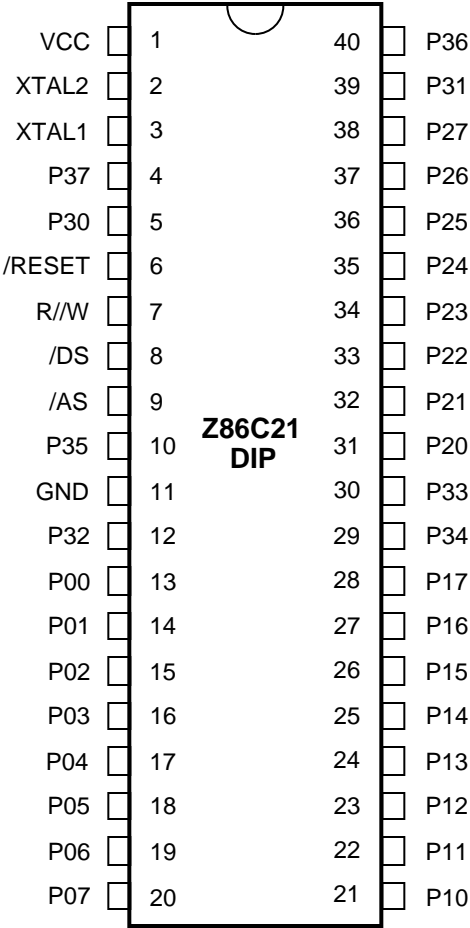


Figure 2. 40-Pin DIP Pin Assignments

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input	11	GND	Ground	Input
2	XTAL2	Crystal, Oscillator Clock	Output	12	P32	Port 3, Pin 2	Input
3	XTAL1	Crystal, Oscillator Clock	Input	13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
4	P37	Port 3, Pin 7	Output	21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
5	P30	Port 3, Pin 0	Input	29	P34	Port 3, Pin 4	Output
6	/RESET	Reset	Input	30	P33	Port 3, Pin 3	Input
7	R/W	Read/Write	Output	31-38	P20-P27	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
8	/DS	Data Strobe	Output	39	P31	Port 3, Pin 1	Input
9	/AS	Address Strobe	Output	40	P36	Port 3, Pin 6	Output
10	P35	Port 3, Pin 5	Output				

PIN DESCRIPTION (Continued)

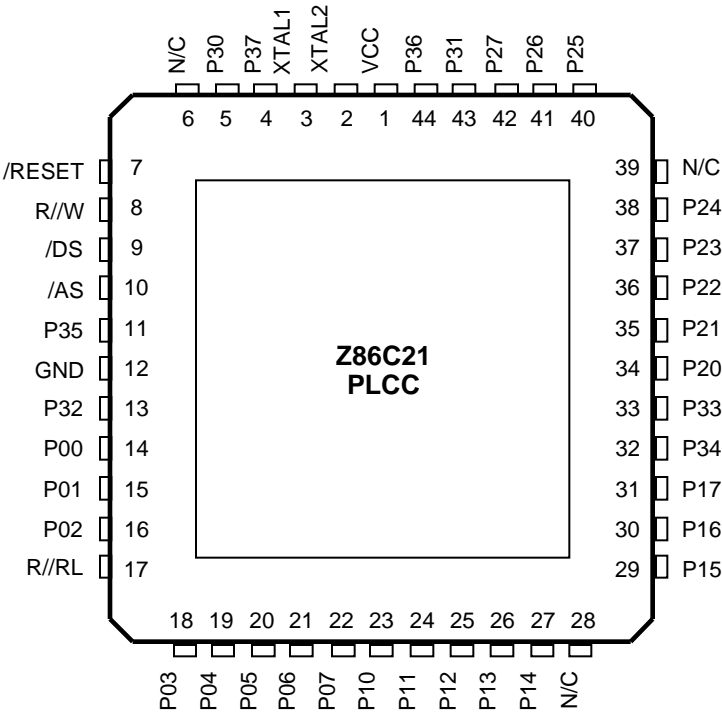
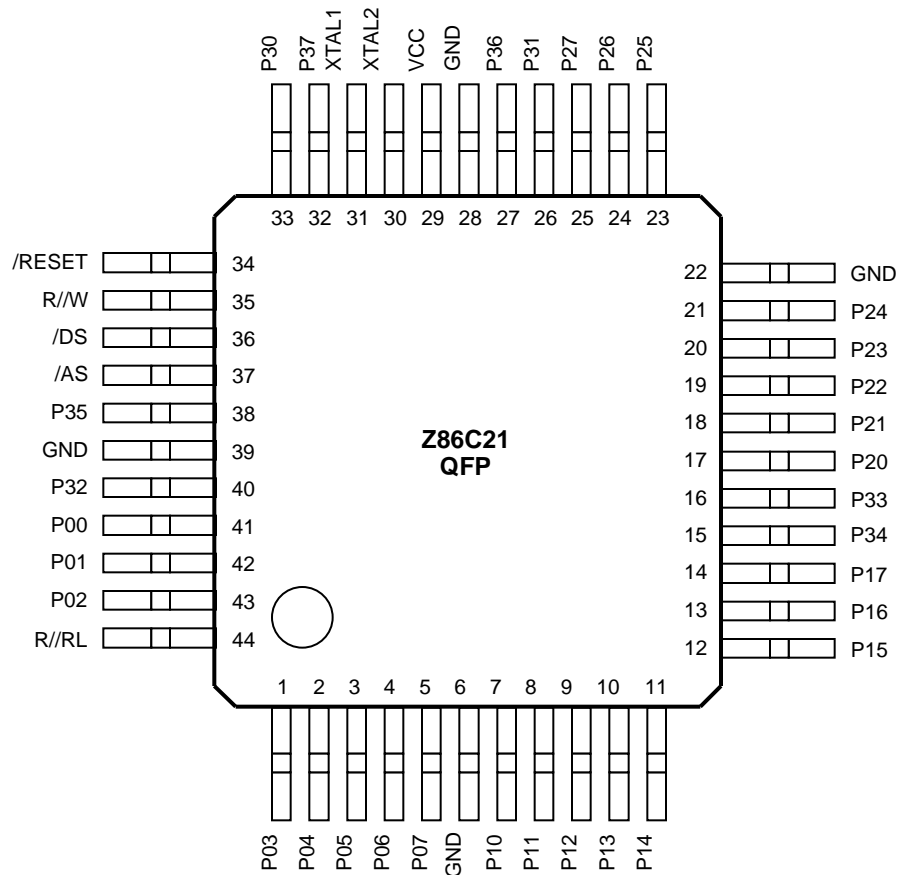


Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input	14-16	P00-P02	Port 0, Pins 0,1,2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output
4	P37	Port 3, Pin 7	Output	23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
5	P30	Port 3, Pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1, Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3, Pin 4	Output
8	R/W	Read/Write	Output	33	P33	Port 3, Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3, Pin 5	Output	40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
12	GND	Ground	Input	43	P31	Port 3, Pin 1	Input
13	P32	Port 3, Pin 2	Input	44	P36	Port 3, Pin 6	Output



**Figure 4. 44-Pin QFP Pin Assignments**

**Table 3. 44-Pin QFP Pin Identification**

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output	31	XTAL1	Crystal, Oscillator Clock	Input
6	GND	Ground	Input	32	P37	Port 3, Pin 7	Output
7-14	P10-P17	Port 1, Pins 0 through 7	In/Output	33	P30	Port 3, Pin 0	Input
15	P34	Port 3, Pin 4	Output	34	/RESET	Reset	Input
16	P33	Port 3, Pin 3	Input	35	R/W	Read/Write	Output
17-21	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output	36	/DS	Data Strobe	Output
22	GND	Ground	Input	37	/AS	Address Strobe	Output
23-25	P25-P27	Port 2, Pins 5,6,7	In/Output	38	P35	Port 3, Pin 5	Output
26	P31	Port 3, Pin 1	Input	39	GND	Ground	Input
27	P36	Port 3, Pin 6	Output	40	P32	Port 3, Pin 2	Input
28	GND	Ground	Input	41-43	P00-P02	Port 0, Pins 0,1,2	In/Output
29	V <sub>CC</sub>	Power Supply	Input	44	R//RL	ROM/ROMless control	Input
30	XTAL2	Crystal, Oscillator Clock	Output				

---

## PIN FUNCTIONS

**/ROMless** (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8. For more details on the ROMless version, refer to the Z86C91 product specification. (**Note:** When left unconnected or pulled high to  $V_{CC}$ , the part functions as a normal Z86C21 ROM version). This pin is only available on the 44-pin versions of the Z86C21.

**/DS** (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

**/AS** (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

**XTAL1, XTAL2** *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

**R/W** (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

**/RESET** (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C21 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

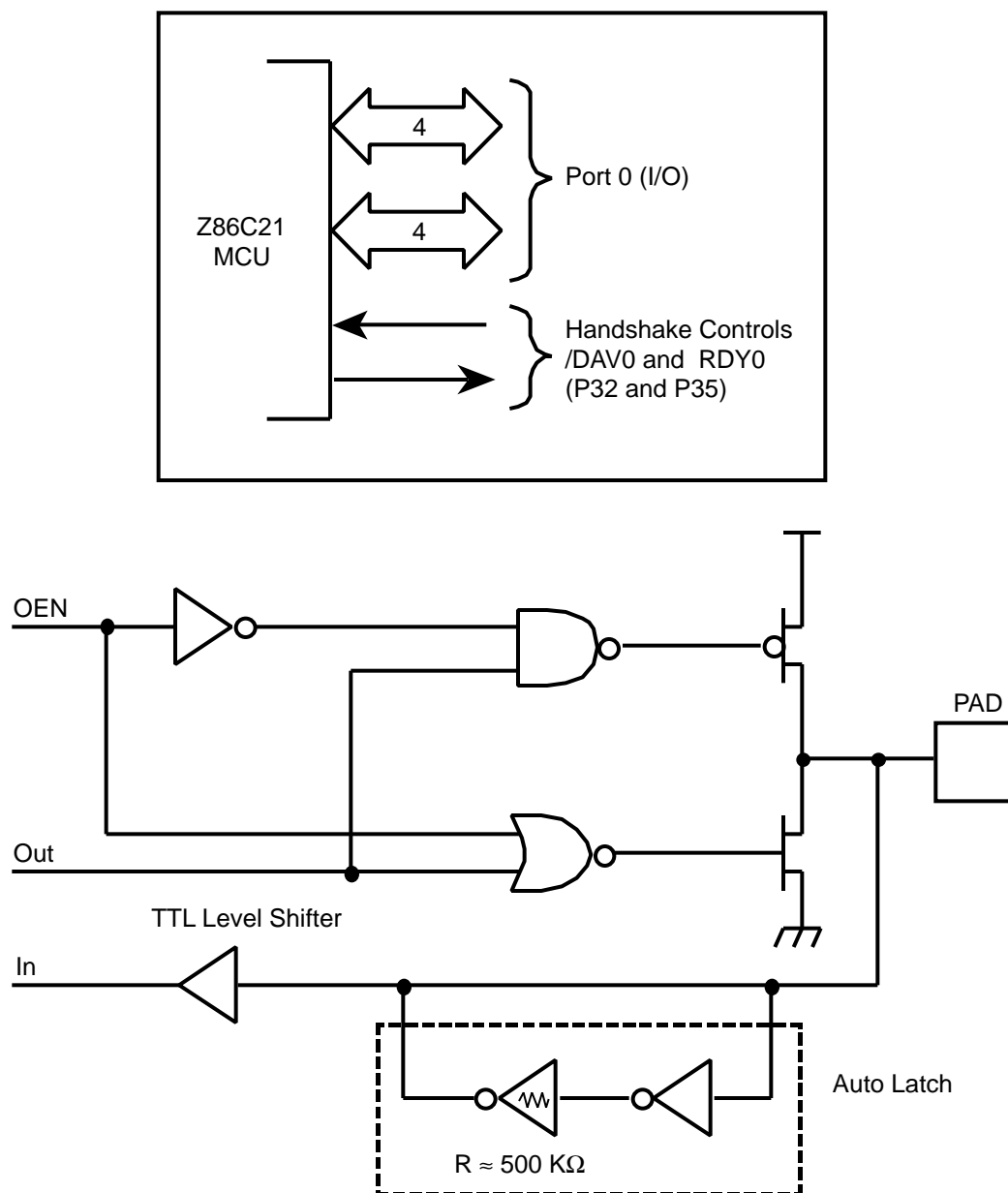
On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC2. When /RESET is deactivated, program execution begins at location 000C (HEX). Power-up reset time must be held Low for 50 ms, or until  $V_{CC}$  is stable, whichever is longer.

**Port 0** (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 5).

---



**Figure 5. Port 0 Configuration**

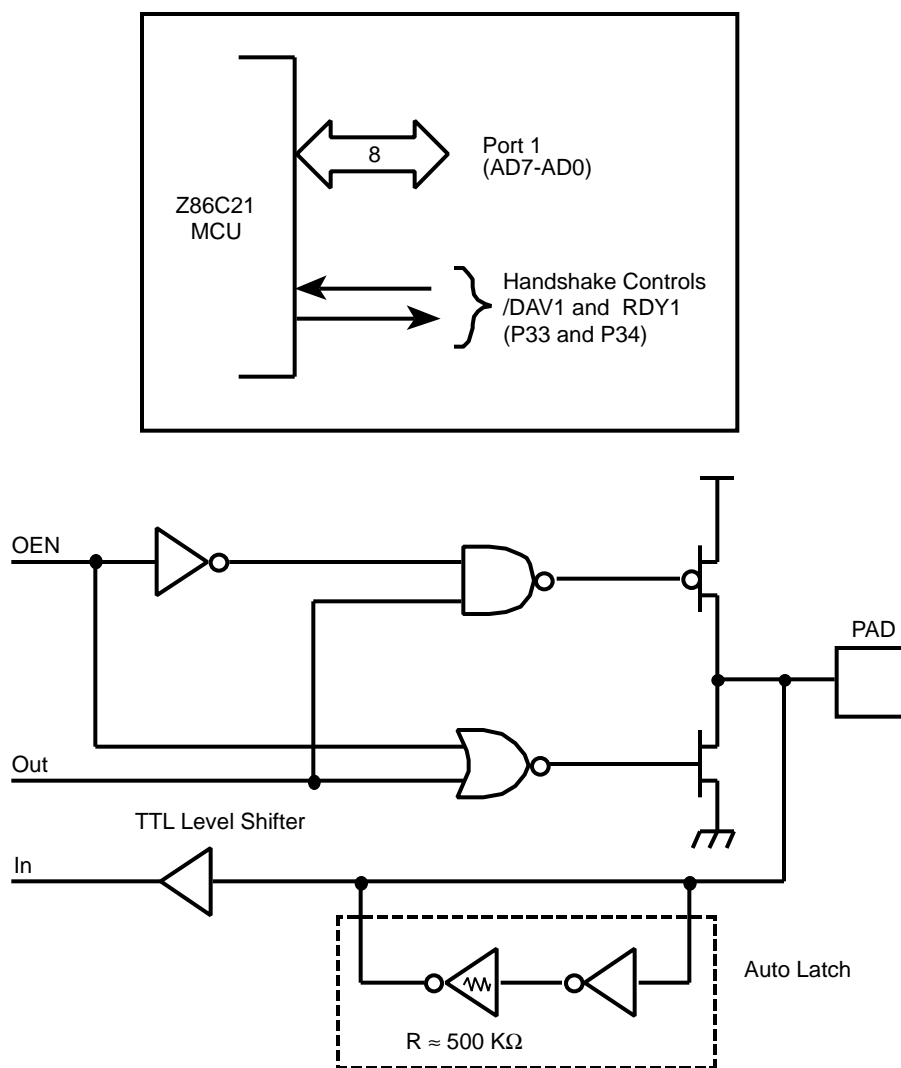
## PIN FUNCTIONS (Continued)

**Port 1** (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C21, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 8192 are referenced through Port 1. To interface external memory, Port 1 is programmed

for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in a high-impedance state along with Port 0, /AS, /DS and R/W, allowing the MCU to share common resource in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 6).

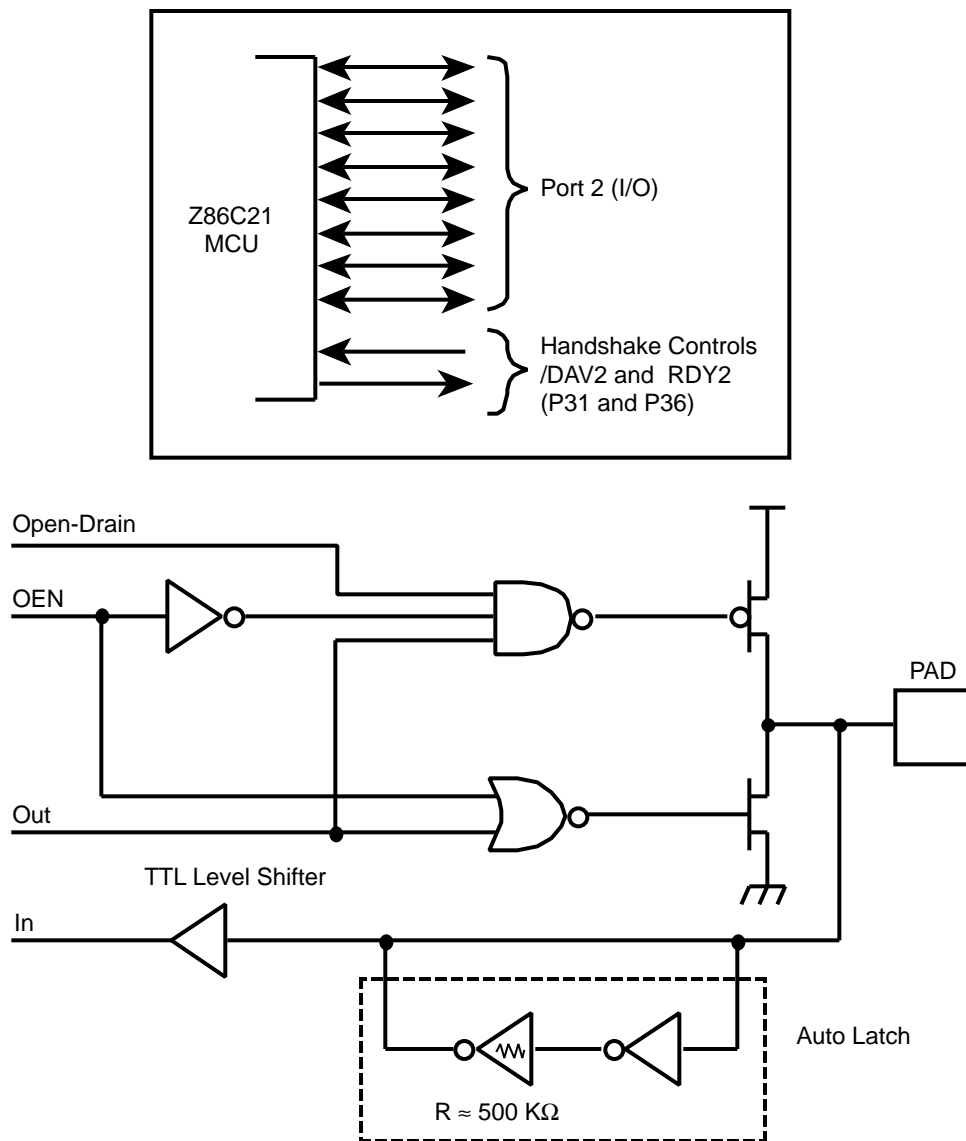


**Figure 6. Port 1 Configuration**



**Port 2** (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this

configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7).



**Figure 7. Port 2 Configuration**

## PIN FUNCTIONS (Continued)

**Port 3** (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed-input and four-fixed-output port. These eight I/O lines have four-fixed input (P33-P30) and four fixed output (P37-P34) ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 8 and Table 4) Port 3 pins have Auto Latches only.

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ), and Data Memory Select (/DM).

**UART Operation.** Port 3 lines P30 and P37, are be programmed as serial I/O lines for full-duplex serial asynchro-

nous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C21 automatically adds a start bit and two stop bits to transmitted data (Figure 9). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

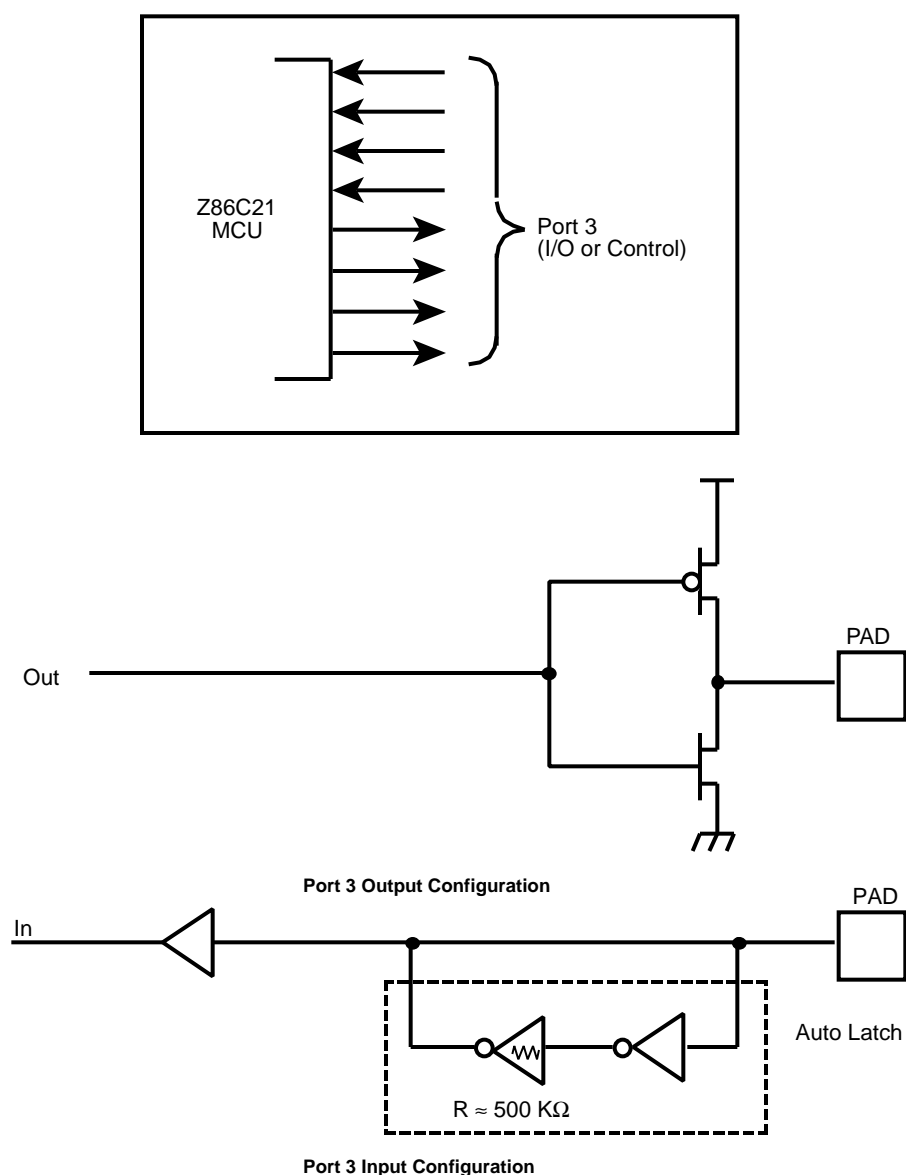


Figure 8. Port 3 Configuration

**Table 4. Port 3 Pin Assignments**

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN	$T_{IN}$	IRQ3	D/R	D/R	D/R	Serial In	
P31	IN		IRQ2					
P32	IN		IRQ0					
P33	IN		IRQ1					
P34	OUT	$T_{OUT}$		R/D	R/D	R/D		DM
P35	OUT							
P36	OUT							
P37	OUT							
T0			IRQ4				Serial Out	
T1			IRQ5					

**Notes:**

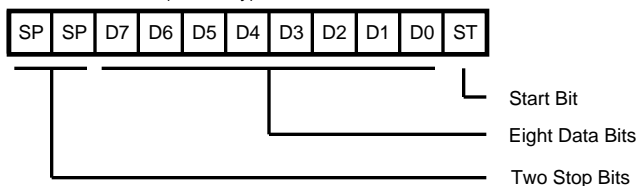
HS = Handshake Signals; D = Data Available; R = Ready

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not been driven by any source.

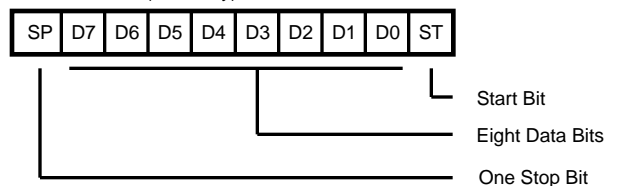
**Low EMI Option.** The Z86C21 is available in a Low EMI option. This option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms typical.
- Oscillator divide-by-two circuitry is eliminated.
- Internal SCLK/TCLK operation is limited to a maximum of 4 MHz (250 ns cycle time)

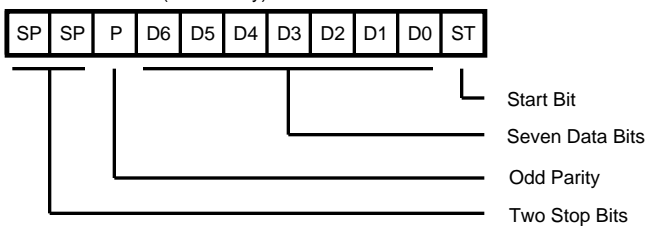
Transmitted Data (No Parity)



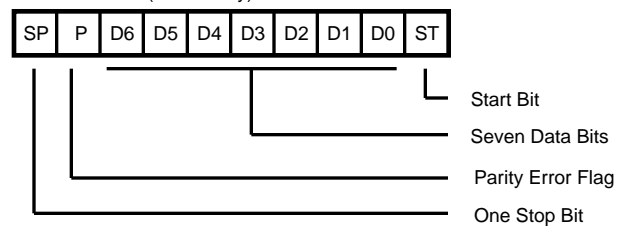
Received Data (No Parity)



Transmitted Data (With Parity)



Received Data (With Parity)



**Figure 9. Serial Data Formats**

FUNCTIONAL DESCRIPTION

Address Space

**Program Memory.** The Z86C21 can address up to 56K bytes of external program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 8191 consists of on-chip ROM. At addresses 8192 and greater, the Z86C21 executes external program memory fetches. In the ROMless mode, the Z86C21 can address up to 64K bytes of external program memory. Program execution begins at external location 000C (HEX) after a reset.

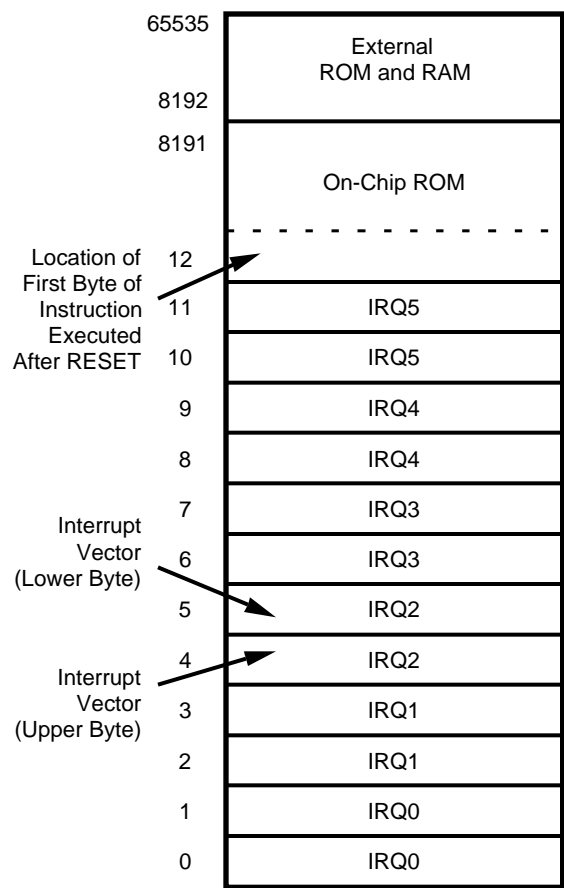


Figure 10. Program Memory Configuration

**Data Memory (/DM).** The ROM version can address up to 56K bytes of external data memory space beginning at location 8192. The ROMless version can address up to 64K bytes of external data memory. External data memory can be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34, is used to distinguish between data and program memory space (Figure 11). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

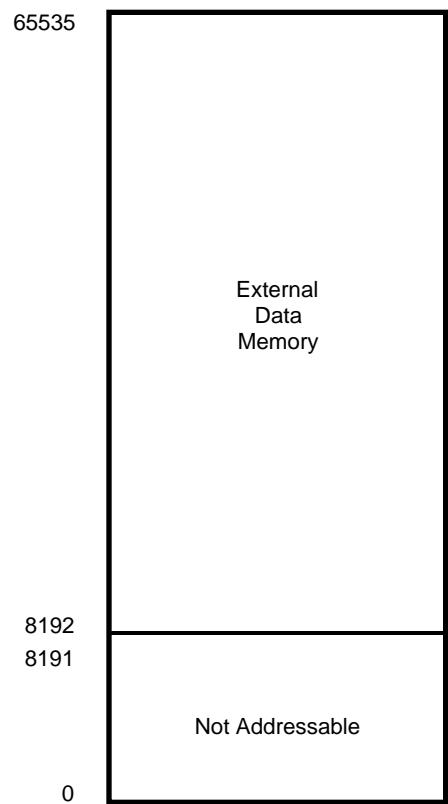


Figure 11. Data Memory Configuration

register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group. For the reset and power-up conditions of the Register File, see Figure 14.

LOCATION		IDENTIFIERS	
R255	Stack Pointer (Bits 7-0)	SPL	
R254	Stack Pointer (Bits 15-8)	SPH	
R253	Register Pointer	RP	
R252	Program Control Flags	FLAGS	
R251	Interrupt Mask Register	IMR	
R250	Interrupt Request Register	IRQ	
R249	Interrupt Priority Register	IPR	
R248	Ports 0-1 Mode	P01M	
R247	Port 3 Mode	P3M	
R246	Port 2 Mode	P2M	
R245	T0 Prescaler	PRE0	
R244	Timer/Counter0	T0	
R243	T1 Prescaler	PRE1	
R242	Timer/Counter1	T1	
R241	Timer Mode	TMR	
R240	Serial I/O	SIO	
R239	General-Purpose Registers		
R4			
R3		Port 3	P3
R2		Port 2	P2
R1		Port 1	P1
R0	Port 0	P0	

The diagram illustrates the Register File structure and its addressing. At the top, the **R253 (Register Pointer)** is shown as a 16-bit register, divided into two 8-bit nibbles: **r7 r6 r5 r4** (upper nibble) and **r3 r2 r1 r0** (lower nibble). Below this, a text box states: "The upper nibble of the register file address provided by the register pointer specifies the active working-register group."

The main part of the diagram is the **Register File**, a vertical stack of registers. The address range **FF** to **F0** is indicated on the left, with a bracket on the right labeled **R15 to R0**. This top section contains several registers, with vertical ellipses indicating more registers in between. Below this, a dashed line separates the top section from the bottom section. The bottom section starts at address **2F** and includes registers for **20**, **1F**, **10**, and **0F**. A bracket on the right for the **1F** to **0F** range is labeled **R15 to R4**. The registers in this bottom section are labeled as follows:

- Specified Working Register Group**: Indicated by an arrow from the text "The lower nibble of the register file address provided by the instruction points to the specified register." This group corresponds to the upper nibble (r7-r4) of the Register Pointer.
- Register Group 1**: Corresponds to the lower nibble (r3-r0) of the Register Pointer.
- Register Group 0**: Corresponds to the lower nibble (r3-r0) of the Register Pointer.
- I/O Ports**: Indicated by a dashed line at the bottom of the register stack.

On the left side of the Register File, a series of horizontal arrows point to the registers, indicating the active register group for each address range. The address **00** is shown at the bottom left, with a bracket on the right labeled **R3 to R0**.

### Figure 13. Register Pointer

## FUNCTIONAL DESCRIPTION (Continued)



**Figure 14. RAM Register File Reset Condition**

**RAM Protect.** The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

**ROM Protect.** The first 8 Kbytes of program memory is mask programmable. A ROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

**Note:** With RAM/ROM protect on, the Z86C21 cannot access the memory space.

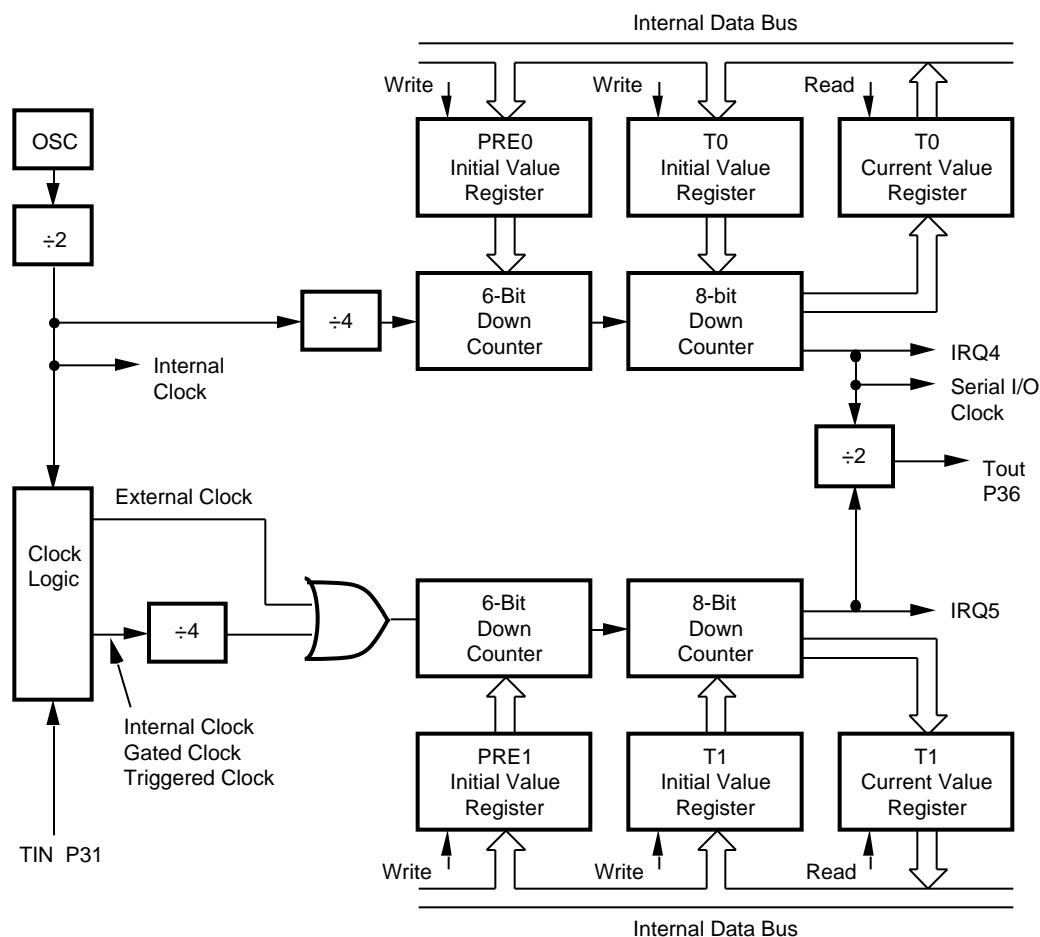
**Stack.** The Z86C21 has a 16-bit Stack Pointer (R254-R255) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 8192 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH-Bit 8-15) is used as a general-purpose register when using internal stack only.

also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The 6-bit prescalers divides the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output ( $T_{OUT}$ ) through which T0, T1 or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.



### Figure 15. Counter/Timers Block Diagram

## FUNCTIONAL DESCRIPTION (Continued)

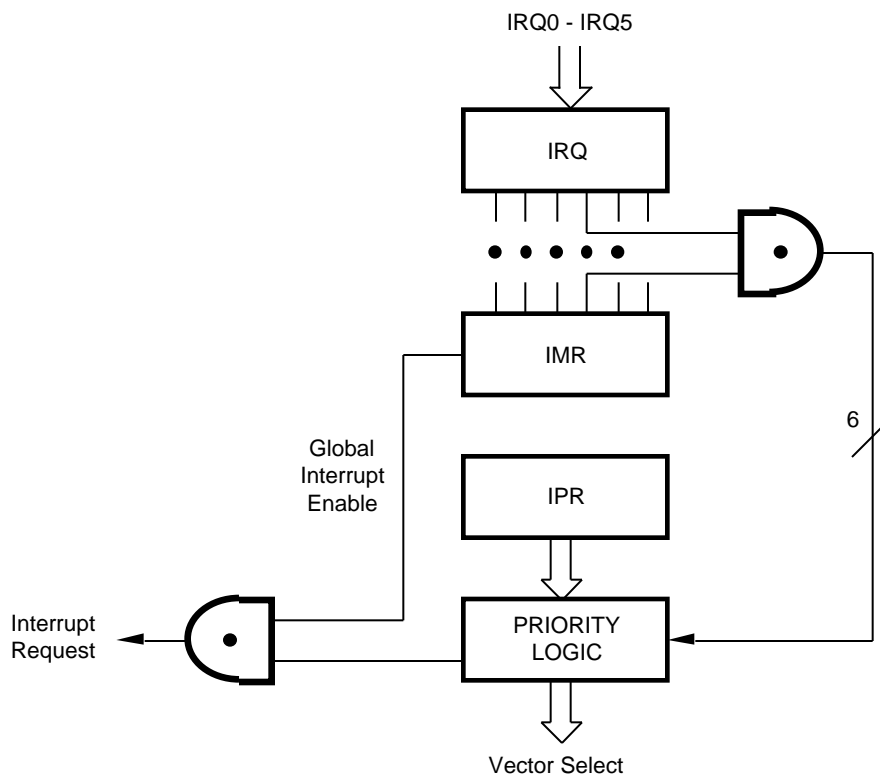
**Interrupts.** The Z86C21 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follow: four sources are claimed by Port 3, lines P33-P30; one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. (Refer to Table 4.)

All Z86C21 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.



**Figure 16. Interrupt Block Diagram**



**Clock.** The Z86C21 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 16 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recom-

mended capacitors ( $10\text{ pF} < C_L < 300\text{ pF}$ ) from each pin 11, ground instead of just system ground. This prevents noise injection into the clock input (Figure 17).

**Note:** Actual capacitor value is specified by the crystal manufacturer.

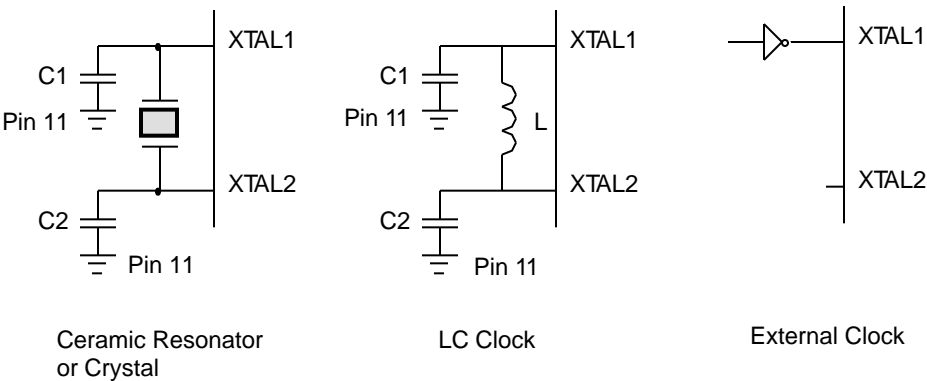


Figure 17. Oscillator Configuration

**HALT.** Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5  $\mu\text{A}$  (typical) or less. The STOP mode is terminated by a reset which causes the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction. i.e.,

```
FF NOP    ; clear the pipeline
6F STOP   ; enter STOP mode
or
FF NOP    ; clear the pipeline
7F HALT   ; enter HALT mode
```

# ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage*	-0.3	+7.0	V
$T_{STG}$	Storage Temp	-65	+150	°C
$T_A$	Oper Ambient Temp		†	°C

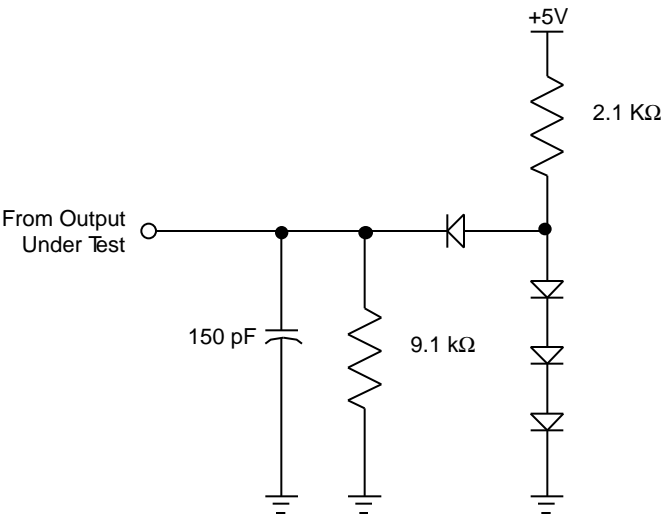
**Notes:**

\* Voltages on all pins with respect to GND.  
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

# STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).



**Figure 18. Test Load Diagram**

## DC CHARACTERISTICS

Sym	Parameter	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$		$T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		Typical @ $25^{\circ}\text{C}$	Units	Conditions
		Min	Max	Min	Max			
	Max Input Voltage		7		7		V	$I_{IN} < 250\text{ }\mu\text{A}$
$V_{CH}$	Clock Input High Voltage	3.8	$V_{CC}+0.3$	3.8	$V_{CC}+0.3$		V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	2	$V_{CC}+0.3$	2.0	$V_{CC}+0.3$		V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
$V_{OH}$	Output High Voltage	2.4		2.4			V	$I_{OH} = -2.0\text{ mA}$
$V_{OH}$	Output High Voltage	$V_{CC} - 100\text{ mV}$		$V_{CC} - 100\text{ mV}$			V	$I_{OH} = -100\text{ }\mu\text{A}$
$V_{OL}$	Output Low Voltage		0.4		0.4		V	$I_{OL} = +5.0\text{ mA}$
$V_{RH}$	Reset Input High Voltage	3.8	$V_{CC}+0.3$	3.8	$V_{CC}+0.3$		V	
$V_{RI}$	Reset Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
$I_{IL}$	Input Leakage	-2	2	-2	2		$\mu\text{A}$	$V_{IN} = 0\text{V}, V_{CC}$
$I_{OL}$	Output Leakage	-2	2	-2	2		$\mu\text{A}$	$V_{IN} = 0\text{V}, V_{CC}$
$I_{IR}$	Reset Input Current		-80		-80		$\mu\text{A}$	$V_{RL} = 0\text{V}$
$I_{CC}$	Supply Current		30		30	20	mA	[1] @ 12 MHz
			35		35	24	mA	[1] @ 16 MHz
$I_{CC1}$	Standby Current		6.5		6.5	4	mA	[1] HALT mode $V_{IN} = 0\text{V}, V_{CC}$ @ 12 MHz
			7		7	4.5	mA	[1] HALT mode $V_{IN} = 0\text{V}, V_{CC}$ @ 16 MHz
$I_{CC2}$	Standby Current		10		20	1	$\mu\text{A}$	[1] STOP mode $V_{IN} = 0\text{V}, V_{CC}$
$I_{ALL}$	Auto Latch Low Current	-10	10	-14	14	5	$\mu\text{A}$	

### Note:

[1] All inputs driven to either 0V or  $V_{CC}$ , outputs floating.

**AC CHARACTERISTICS**

External I/O or Memory Read or Write Timing Diagram

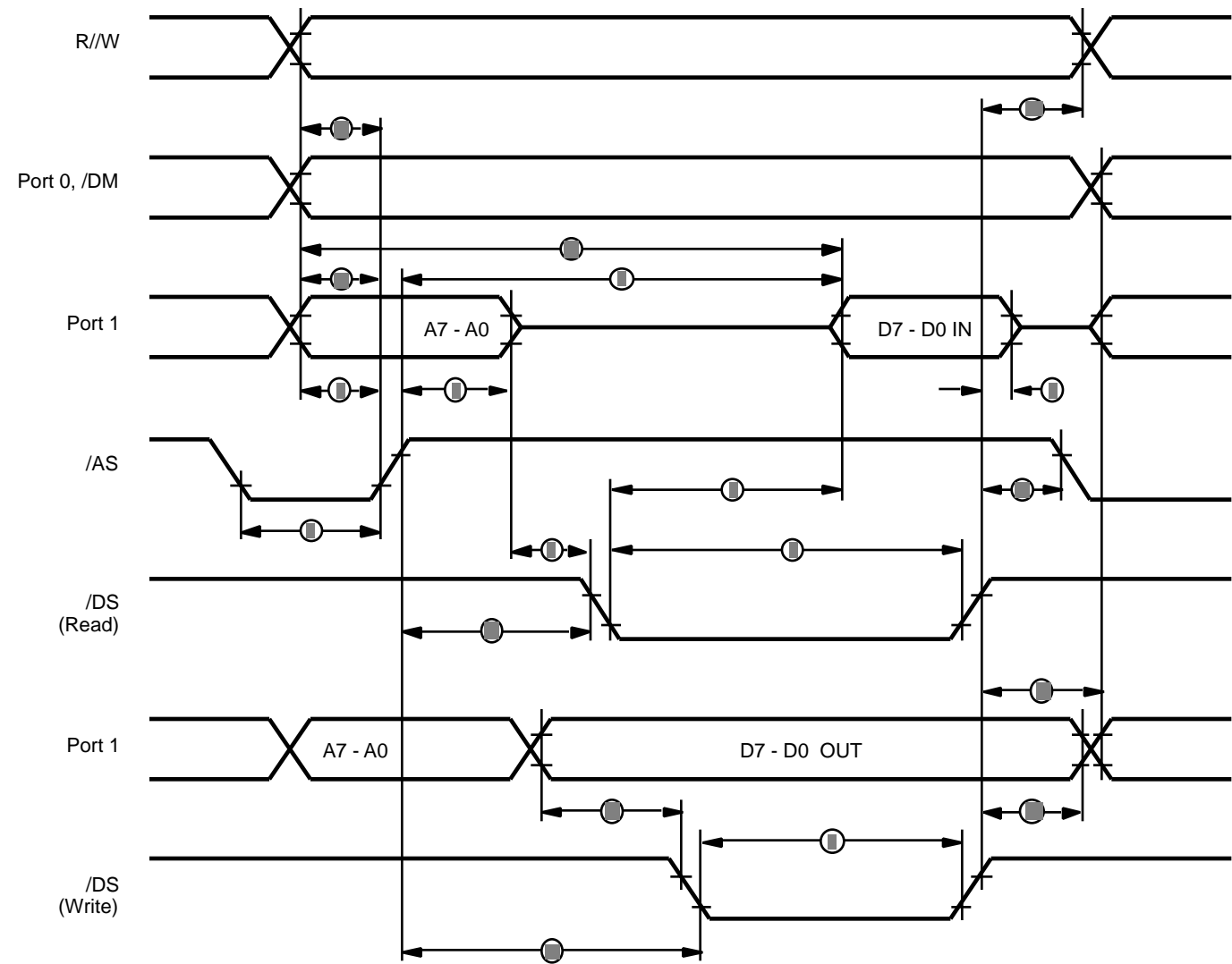


Figure 19. External I/O or Memory Read/Write Timing

## AC CHARACTERISTICS

### External I/O or Memory Read or Write Timing Table

No	Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C				T <sub>A</sub> = –40°C to +105°C				Units	Notes
			12 MHz		16 MHz		12 MHz		16 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	35		25		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		35		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		250		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		40		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	65		50		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	45		35		45		35		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	50		35		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	55		35		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		310		230		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	65		45		65		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS Rise Delay	50		30		50		30		ns	[2,3]

#### Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

#### Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	$0.40TpC + 0.32$
2	TdAS(A)	$0.59TpC - 3.25$
3	TdAS(DR)	$2.83TpC + 6.14$
4	TwAS	$0.66TpC - 1.65$
6	TwDSR	$2.33TpC - 10.56$
7	TwDSW	$1.27TpC + 1.67$
8	TdDSR(DR)	$1.97TpC - 42.5$
10	TdDS(A)	$0.8TpC$
11	TdDS(AS)	$0.59TpC - 3.14$
12	TdR/W(AS)	$0.4TpC$
13	TdDS(R/W)	$0.8TpC - 15$
14	TdDW(DSW)	$0.4TpC$
15	TdDS(DW)	$0.88TpC - 19$
16	TdA(DR)	$4TpC - 20$
17	TdAS(DS)	$0.91TpC - 10.7$
18	TdDM(AS)	$0.9TpC - 26.3$

## AC CHARACTERISTICS

### Additional Timing Diagram

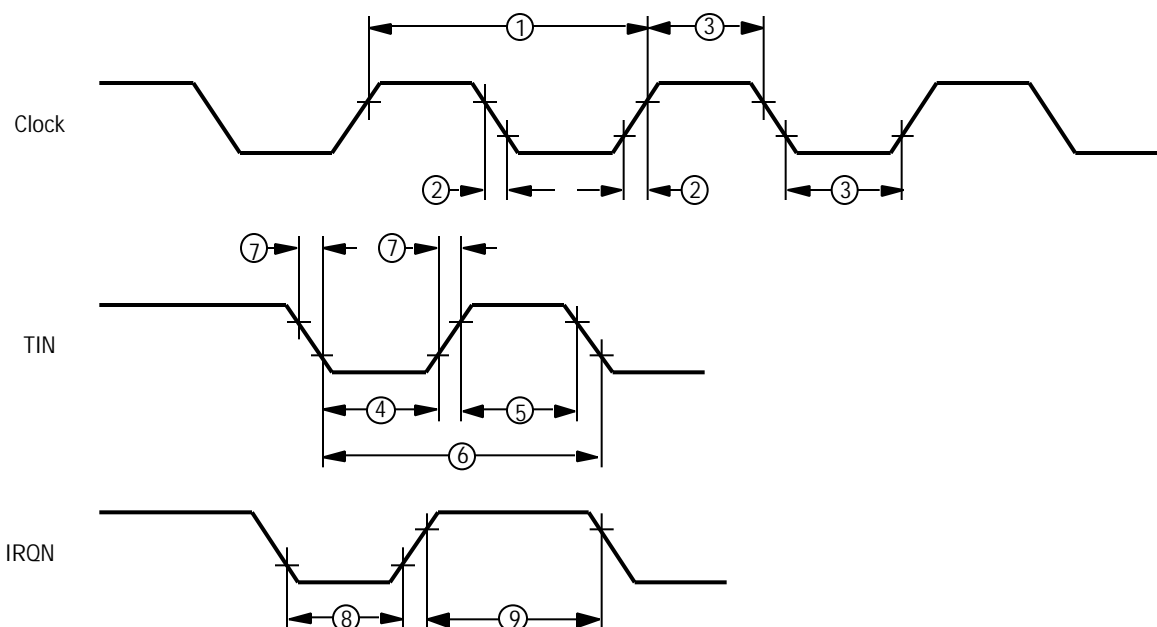


Figure 20. Additional Timing

## AC CHARACTERISTICS

### Additional Timing Table

No	Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +105^\circ\text{C}$						Units	Notes
			12 MHz	16 MHz	12 MHz	16 MHz	Min	Max	Min	Max		
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	35		25		35		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC	3TpC	3TpC	3TpC						[2]
6	TpTin	Timer Input Period	8TpC	8TpC	8TpC	8TpC						[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100	100	100	100					ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70	70	70	50					ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC	3TpC	3TpC	3TpC						[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC	3TpC	3TpC	3TpC						[2,3]

#### Notes:

[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.

[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

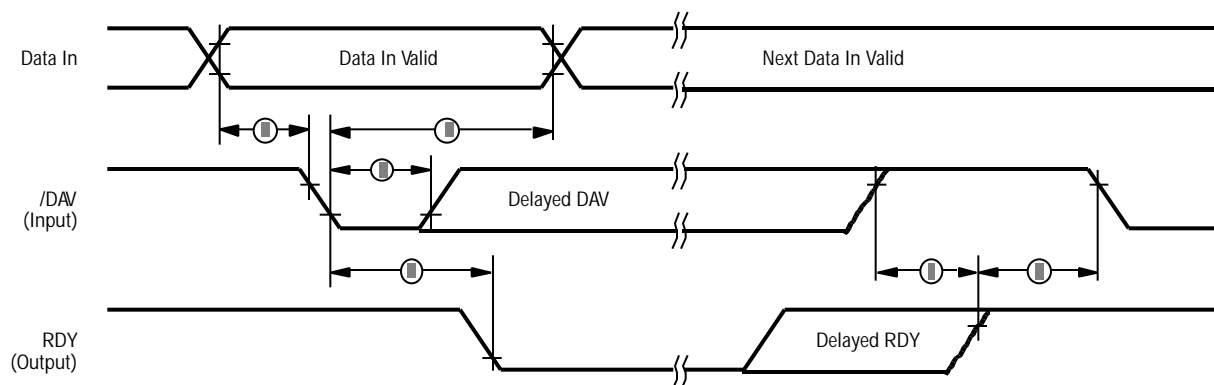
[3] Interrupt references request through Port 3.

[4] Interrupt request through Port 3 (P33-P31).

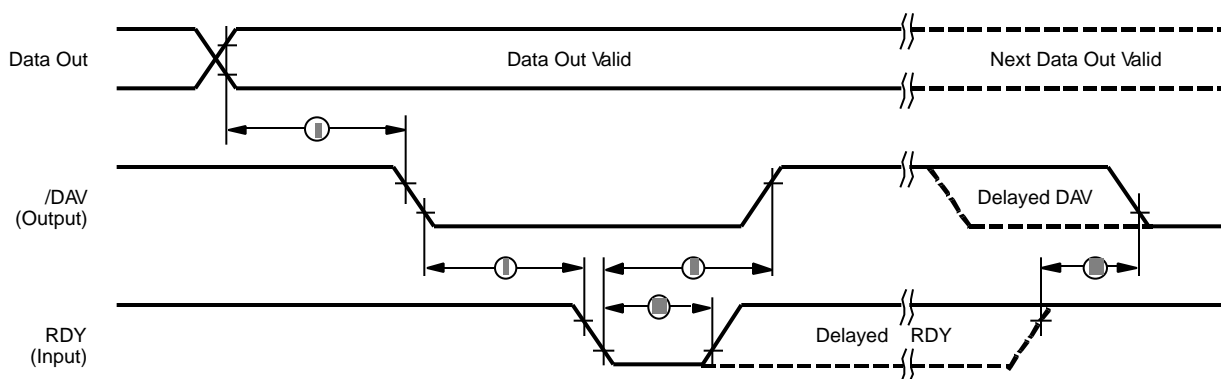
[5] Interrupt request through Port 30.

## AC CHARACTERISTICS

### Handshake Timing Diagrams



**Figure 21. Input Handshake Timing**



**Figure 22. Output Handshake Timing**

## AC CHARACTERISTICS

### Handshake Timing Table

No	Sym	Parameter	T <sub>A</sub> = 0°C to +70°C				T <sub>A</sub> = -40°C to +105°C				Data Direction
			12 MHz	16 MHz	12 MHz	16 MHz	12 MHz	16 MHz	12 MHz	16 MHz	
1	TsDI(DAV)	Data In Setup Time	0	0	0	0	0	0	0	0	IN
2	ThDI(DAV)	Data In Hold Time	145	145	145	145	145	145	145	145	IN
3	TwDAV	Data Available Width	110	110	110	110	110	110	110	110	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVI(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdRDYD(DAV)	RDY Rise to DAV Fall Delay	0	0	0	0	0	0	0	0	IN
7	TdDO(DAV)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TdDAVO(RDY)	DAV Fall to RDY Fall Delay	0	0	0	0	0	0	0	0	OUT
9	TdRDYD(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110	110	110	110	110	110	110	110	OUT
11	TdRDYd(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

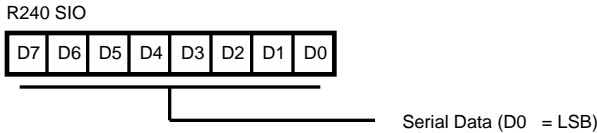


Figure 23. Serial I/O Register  
(F0<sub>H</sub>: Read/Write)

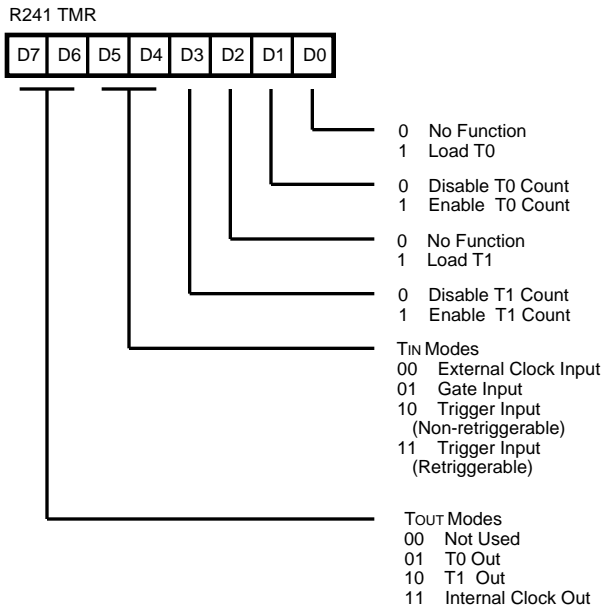


Figure 24. Timer Mode Register  
(F1<sub>H</sub>: Read/Write)

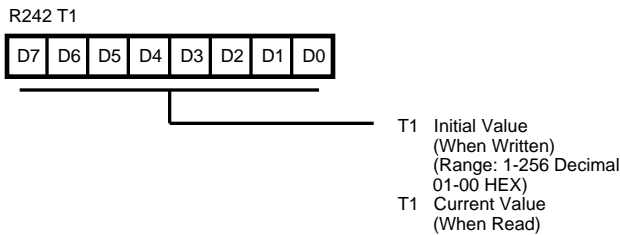


Figure 25. Counter/Timer 1 Register  
(F2<sub>H</sub>: Read/Write)

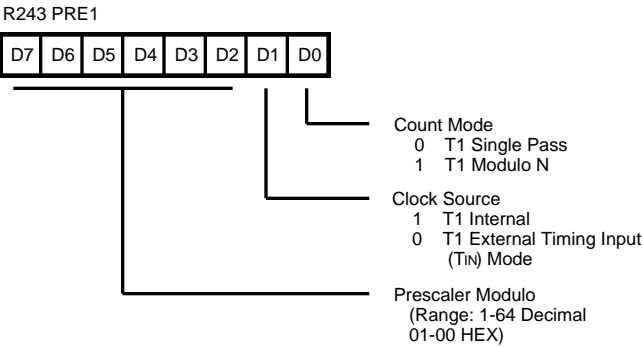


Figure 26. Prescaler 1 Register  
(F3<sub>H</sub>: Write Only)

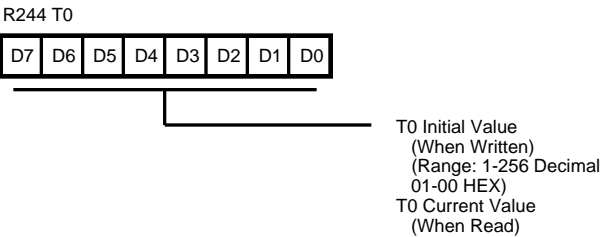


Figure 27. Counter/Timer 0 Register  
(F4<sub>H</sub>: Read/Write)

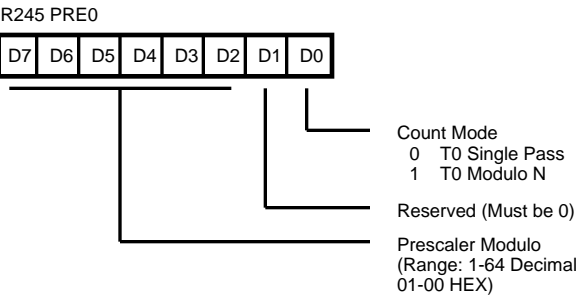
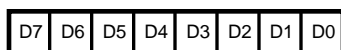


Figure 28. Prescaler 0 Register  
(F5<sub>H</sub>: Write Only)



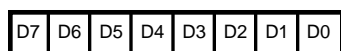
R246 P2M



P2<sub>0</sub> - P2<sub>7</sub> I/O Definition  
 0 Defines Bit as Output  
 1 Defines Bit as Input

**Figure 29. Port 2 Mode Register  
(F6<sub>H</sub>: Write Only)**

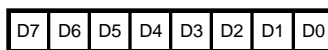
R247 P3M



0 Port 2 Open Drain  
 1 Port 2 Push-pull  
 Reserved (Must be 0)  
 0 P3<sub>2</sub> = Input  
 P3<sub>5</sub> = Output  
 1 P3<sub>2</sub> = /DAV0/RDY0  
 P3<sub>5</sub> = RDY0//DAV0  
 00 P3<sub>3</sub> = Input  
 P3<sub>4</sub> = Output  
 01 P3<sub>3</sub> = Input  
 10 P3<sub>4</sub> = /DM  
 11 P3<sub>3</sub> = /DAV1/RDY1  
 P3<sub>4</sub> = RDY1//DAV1  
 0 P3<sub>1</sub> = Input (TIN)  
 P3<sub>6</sub> = Output (TOUT)  
 1 P3<sub>1</sub> = /DAV2/RDY2  
 P3<sub>6</sub> = RDY2//DAV2  
 0 P3<sub>0</sub> = Input  
 P3<sub>7</sub> = Output  
 1 P3<sub>0</sub> = Serial In  
 P3<sub>7</sub> = Serial Out  
 0 Parity Off  
 1 Parity On

**Figure 30. Port 3 Mode Register  
(F7<sub>H</sub>: Write Only)**

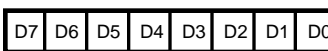
R248 P01M



P0<sub>0</sub> - P0<sub>0</sub> Mode  
 00 Output  
 01 Input  
 1X A<sub>11</sub> - A<sub>8</sub>  
 Stack Selection  
 0 External  
 1 Internal  
 P1<sub>7</sub> - P1<sub>0</sub> Mode  
 00 Byte Output  
 01 Byte Input  
 10 AD<sub>7</sub> - AD<sub>0</sub>  
 11 High-Impedance AD<sub>7</sub> - DA<sub>0</sub>,  
 /AS, /DS, /R/W, A<sub>11</sub> - A<sub>8</sub>,  
 A<sub>15</sub> - A<sub>12</sub>, If Selected  
 External Memory Timing  
 0 Normal  
 1 Extended  
 P0<sub>7</sub> - P0<sub>4</sub> Mode  
 00 Output  
 01 Input  
 1X A<sub>15</sub> - A<sub>12</sub>

**Figure 31. Port 0 and 1 Mode Register  
(F8<sub>H</sub>: Write Only)**

R249 IPR



Interrupt Group Priority  
 Reserved = 000  
 C > A > B = 001  
 A > B > C = 010  
 A > C > B = 011  
 B > C > A = 100  
 C > B > A = 101  
 B > A > C = 110  
 Reserved = 111  
 IRQ1, IRQ4 Priority (Group C)  
 0 IRQ1 > IRQ4  
 1 IRQ4 > IRQ1  
 IRQ0, IRQ2 Priority (Group B)  
 0 IRQ2 > IRQ0  
 1 IRQ0 > IRQ2  
 IRQ3, IRQ5 Priority (Group A)  
 0 IRQ5 > IRQ3  
 1 IRQ3 > IRQ5  
 Reserved (Must be 0)

**Figure 32. Interrupt Priority Register  
(F9<sub>H</sub>: Write Only)**

Z8 CONTROL REGISTER DIAGRAMS (Continued)

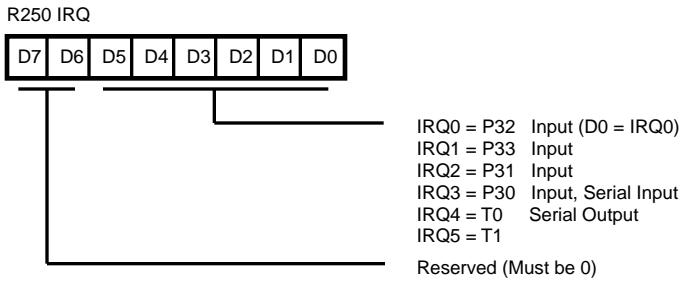


Figure 33. Interrupt Request Register  
(FA<sub>H</sub>: Read/Write)

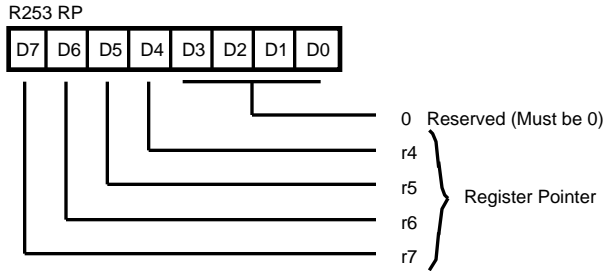


Figure 36. Register Pointer Register  
(FD<sub>H</sub>: Read/Write)

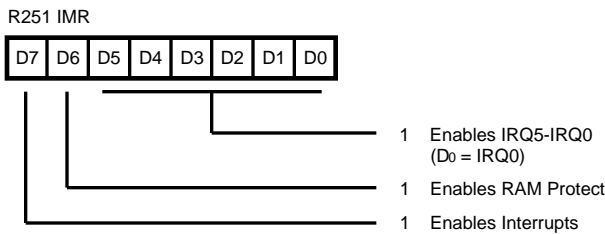


Figure 34. Interrupt Mask Register  
(FB<sub>H</sub>: Read/Write)

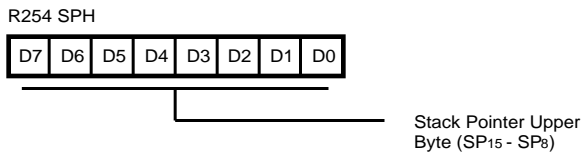


Figure 37. Stack Pointer Register  
(FE<sub>H</sub>: Read/Write)

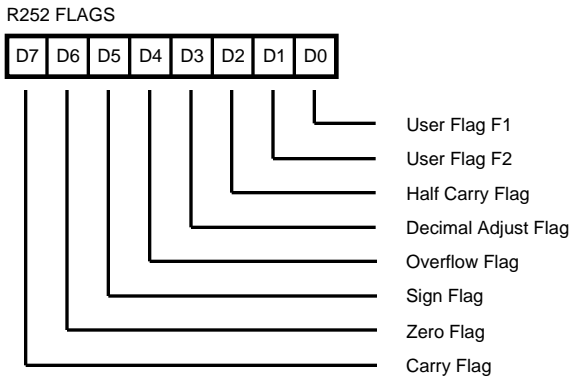


Figure 35. Flag Register  
(FC<sub>H</sub>: Read/Write)

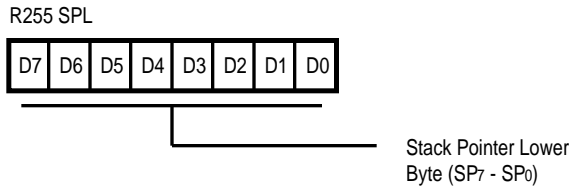


Figure 38. Stack Pointer Register  
(FF<sub>H</sub>: Read/Write)

---

## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

**Symbols.** The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

**Flags.** Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

---

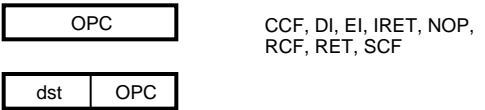
---

## CONDITION CODES

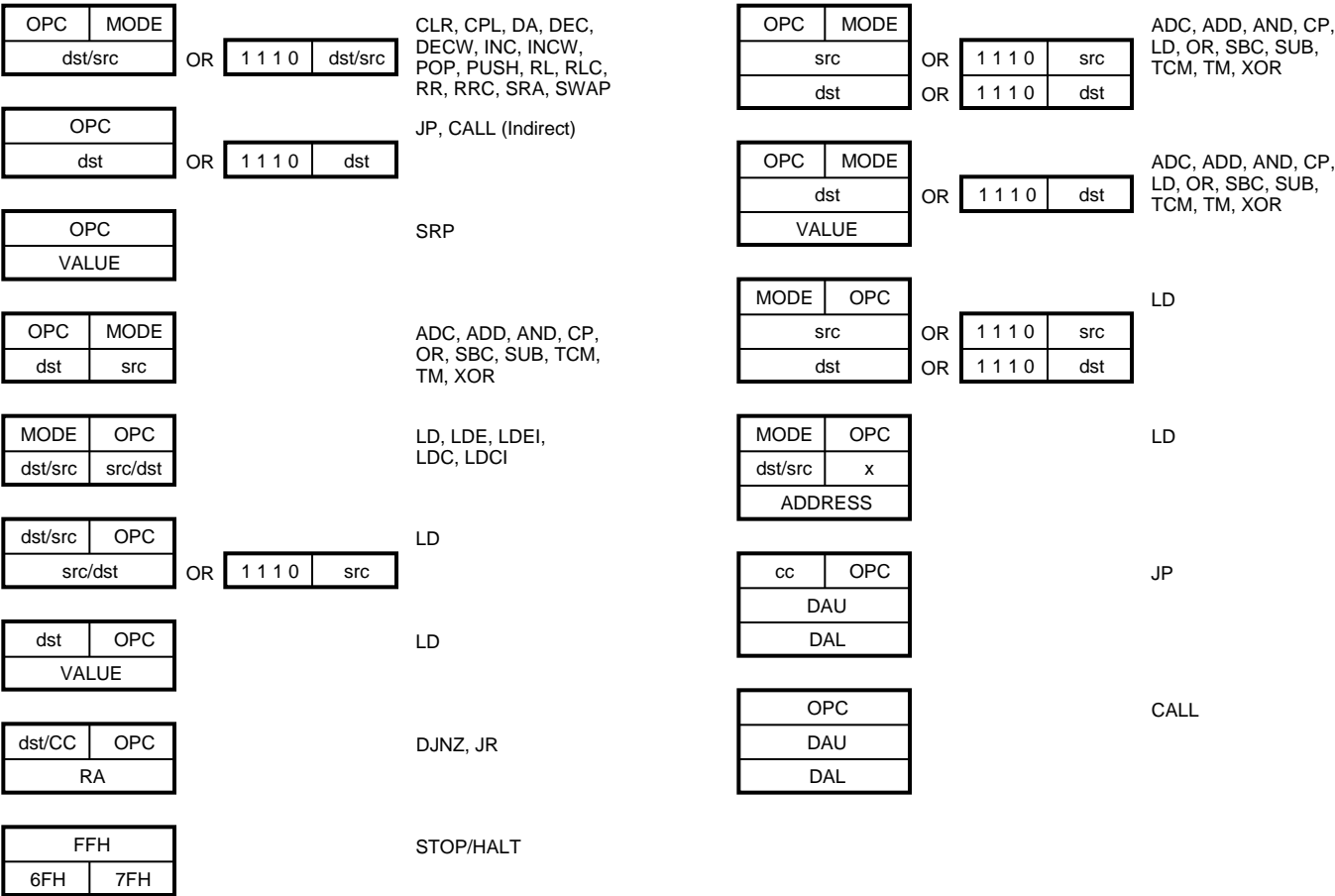
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	$C = 1$
1111	NC	No Carry	$C = 0$
0110	Z	Zero	$Z = 1$
1110	NZ	Not Zero	$Z = 0$
1101	PL	Plus	$S = 0$
0101	MI	Minus	$S = 1$
0100	OV	Overflow	$V = 1$
1100	NOV	No Overflow	$V = 0$
0110	EQ	Equal	$Z = 1$
1110	NE	Not Equal	$Z = 0$
1001	GE	Greater Than or Equal	$(S \text{ XOR } V) = 0$
0001	LT	Less than	$(S \text{ XOR } V) = 1$
1010	GT	Greater Than	$[Z \text{ OR } (S \text{ XOR } V)] = 0$
0010	LE	Less Than or Equal	$[Z \text{ OR } (S \text{ XOR } V)] = 1$
1111	UGE	Unsigned Greater Than or Equal	$C = 0$
0111	ULT	Unsigned Less Than	$C = 1$
1011	UGT	Unsigned Greater Than	$(C = 0 \text{ AND } Z = 0) = 1$
0011	ULE	Unsigned Less Than or Equal	$(C \text{ OR } Z) = 1$
0000	F	Never True (Always False)	

---

INSTRUCTION FORMATS



One-Byte Instructions



OPC

MODE

src

dst

OR

1 1 1 0

src

ADC, ADD, AND, CP,  
LD, OR, SBC, SUB,  
TCM, TM, XOR

OR

1 1 1 0

dst

OPC

MODE

dst

VALUE

ADC, ADD, AND, CP,  
LD, OR, SBC, SUB,  
TCM, TM, XOR

MODE

OPC

src

dst

OR

1 1 1 0

src

LD

OR

1 1 1 0

dst

MODE

OPC

dst/src

x

ADDRESS

LD

cc

OPC

DAU

DAL

JP

OPC

DAU

DAL

CALL

Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

**Note:** Assignment of a value is indicated by the symbol “ ← ”. For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation “addr (n)” is used to refer to bit (n) of a given operand location. For example:

dst (7)

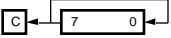
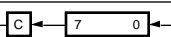
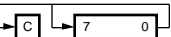
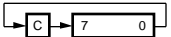
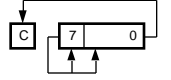
refers to bit 7 of the destination operand.

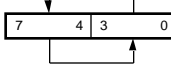
## INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address		Opcode Byte (Hex)	Flags Affected						
	Mode	dst src		C	Z	S	V	D	H	
<b>ADC</b> dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*	
<b>ADD</b> dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*	
<b>AND</b> dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-	
<b>CALL</b> dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-	
<b>CCF</b> C←NOT C			EF	*	-	-	-	-	-	
<b>CLR</b> dst dst←0	R IR		B0 B1	-	-	-	-	-	-	
<b>COM</b> dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-	
<b>CP</b> dst, src dst - src	†		A[ ]	*	*	*	*	-	-	
<b>DA</b> dst dst←DA dst	R IR		40 41	*	*	*	X	-	-	
<b>DEC</b> dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-	
<b>DECW</b> dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-	
<b>DI</b> IMR(7)←0			8F	-	-	-	-	-	-	
<b>DJNZ</b> r, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-	
<b>EI</b> IMR(7)←1			9F	-	-	-	-	-	-	
<b>HALT</b>			7F	-	-	-	-	-	-	

Instruction and Operation	Address		Opcode Byte (Hex)	Flags Affected						
	Mode	dst src		C	Z	S	V	D	H	
<b>INC</b> dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-	
<b>INCW</b> dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-	
<b>IRET</b> FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*	
<b>JP</b> cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-	
<b>JR</b> cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-	
<b>LD</b> dst, src dst←src	r r R r X r r lr R R R R IR IM IR R	lm R r X r lr r R R R R IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	
<b>LDC</b> dst, src	r	lrr	C2	-	-	-	-	-	-	
<b>LDCI</b> dst, src dst←src r←r + 1; rr←rr + 1	lr	lrr	C3	-	-	-	-	-	-	

## INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
<b>NOP</b>			FF	-	-	-	-	-	-	-
<b>OR</b> dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-	
<b>POP</b> dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-	
<b>PUSH</b> src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-	
<b>RCF</b> C←0			CF	0	-	-	-	-	-	
<b>RET</b> PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-	
<b>RL</b> dst 	R IR		90 91	*	*	*	*	-	-	
<b>RLC</b> dst 	R IR		10 11	*	*	*	*	-	-	
<b>RR</b> dst 	R IR		E0 E1	*	*	*	*	-	-	
<b>RRC</b> dst 	R IR		C0 C1	*	*	*	*	-	-	
<b>SBC</b> dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*	
<b>SCF</b> C←1			DF	1	-	-	-	-	-	
<b>SRA</b> dst 	R IR		D0 D1	*	*	*	0	-	-	
<b>SRP</b> src RP←src		Im	31	-	-	-	-	-	-	

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
<b>STOP</b>			6F	-	-	-	-	-	-	-
<b>SUB</b> dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*	
<b>SWAP</b> dst 	R IR		F0 F1	X	*	*	X	-	-	
<b>TCM</b> dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-	
<b>TM</b> dst, src dst AND src	†		7[ ]	-	*	*	0	-	-	
<b>XOR</b> dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-	

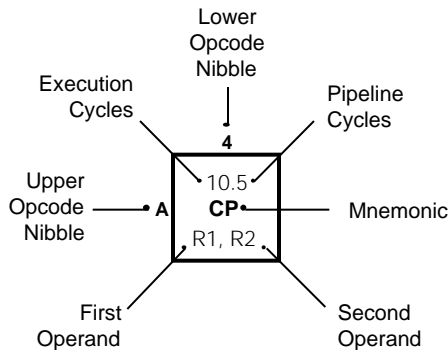
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode		Lower Opcode Nibble
dst	src	
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

# OPCODE MAP

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	6.5 <b>DEC</b> R1	6.5 <b>DEC</b> IR1	6.5 <b>ADD</b> r1, r2	6.5 <b>ADD</b> r1, Ir2	10.5 <b>ADD</b> R2, R1	10.5 <b>ADD</b> IR2, R1	10.5 <b>ADD</b> R1, IM	10.5 <b>ADD</b> IR1, IM	6.5 <b>LD</b> r1, R2	6.5 <b>LD</b> r2, R1	12/10.5 <b>DJNZ</b> r1, RA	12/10.0 <b>JR</b> cc, RA	6.5 <b>LD</b> r1, IM	12.10.0 <b>JP</b> cc, DA	6.5 <b>INC</b> r1	
	1	6.5 <b>RLC</b> R1	6.5 <b>RLC</b> IR1	6.5 <b>ADC</b> r1, r2	6.5 <b>ADC</b> r1, Ir2	10.5 <b>ADC</b> R2, R1	10.5 <b>ADC</b> IR2, R1	10.5 <b>ADC</b> R1, IM	10.5 <b>ADC</b> IR1, IM								
	2	6.5 <b>INC</b> R1	6.5 <b>INC</b> IR1	6.5 <b>SUB</b> r1, r2	6.5 <b>SUB</b> r1, Ir2	10.5 <b>SUB</b> R2, R1	10.5 <b>SUB</b> IR2, R1	10.5 <b>SUB</b> R1, IM	10.5 <b>SUB</b> IR1, IM								
	3	8.0 <b>JP</b> IRR1	6.1 <b>SRP</b> IM	6.5 <b>SBC</b> r1, r2	6.5 <b>SBC</b> r1, Ir2	10.5 <b>SBC</b> R2, R1	10.5 <b>SBC</b> IR2, R1	10.5 <b>SBC</b> R1, IM	10.5 <b>SBC</b> IR1, IM								
	4	8.5 <b>DA</b> R1	8.5 <b>DA</b> IR1	6.5 <b>OR</b> r1, r2	6.5 <b>OR</b> r1, Ir2	10.5 <b>OR</b> R2, R1	10.5 <b>OR</b> IR2, R1	10.5 <b>OR</b> R1, IM	10.5 <b>OR</b> IR1, IM								
	5	10.5 <b>POP</b> R1	10.5 <b>POP</b> IR1	6.5 <b>AND</b> r1, r2	6.5 <b>AND</b> r1, Ir2	10.5 <b>AND</b> R2, R1	10.5 <b>AND</b> IR2, R1	10.5 <b>AND</b> R1, IM	10.5 <b>AND</b> IR1, IM								
	6	6.5 <b>COM</b> R1	6.5 <b>COM</b> IR1	6.5 <b>TCM</b> r1, r2	6.5 <b>TCM</b> r1, Ir2	10.5 <b>TCM</b> R2, R1	10.5 <b>TCM</b> IR2, R1	10.5 <b>TCM</b> R1, IM	10.5 <b>TCM</b> IR1, IM								6.0 <b>STOP</b>
	7	10/12.1 <b>PUSH</b> R2	12/14.1 <b>PUSH</b> IR2	6.5 <b>TM</b> r1, r2	6.5 <b>TM</b> r1, Ir2	10.5 <b>TM</b> R2, R1	10.5 <b>TM</b> IR2, R1	10.5 <b>TM</b> R1, IM	10.5 <b>TM</b> IR1, IM								7.0 <b>HALT</b>
	8	10.5 <b>DECW</b> RR1	10.5 <b>DECW</b> IR1	12.0 <b>LDE</b> r1, Irr2	18.0 <b>LDEI</b> Ir1, Irr2												6.1 <b>DI</b>
	9	6.5 <b>RL</b> R1	6.5 <b>RL</b> IR1	12.0 <b>LDE</b> r2, Irr1	18.0 <b>LDEI</b> Ir2, Irr1												6.1 <b>EI</b>
	A	10.5 <b>INCW</b> RR1	10.5 <b>INCW</b> IR1	6.5 <b>CP</b> r1, r2	6.5 <b>CP</b> r1, Ir2	10.5 <b>CP</b> R2, R1	10.5 <b>CP</b> IR2, R1	10.5 <b>CP</b> R1, IM	10.5 <b>CP</b> IR1, IM								14.0 <b>RET</b>
	B	6.5 <b>CLR</b> R1	6.5 <b>CLR</b> IR1	6.5 <b>XOR</b> r1, r2	6.5 <b>XOR</b> r1, Ir2	10.5 <b>XOR</b> R2, R1	10.5 <b>XOR</b> IR2, R1	10.5 <b>XOR</b> R1, IM	10.5 <b>XOR</b> IR1, IM								16.0 <b>IRET</b>
	C	6.5 <b>RRC</b> R1	6.5 <b>RRC</b> IR1	12.0 <b>LDC</b> r1, Irr2	18.0 <b>LDCI</b> Ir1, Irr2				10.5 <b>LD</b> r1,x,R2								6.5 <b>RCF</b>
	D	6.5 <b>SRA</b> R1	6.5 <b>SRA</b> IR1	12.0 <b>LDC</b> r1, Irr2	18.0 <b>LDCI</b> Ir1, Irr2	20.0 <b>CALL*</b> IRR1		20.0 <b>CALL</b> DA	10.5 <b>LD</b> r2,x,R1								6.5 <b>SCF</b>
	E	6.5 <b>RR</b> R1	6.5 <b>RR</b> IR1		6.5 <b>LD</b> r1, IR2	10.5 <b>LD</b> R2, R1	10.5 <b>LD</b> IR2, R1	10.5 <b>LD</b> R1, IM	10.5 <b>LD</b> IR1, IM								6.5 <b>CCF</b>
	F	8.5 <b>SWAP</b> R1	8.5 <b>SWAP</b> IR1		6.5 <b>LD</b> Ir1, r2		10.5 <b>LD</b> R2, IR1										6.0 <b>NOP</b>
		2				3				2		2		3		1	
		Bytes per Instruction															



## Legend:

R = 8-bit Address  
r = 4-bit Address  
R1 or r1 = Dst Address  
R2 or r2 = Src Address

## Sequence:

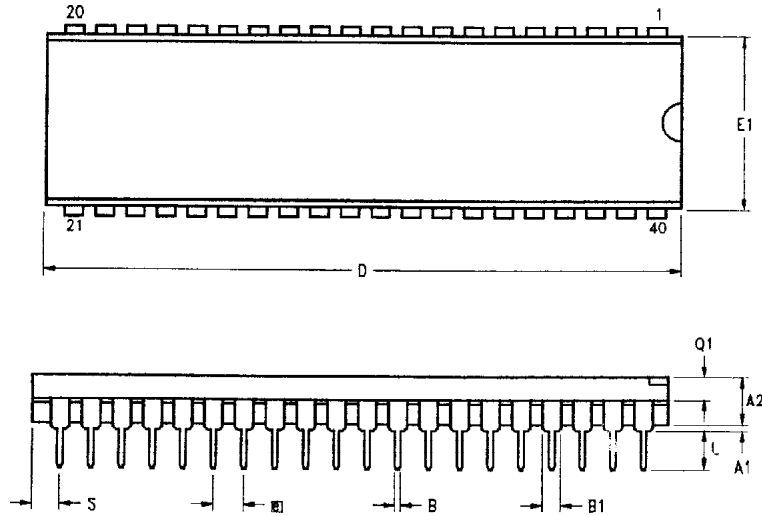
Opcode, First Operand,  
Second Operand

**Note:** Blank areas not defined.

\*2-byte instruction appears as  
a 3-byte instruction

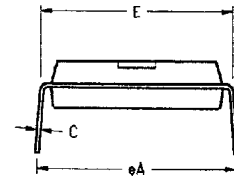


## PACKAGE INFORMATION

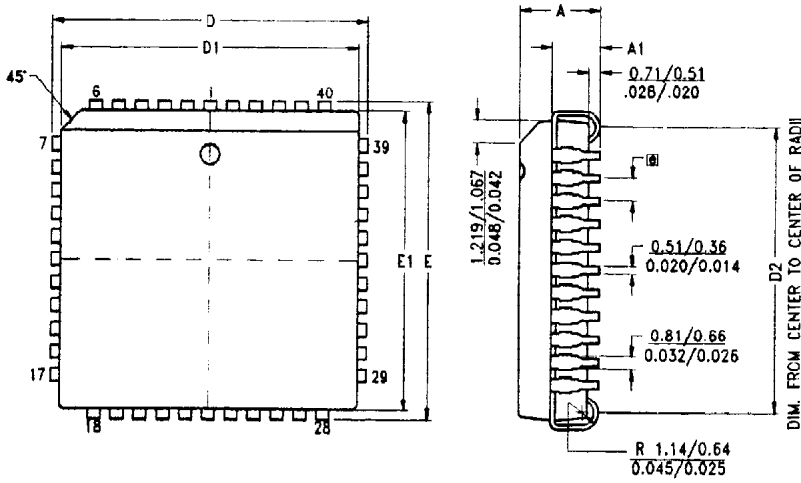


CONTROLLING DIMENSIONS : INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
⌀	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090



40-Pin PDIP Package Diagram



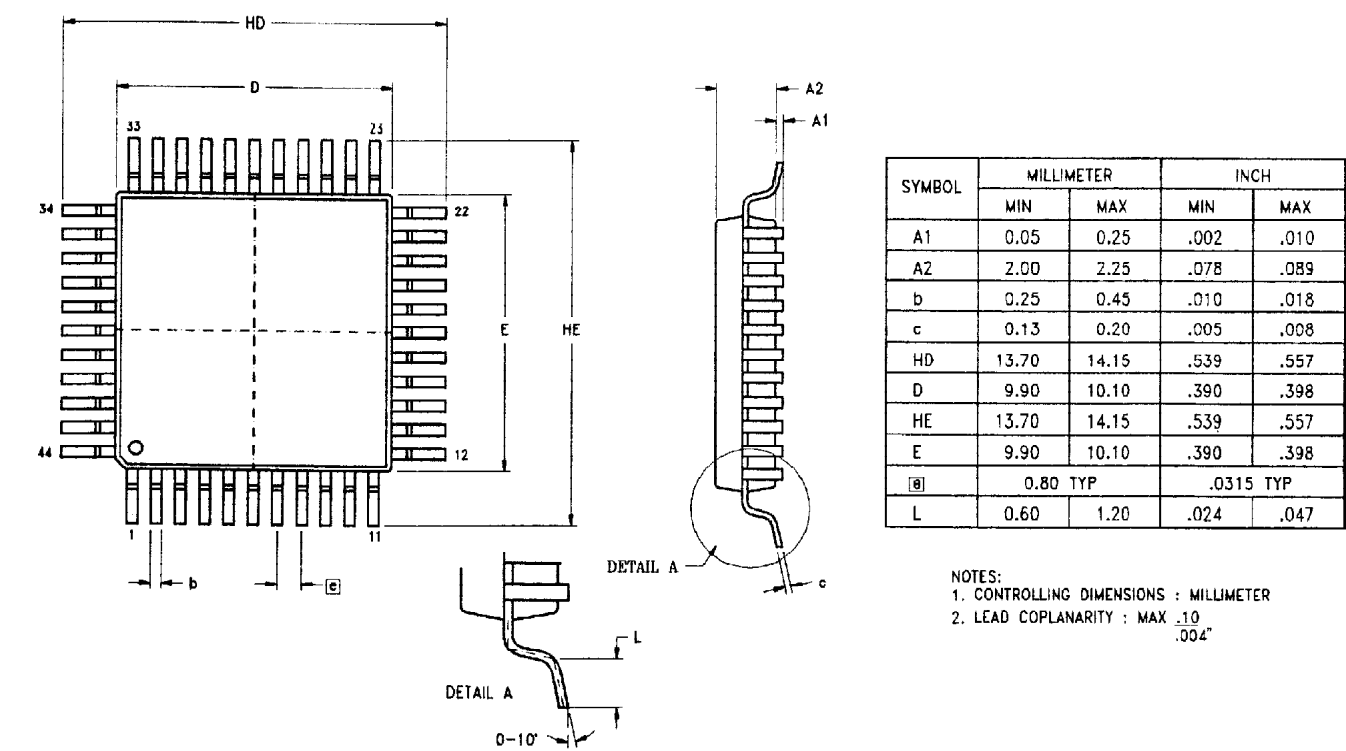
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.500	0.630
⌀	1.27 TYP		0.050 TYP	

NOTES:

1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION :  $\frac{MM}{INCH}$

44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)



44-Pin QFP Package Diagram

## ORDERING INFORMATION

### Z86C21

#### 12 MHz

##### 40-pin DIP

Z86C2112PSC

Z86C2112PEC

##### 44-pin PLCC

Z86C2112VSC

Z86C2112VEC

##### 44-pin QFP

Z86C2112FSC

Z86C2112FEC

#### 16 MHz

##### 40-pin DIP

Z86C2116PSC

##### 44-pin PLCC

Z86C2116VSC

##### 44-pin QFP

Z86C2116FSC

For fast results, contact your local Zilog Sales Office for assistance in ordering the part desired.

## CODES

### Preferred Package

P = Plastic DIP

V = Plastic Chip Carrier

### Longer Lead Time

F = Plastic Quad Flat Pack

### Preferred Temperature

S = 0°C to +70°C

### Longer Lead Time

E = -40°C to +105°C

### Speeds

12 = 12 MHz

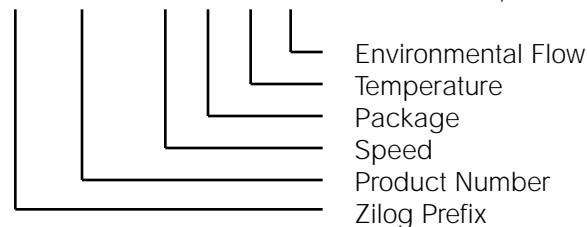
16 = 16 MHz

### Environmental

C = Plastic Standard

#### Example:

**Z 89C21 12 P S C** is a Z89C21, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



© 1997 by Zilog, Inc. All rights reserved. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Zilog, Inc. The information in this document is subject to change without notice. Devices sold by Zilog, Inc. are covered by warranty and patent indemnification provisions appearing in Zilog, Inc. Terms and Conditions of Sale only.

ZILOG, INC. MAKES NO WARRANTY, EXPRESS, STATUTORY, IMPLIED OR BY DESCRIPTION, REGARDING THE INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED DEVICES FROM INTELLECTUAL PROPERTY INFRINGEMENT. ZILOG, INC. MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE.

Zilog, Inc. shall not be responsible for any errors that may appear in this document. Zilog, Inc. makes no commitment to update or keep current the information contained in this document.

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Zilog, Inc. 210 East Hacienda Ave.  
Campbell, CA 95008-6600  
Telephone (408) 370-8000  
Telex 910-338-7621  
FAX 408 370-8056  
Internet: <http://www.zilog.com>