



Z84C10

CMOS Z80[®] DMA DIRECT
MEMORY ACCESS CONTROLLER

GENERAL DESCRIPTION

The Z80[®] DMA (Direct Memory Access), hereafter referred to as Z80 DMA or DMA, is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte

searches can be performed either concurrently with transfers or as an operation itself.

The Z80 DMA contains direct interfacing to and independent control of, system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart, minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The Z80 DMA is packaged in a 40-pin plastic or Cerdip DIP, or 44-pin PLCC. It uses a single +5V power supply and the standard Z80 Family single-phase clock.

GENERAL DESCRIPTION (Continued)

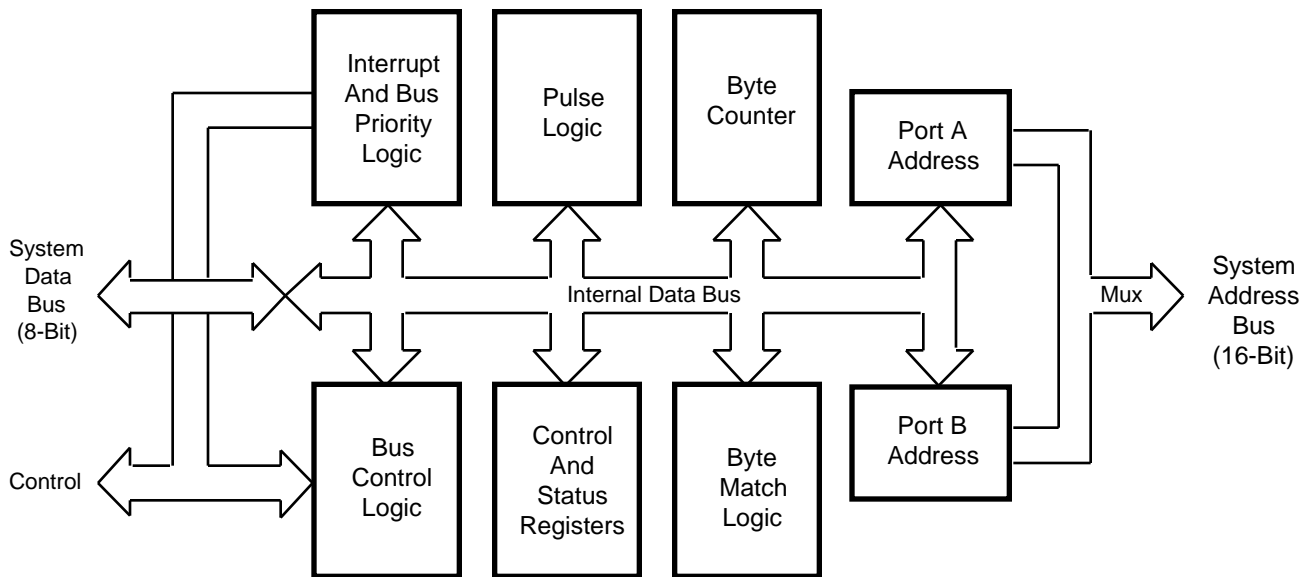


Figure 1. Z84C10 Functional Block Diagram

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