PRELIMINARY

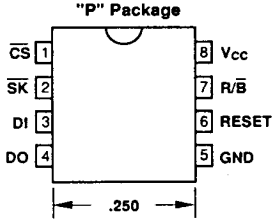
4096-Bit Serial (5V) Electrically Erasable PROM

FEATURES

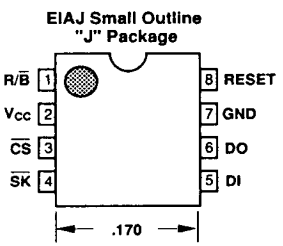
- **4096-bit Serial Architecture**
  - **—256 registers, 16 bits each**
  - **—Nonvolatile data storage**
  - **—Single 5V supply**
- **Versatile, Easy-to-Use Interface**
  - **—READY/$\overline{\text{BUSY}}$ status signal**
  - **—Automatic write cycle time-out**
  - **—Software controlled write protection**
- **Advanced CMOS E²PROM Technology**
- **Low Power Consumption**
  - **—3mA max. active**
  - **—1mA max. standby, TTL**
  - **—25µA max. standby CMOS**
- **Up to 10,000 Erase/Write Cycles Per Register**
- **10 Year Data Retention**

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



EIAJ Small Outline "J" Package



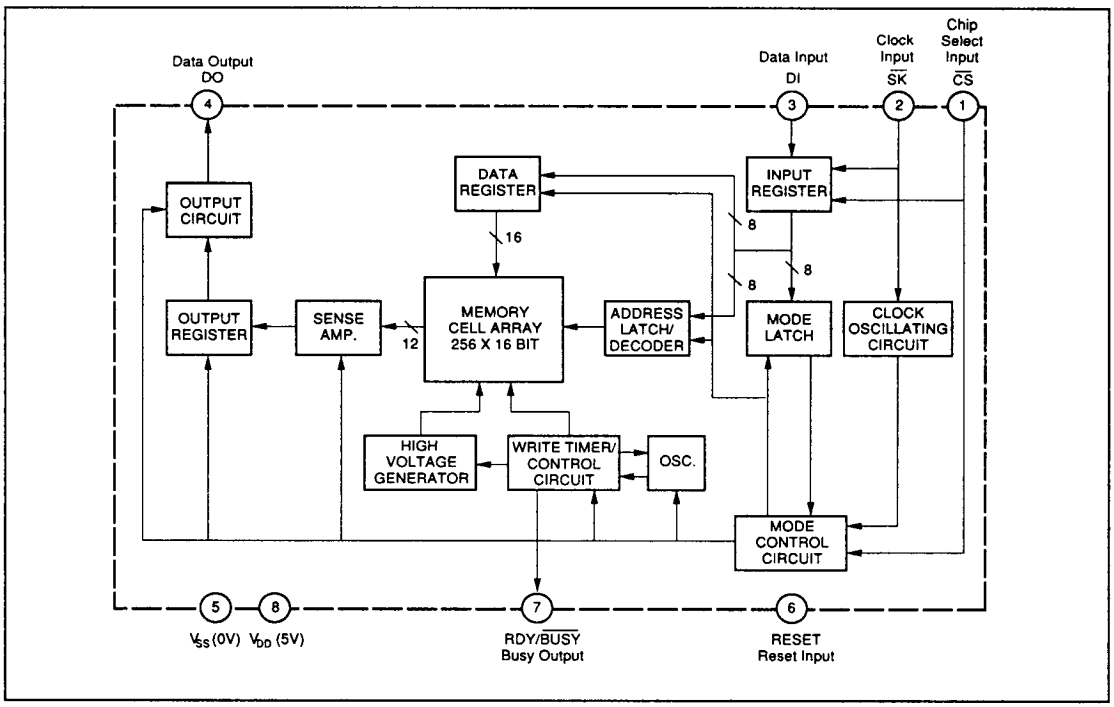
OVERVIEW

The XL90C41 is a 4096-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL90C41 provides external read/write memory arranged as 256 registers of 16 bits each. Five 8-bit instructions control the operation of the device, which include read, write, enable and status functions. The XL90C41 has been designed for applications requiring up to 10,000 erase/write cycles per register. In the standby mode, the XL90C41 reduces power consumption by more than 80%, compared to an NMOS counterpart.

PIN NAMES

$\overline{\text{CS}}$	Chip Select
$\overline{\text{SK}}$	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
RESET	Reset Input
R/$\overline{\text{B}}$	READY/$\overline{\text{BUSY}}$ Output
Vcc	Power Supply

BLOCK DIAGRAM



APPLICATIONS

The XL90C41 is ideal for high volume applications requiring low density data storage. It uses a low cost, space saving 8-pin package, and readily interfaces with standard microprocessors and popular microcontrollers such as the 8048/49/51/96, the COP4XX series, the 6801/05, the TMS1000 and the Z8.

Candidate applications include alarm devices, appliances, computer terminals and smart cards, electronic locks, meters, robotics and telephone, to name just a few.

ENDURANCE AND DATA RETENTION

The XL90C41 is designed for applications requiring up to 10,000 write cycles per bit. It provides 10 years of secure data retention, with or without power applied.

DEVICE OPERATION

The XL90C41 is a clocked serial port compatible E²PROM. Input data is latched on the rising edge of the clock, and data is output on the falling edge of the clock.

Data is grouped in 8-bit bytes. The beginning 8 bits specify the mode, the next 8 bits specify the address, and subsequent 16 bits specify the I/O data.

During the self-timed internal programming cycle that accompanies a write, the $\overline{SK}$ clock is de-activated. It is needed only when instructions or data are being passed to or from the memory.

Any of the six modes (read, write, write enable, write disable, erase all and write all) may be specified. The write time is set by internal timer, and determination of whether a write operation is in progress or not can be made from the status of the READY/$\overline{BUSY}$ pin. When the asynchronous RESET pin is taken HIGH, any ongoing operation is immediately halted.

Read (READ)
The read instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into the output register. The output on DO changes during the HIGH to LOW transition of $\overline{SK}$.

Write (WRITE)
After a write instruction and its address have been decoded, the device expects 16 bits of data. These are to be transferred into the specific memory register which has previously been automatically erased. After the last data bit has been clocked into DI on the 32nd clock edge, the self-timed internal programming cycle is initiated. The write cycle status can be monitored by observing the READY/$\overline{BUSY}$ pin.

Write Enable/Disable (EWEN, EWDS) — When the XL90C41 is powered up, it comes up in the write disabled state. In order to be programmable, it must receive an enable instruction. The device remains programmable until a disable instruction is entered, or until it is powered down. The disable instruction provides protection against inadvertent writes. Read capability is not affected.

Erase All (ERAL)
Full-chip erase is provided for ease in programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."

Write All (WRAL)
The write all command forces all registers in the memory array to an arbitrary 16-bit pattern. Like the standard write instruction, this instruction is followed by 16-bits of serial data on the DI pin. The erase all command should be entered before forcing write all command.

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address	Input Data
READ	1010	1000	A_0-A_7	
WRITE	1010	0100	A_0-A_7	D_0-D_{15}
Erase/Write Enable (EWEN)	1010	0011	XXXXXXXX	
Erase/Write Disable (EWDS)	1010	0000	XXXXXXXX	
Erase All Registers (ERAL)	1010	0010	XXXXXXXX	
Write All Registers (WRAL)	1010	0001	XXXXXXXX	D_0-D_{15}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -40°C to +70°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin. ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS90C41 or -40°C to +85°C for XLE90C41, V_{CC} = 5V ±10%

			XLS90C41		XLE90C41		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
I_{CC1}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz CMOS Input Levels		3		3	mA
I_{CC2}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz TTL Input Levels		3		3	mA
I_{CC3}	Standby Current	$\overline{CS}$ = 0V DI = $\overline{SK}$ = PE = Vcc		100, 3*		100, 3*	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, $\overline{CS}$, $\overline{SK}$, DI		2		2	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc		2		2	µA
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0		2		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL	2.4		2.4		V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL		0.4		0.4	V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

* -A = 100µA, -B = 3µA

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS90C41 or -40°C to +85°C for the XLE90C41, V_{CC} = 5V ±10%

			XLS90C41		XLE90C41		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SK}	$\overline{SK}$ Clock Frequency			1		1	MHz
t_{SKH}	$\overline{SK}$ HIGH Time		450		450		ns
t_{SKL}	$\overline{SK}$ LOW Time		450		450		ns
t_{CS}	Minimum $\overline{CS}$ HIGH Time		1		1		µs
t_{CSS}	$\overline{CS}$ Setup Time	Relative to $\overline{SK}$ ⌝	200		200		ns
t_{DIS}	DI Setup Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to $\overline{SK}$ ⌟	0		0		ns
t_{DIH}	DI Hold Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{PD1}	Output Delay to "1"	AC Test		350		350	ns
t_{PD0}	Output Delay to "0"	AC Test		350		350	ns
t_{SV}	$\overline{CS}$ to Status Valid	AC Test		1		1	µs
t_{DF}	$\overline{CS}$ to DO in 3-state	$\overline{CS}$ = V_{IL}		400		400	ns
$t_{E/W}$	Write Cycle Time			10		10	ms

CAPACITANCE

T_A = 25°C, f = 1MHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

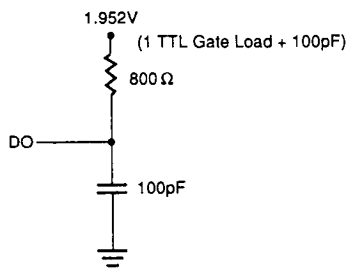


FIGURE 1. AC TEST CONDITIONS

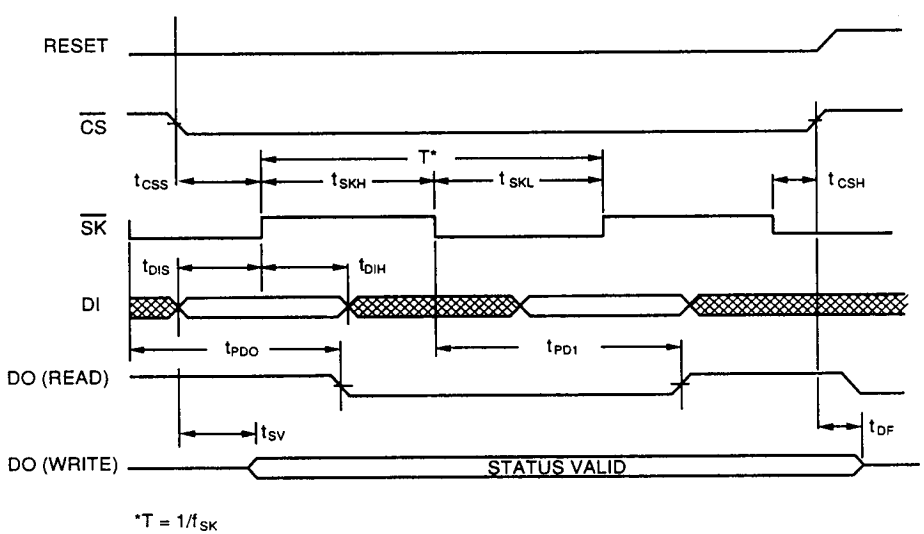


FIGURE 2. SYNCHRONOUS DATA TIMING

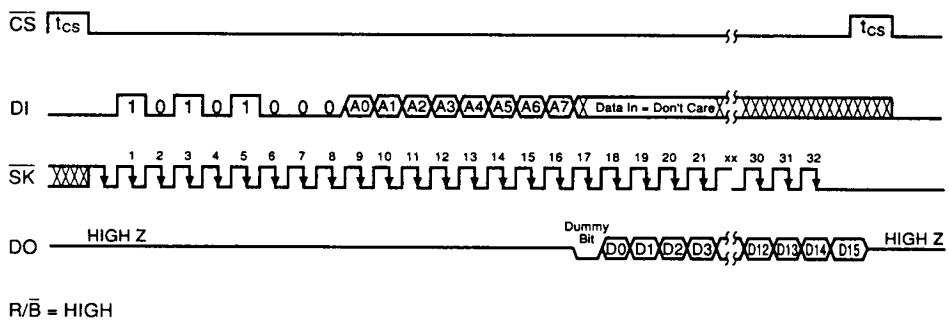


FIGURE 3. READ CYCLE TIMING

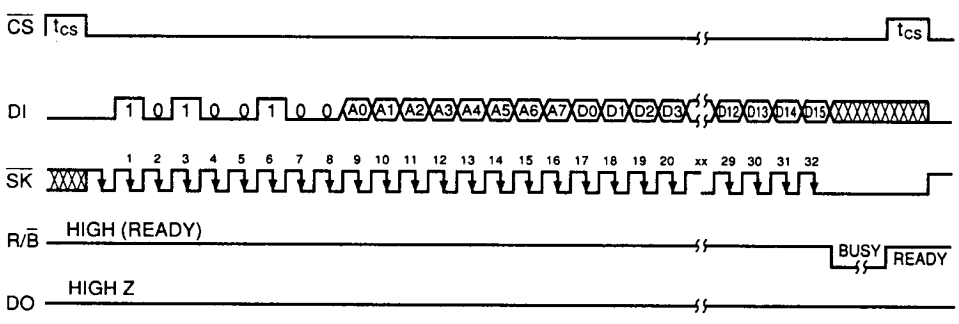


FIGURE 4. WRITE CYCLE TIMING

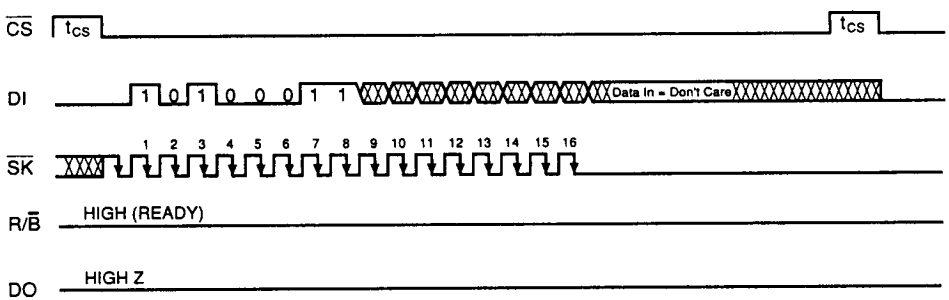


FIGURE 5. WRITE ENABLE (EWEN) CYCLE TIMING

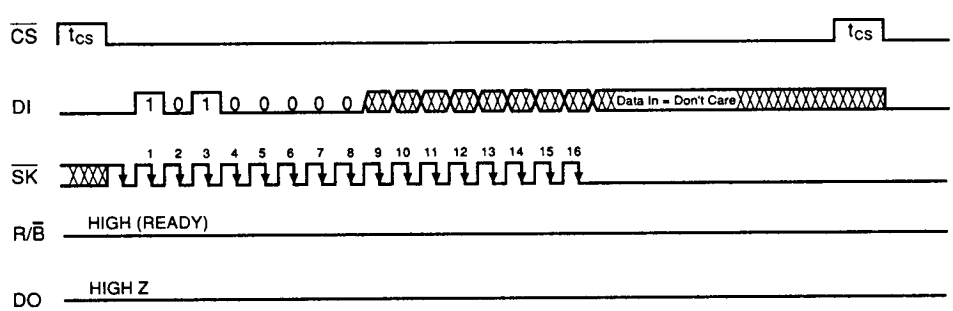


FIGURE 6. WRITE DISABLE (EWDS) CYCLE TIMING

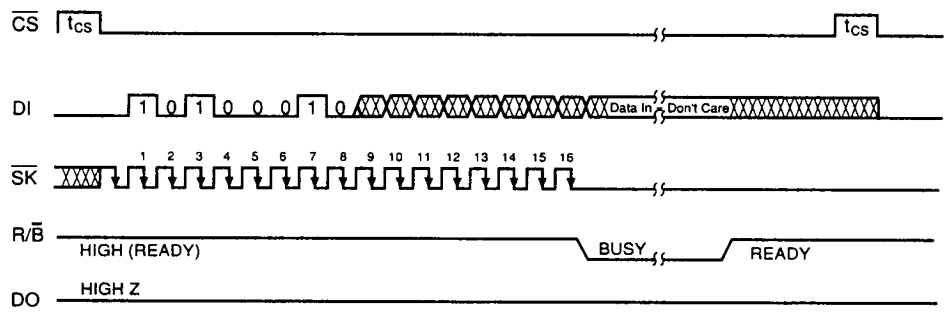


FIGURE 7. ERASE ALL (ERAL) CYCLE TIMING

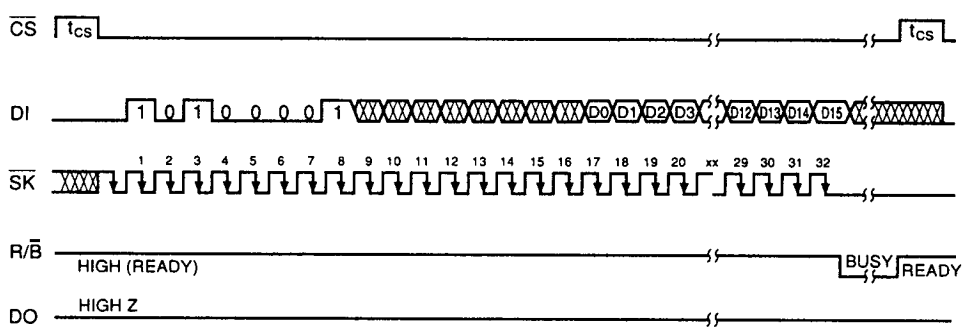


FIGURE 8. WRITE ALL (WRAL) CYCLE TIMING