Preliminary Information

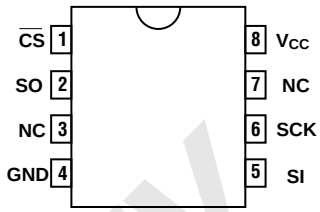
16K-bit SPI Nonvolatile Memory

FEATURES

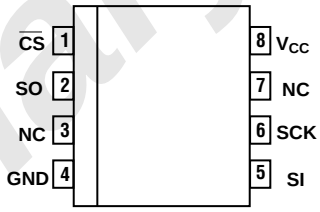
- **Motorola SPI (Modes 0 and 3) and SIOP Compatible**
- **2MHz Data Transfer Rate**
- **Low Power CMOS**
- **Active Current - Less than 3mA**
  - **— Standby Current @ 5.5V Vcc - 5µA**
  - **— Standby Current @ 1.8V Vcc - 1µA**
- **Direct Interface SPI Bus Configuration**
- **Early End of Write Detection**
  - **— Status Register Polling**
- **Software Controlled Inadvertent Write Protection**
- **High Reliability**
  - **— Endurance - 100,000 minimum write cycles**
  - **— Data Retention - Greater than 100 years**
- **Automatic Address Increment (Sequential Read)**
- **Extended (-40 to +85° C) and Automotive (-40 to +125° C) Temperature Ranges**
- **8-pin PDIP and 8-pin SOIC (JEDEC)**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



JEDEC Small Outline "Y" Package



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PIN NAMES

Pin	Pin Name	Function
1	$\overline{CS}$	Chip Select Input
2	SO	Serial Data Output
3	NC	Not Connected
4	Vss	Ground
5	SI	Serial Data Input
6	SCK	Serial Clock Input
7	NC	Not Connected
8	Vcc	Power Supply

OVERVIEW

The XL25161, a member of the SPI Lite™ memory family, is a low cost, low power CMOS serial nonvolatile memory which is fully compatible with the synchronous peripheral interface (SPI Bus) developed by Motorola. The XL25161 is fully operational from 1.8V to 5.5V over the full industrial temperature range of -40°C to +85°C. The XL25161 has been designed for full operation at 5V ±10% over an extended automotive temperature range of -40°C to +125°C.

The XL25161 is organized 2K x 8 and supports SPI operating modes 0,0 and 1,1. In addition it supports data transfer rates up to 2M-bits per second.

PIN DESCRIPTIONS

Serial Output (SO)

During a read cycle, data is shifted out on the SO pin. Data is clocked out by the falling edge of the serial clock.

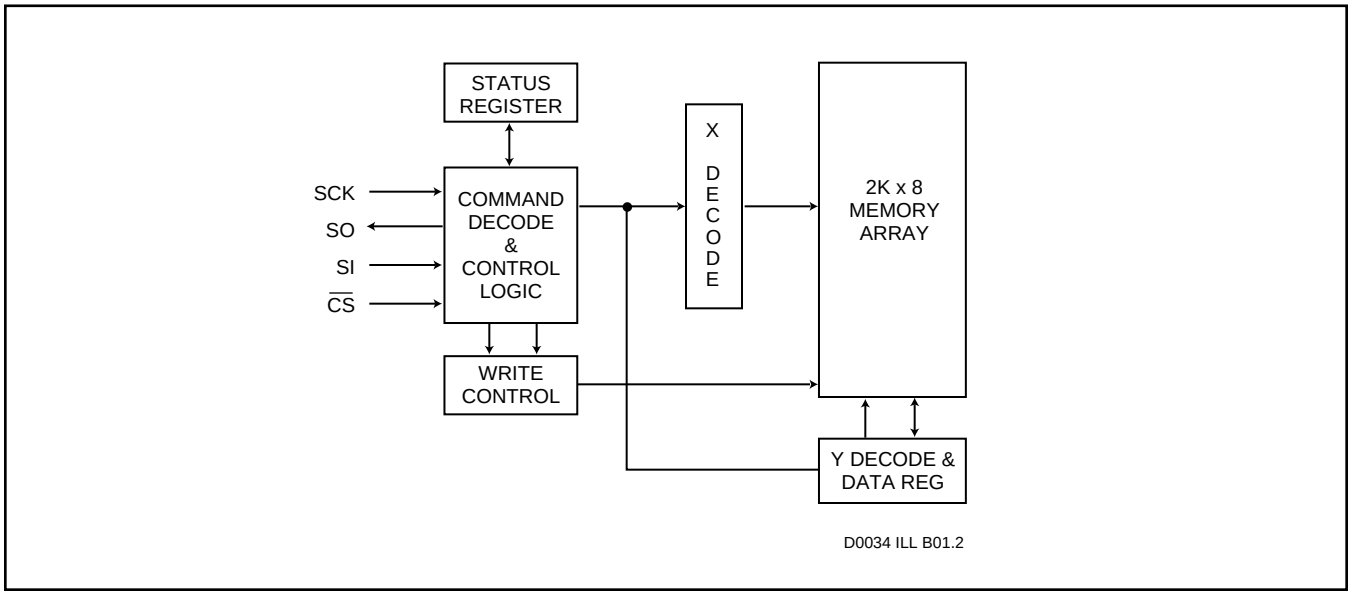
Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses or data present on the SI pin are latched on the rising edge of the clock while data on the SO pin change after the falling edge of the clock.

BLOCK DIAGRAM



Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the XL25161 is deselected and the SO pin is at high impedance and unless an internal write operation is underway, the XL25161 will be in the standby power mode. $\overline{CS}$ LOW enables the XL25161 and places the device in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

BASIC DEVICE OPERATION

The XL25161 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families. Because of the 8-bit data format employed the XL25161 can also be easily interfaced to a large number of microcontroller serial ports.

Each device has an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be low during the entire operation of clocking the instruction, address and subsequent data transfer. The following table contains a list of the instructions, their opcodes and a description of the operation.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. SCK is a static input and generally has no maximum duration either high or low; therefore, the user may stop the clock while servicing another interrupt.

Instruction	Instruction Format	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
READ	0000 0011	Read Data From Memory Array at Selected Address
WRITE	0000 0010	Write Data to Memory Array at Selected Address
NO-OP	0000 0001	Provides No-op in place of 25160 Write Status Register Instruction

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Write Enable (WREN) and Write Disable (WRDI)
The XL25161 contains a write enable latch. This latch must be **SET** before a nonvolatile write operation will be completed. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is automatically reset during power-on.

Read Status Register (RDSR)
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a nonvolatile write cycle. The Status register is formatted as follows:

7	6	5	4	3	2	1	0
1	1	1	1	1	1	WEL	WIP

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Bits 2 thru 7 are don't care and will be read as logic 1's.

The **Write-in-Process (WIP)** bit indicates whether the device is busy with a write operation. When set to a "1" a write is in progress when set to a "0" no write is in progress.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When read as a "1" the latch is set, when read as a "0" the latch is reset.

Clock and Data Timing
Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK

Read Sequence
The $\overline{CS}$ line is first pulled low to select the device. The 8-bit opcode is set to the device and followed by the address to be read. After the read opcode and address are sent, the data stored at the selected memory location will be shifted out on the SO line. The data stored at the next higher address location can be read sequentially by continuing to provide clock pulses. Internally the address is automatically incremented to the next higher address after each byte of data is shifted out on the SO pin. When the highest address is reach the address counter will roll over to address 000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Write Sequence
In order to write to the device the write enable latch must be set. The $\overline{CS}$ line is taken low and the 8-bit WREN instruction is clocked into the device. After the eighth clock $\overline{CS}$ must be returned high before issuing the WRITE opcode, address and data to be written.

Once the write enable latch is set, the user may proceed by issuing the write instruction, address and then the data to be written. This is a thirty-two clock operation, $\overline{CS}$ must go low and remain low for the entire thirty-two clocks and must be brought high before a thirty-third clock is detected.

[the write enable register will not be reset upon the completion of the write cycle]

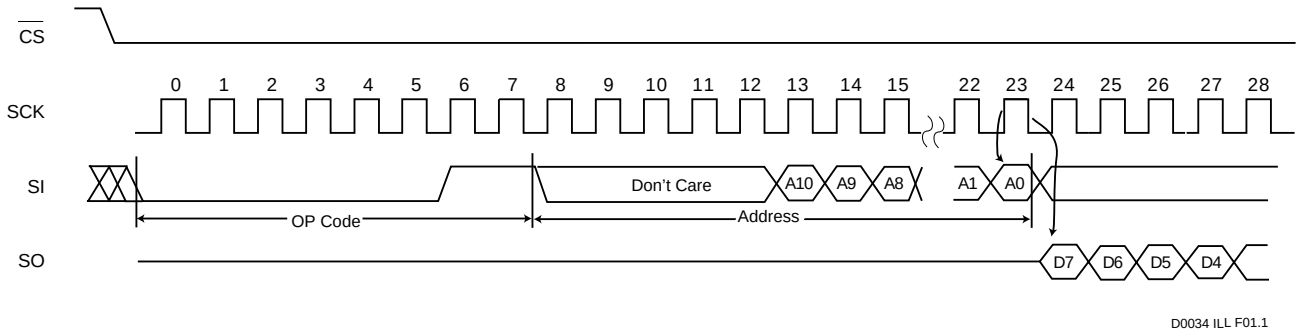

FIGURE 1. READ E²PROM ARRAY OPERATION SEQUENCE DETAIL

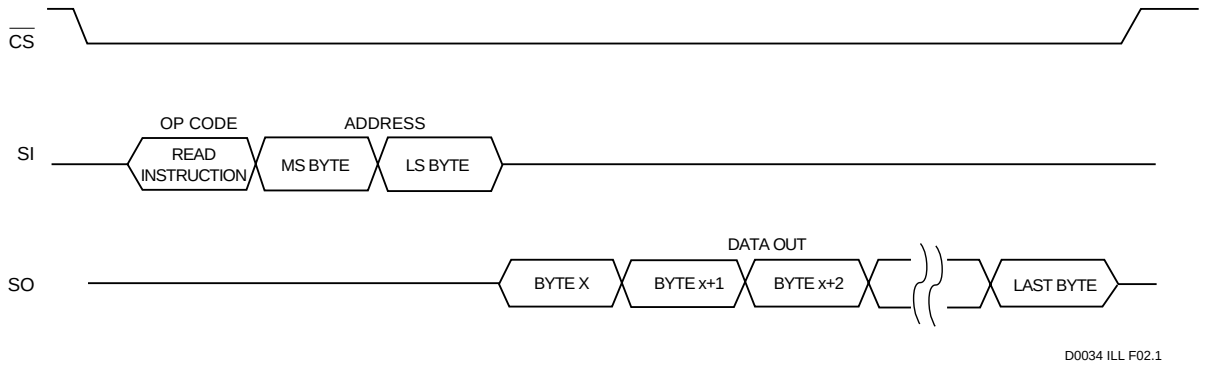

FIGURE 2. SEQUENTIAL READ SEQUENCE

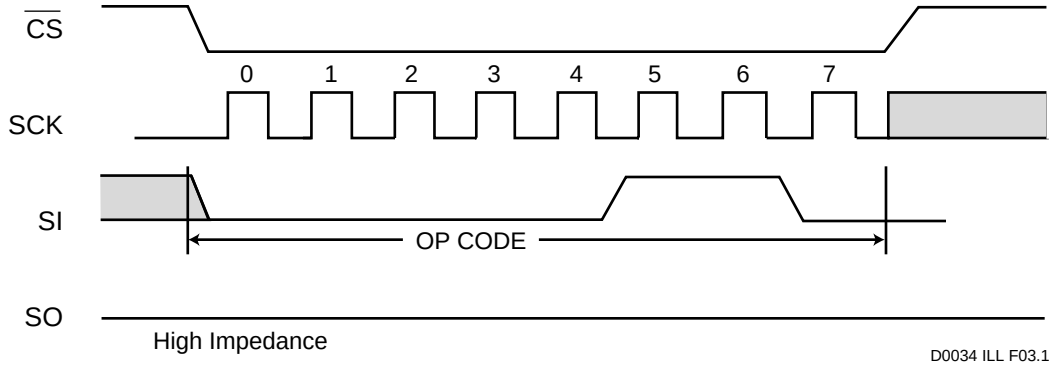

FIGURE 3. WRITE ENABLE SEQUENCE DETAIL (WREN INSTRUCTION)

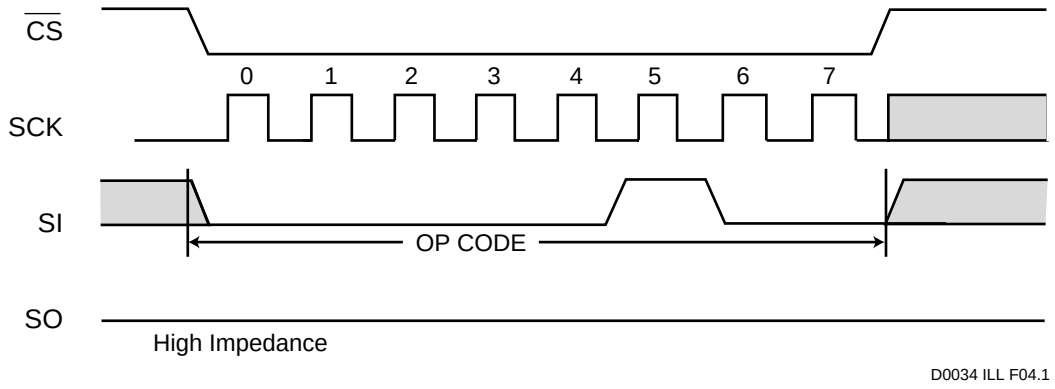

FIGURE 4. WRITE DISABLE SEQUENCE DETAIL

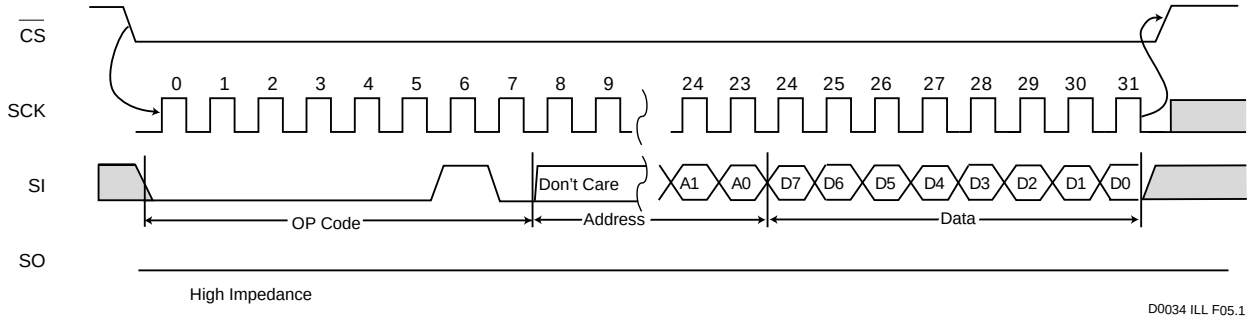

FIGURE 5. BYTE WRITE OPERATION SEQUENCE DETAIL

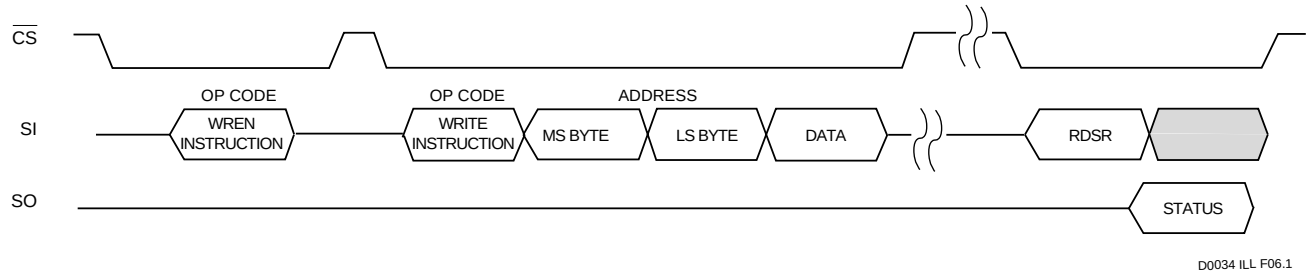

FIGURE 6. BYTE WRITE OPERATION

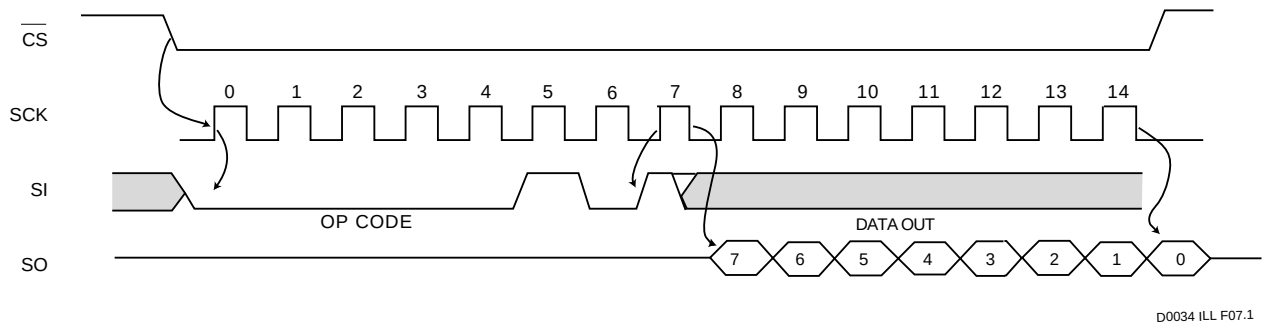

FIGURE 7. READ STATUS REGISTER SEQUENCE DETAIL

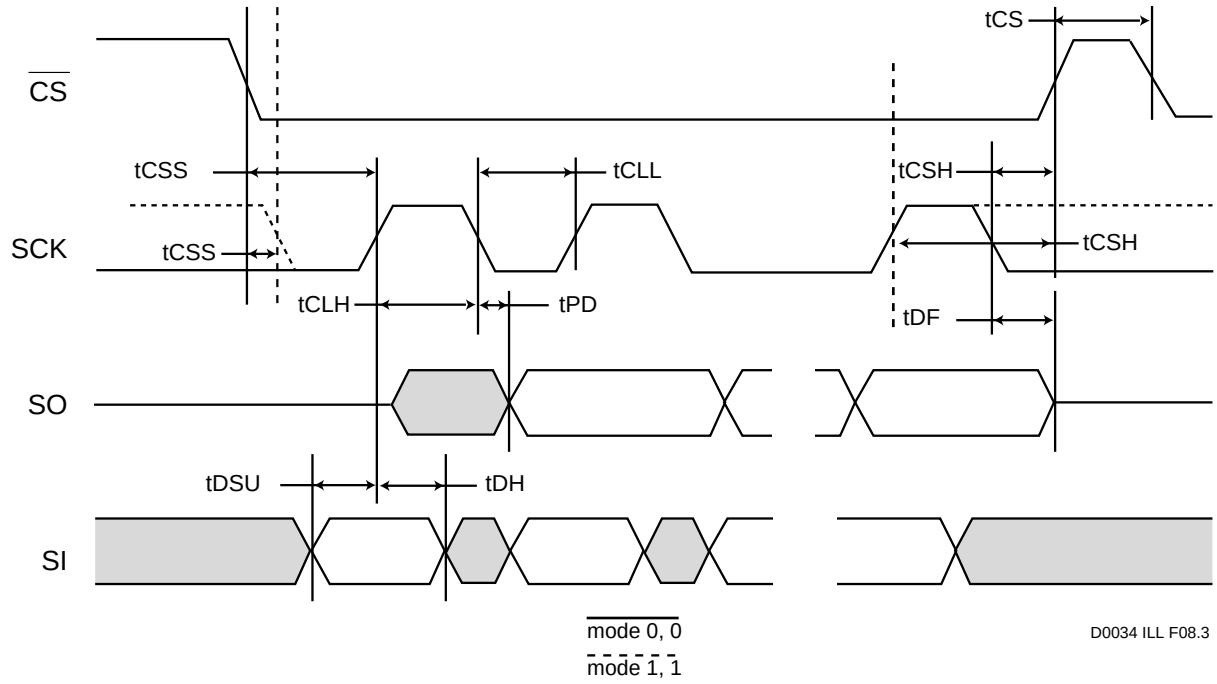

FIGURE 8. A.C. TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... -0.3 to 7.0V
Voltage on Any Pin. ..... -0.3 to Vcc +0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C, V_{CC} = 1.8V to 5.5V

Symbol	Parameter	Condition	Min	Max	Unit
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = 5.5V		3	mA
		$\overline{CS}$ = V_{IL}, V_{CC} = 1.8V		2	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{CC} = 5.5V		5	µA
		$\overline{CS}$ = V_{CC} = 1.8V		1	µA
I_{IL}	Input Leakage Current	V_{IN} + 0V to V_{CC}	-1	1	
I_{OL}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-1	1	
V_{IL}	Input Low Voltage		-0.3	0.3xV_{CC}	V
V_{IH}	Input High Voltage		0.7xV_{CC}	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, V_{CC} = 5.5V		0.4	V
		I_{OL} = 10µA, V_{CC}= 1.8V		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -400µA, V_{CC} = 5.5V	2.4		V
		I_{OH} = -10µA, V_{CC} = 1.8V	V_{CC}-0.2		V

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TA = -40°C to +125°C, V_{CC} = 5V+10%

Symbol	Parameter	Condition	Min	Max	Unit
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = 5.5V		3	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5V		200	µA
I_{IL}	Input Leakage Current	V_{IN} + 0V to V_{CC}	-1	1	
I_{OL}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-1	1	
V_{IL}	Input Low Voltage		-0.3	0.3xV_{CC}	V
V_{IH}	Input High Voltage		0.7xV_{CC}	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	V_{OL} = 2.1mA, V_{CC} = 5.5V		0.4	V
V_{OH}	Output High Voltage	V_{OH} = -400µA, V_{CC} = 5.5V	2.4		V

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POWER-UP TIMING

Symbol	Parameter	Condition	Min	Max	Unit
tPUR [2]	Power-up to Read Operation			1	ms
tPUW [2]	Power-up to Write Operation			5	ms

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CAPACITANCE

TA = +25°C, f=1MHz, V_{CC}=5V

Symbol	Parameter	Max	Units	Conditions
C_{OUT} [1]	Output Capacitance (SO)	8	pF	V_{OUT}=0V
C_{IN} [1]	Input Capacitance (SI, SCK, $\overline{CS}$)	6	pF	V_{IN}=0V

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1 This parameter is periodically sampled and 100% tested
2 tPUR and tPUW are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These functions are initially characterized and are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C, V_{CC} = 1.8V to 5.5V
TA = -40°C to +125°C, V_{CC} = 5V+10%

Symbol	Parameter	Condition	Min	Max	Units
f_{SCK}	SCK Clock Frequency	TA = -40°C to +85°C	0	2	Mhz
		TA = -40°C to +125°C	0	1	Mhz
t_{CLH}	SCK Clock High Time	TA = -40°C to +85°C	240		ns
		TA = -40°C to +125°C	400		ns
t_{CLL}	SCK Clock Low Time	TA = -40°C to +85°C	240		ns
		TA = -40°C to +125°C	400		ns
t_{CSS}	Chip Select Setup Time	TA = -40°C to +85°C	240		ns
		TA = -40°C to +125°C	500		ns
t_{CSH}	Chip Select Hold Time	TA = -40°C to +85°C	240		ns
		TA = -40°C to +125°C	500		ns
t_{CS}	CS Deselect Time	TA = -40°C to +85°C	250		ns
		TA = -40°C to +125°C	500		ns
t_{PD}	Output Delay	TA = -40°C to +85°C		240	ns
		TA = -40°C to +125°C		360	ns
t_{DSU}	Data In Setup Time	TA = -40°C to +85°C	100		ns
		TA = -40°C to +125°C	100		ns
t_{DH}	Data In Hold Time	TA = -40°C to +85°C	100		ns
		TA = -40°C to +125°C	100		ns
t_{DF}	Output Disable Time	TA = -40°C to +85°C		240	ns
		TA = -40°C to +125°C		500	ns
t_{WP}	Write Cycle Time	TA = -40°C to +85°C		5	ms
		TA = -40°C to +125°C		5	ms

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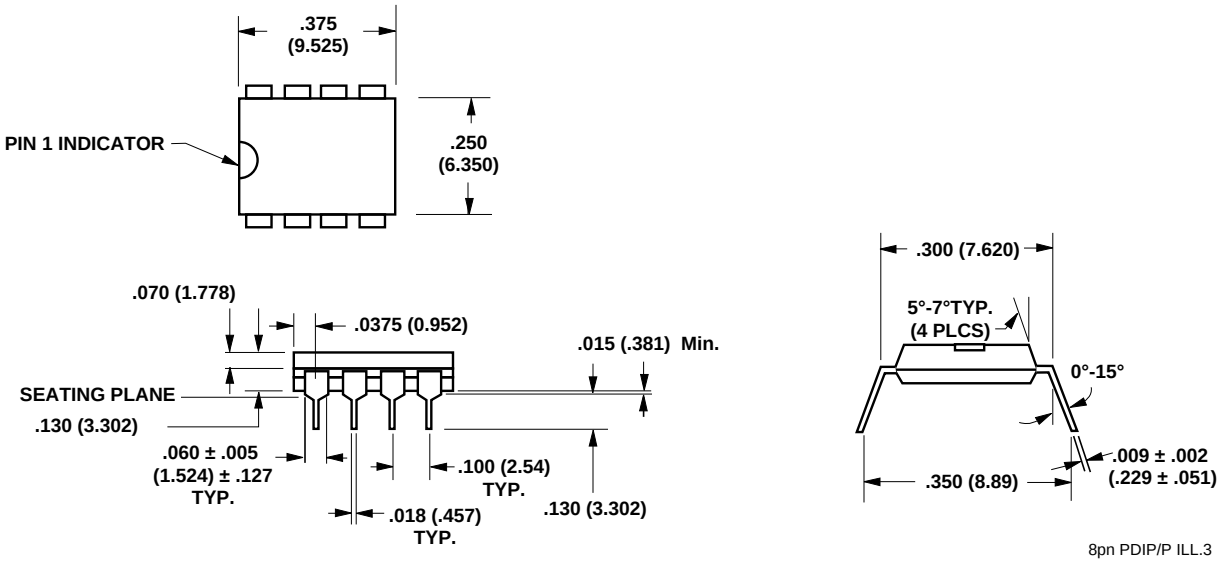
PACKAGE DIAGRAMS

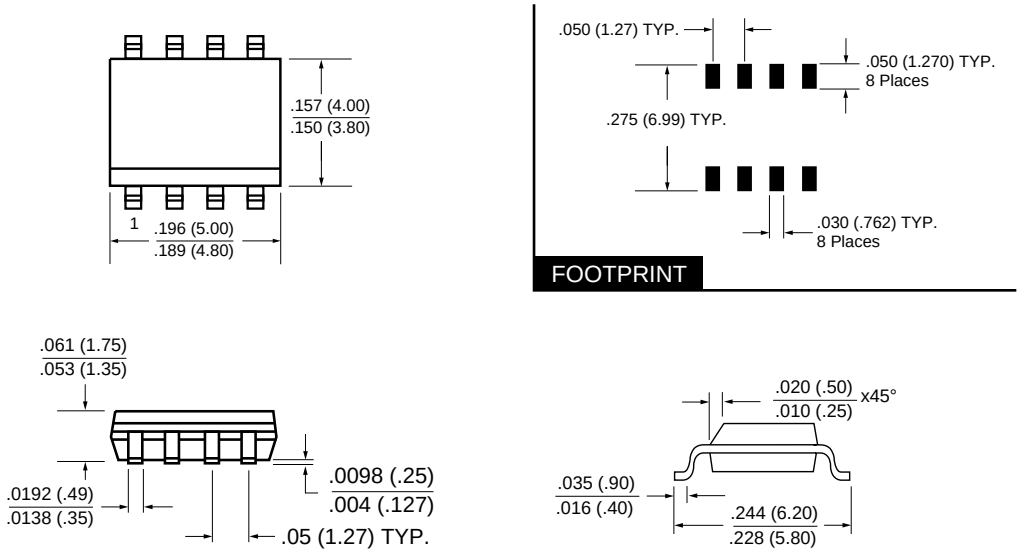
Plastic Dual-in-line (Type "P") Package (PDIP)



8pn PDIP/P ILL.3

ALL DIMENSIONS IN INCHES (MM).

8 Pin SOIC (Type "Y") Package JEDEC 150 mil body width*



8pn JEDEC SOIC ILL.1

ALL DIMENSIONS IN INCHES (MM).

* See cover page for pinout options.

ORDERING INFORMATION

Standard Configurations

Prefix	Part Type	Package Type
XL	25161	P, Y

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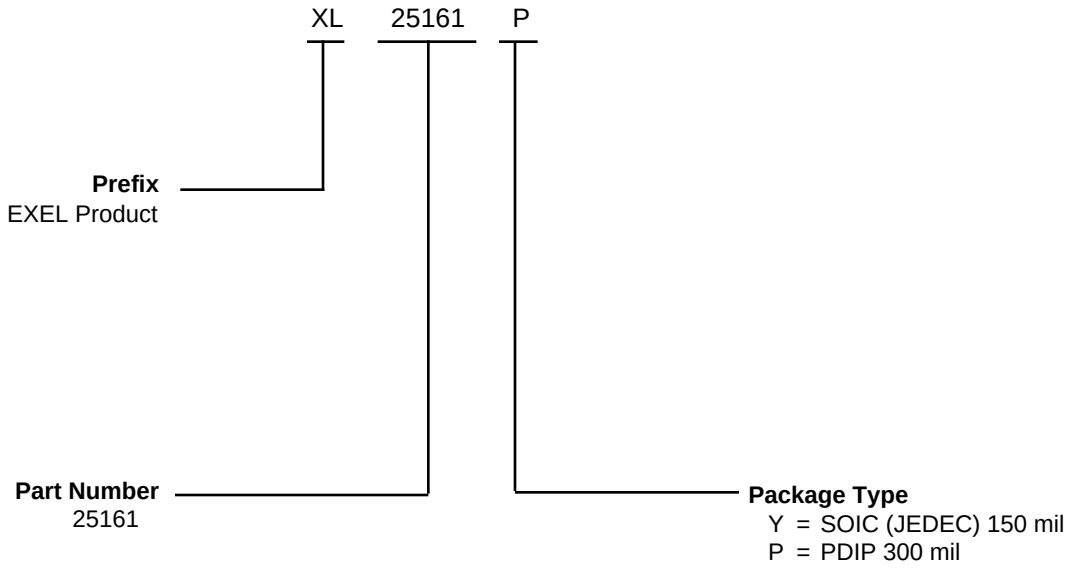
Part Numbers:

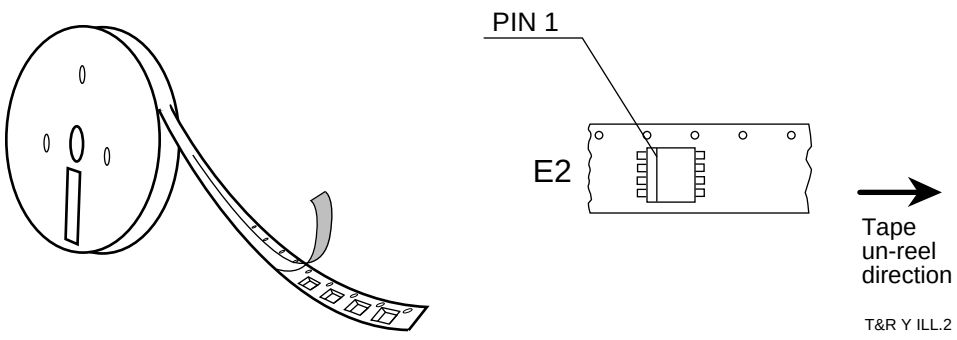


MARKING INFORMATION

* See cover page for pinout options.

TAPE AND REEL (EMBOSSED) INFORMATION

Surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The following diagram provides general information regarding the direction of the IC's. Tape "E2" shall be designated with PIN 1 at the trail direction.



Quantity per reel: 2,500 SOIC parts.

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