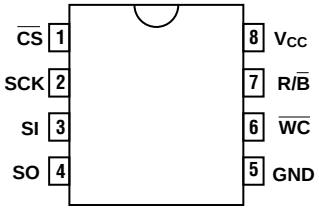
2,048-Bit Serial Electrically Erasable PROM
Synchronous Peripheral Interface
2.7 to 5.5 Volt Operation

FEATURES

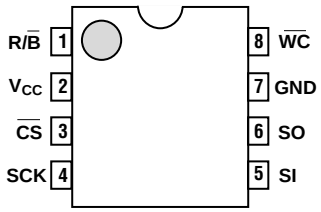
- **Motorola SPI (Modes 0 and 3) and SIOP Compatible**
- **1 MHz Clock Rate**
- **Extended Temperature Range: -40°C to +85°C**
- **Low Power Consumption**
  - **— Active current 500μA**
  - **— Standby current 2μA**
- **2.7 to 5.5 volt operation (both READ and WRITE)**
- **Hardware & Software Write Protection**
  - **— Defaults to disabled state at power up**
  - **— Software instructions for WRITE-enable/ disable**
- **Internally Organized as 128 x 16 bits**
- **Easy-to-Use Interface**
  - **— READY/$\overline{\text{BUSY}}$ status signal**
  - **— Automatic write cycle time-out**
- **High Reliability**
  - **— Endurance: 100,000 erase/write cycles**
  - **— Data retention: 100 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



EIAJ Small Outline "F" Package



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PIN NAMES

$\overline{\text{CS}}$	Chip Select Input
SCK	Serial Clock Input
SI	Serial Input
SO	Serial Output
GND	Ground
$\overline{\text{WC}}$	Write Control Input
R/$\overline{\text{B}}$	READY/$\overline{\text{BUSY}}$ Output
Vcc	Power Supply

OVERVIEW

The XL25026, a member of the SPI Lite™ memory family, is a cost effective 2,048-bit, nonvolatile, serial E^2PROM designed to directly interface with the Motorola SIOP and SPI ports. The XL25026 provides external read/write memory arranged as 128 registers of 16 bits each. Four 8-bit instructions control the operation of the device, which include read, write, write enable and write disable. The READY/$\overline{\text{BUSY}}$ pin indicates the status of the device when polled during the WRITE operation. The serial data output pin (SO) also indicates the status of the device during the self-timed nonvolatile programming cycle. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. After the initiation of the write cycle, if Chip Select ($\overline{\text{CS}}$) is brought LOW, while SCK is low, the SO pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

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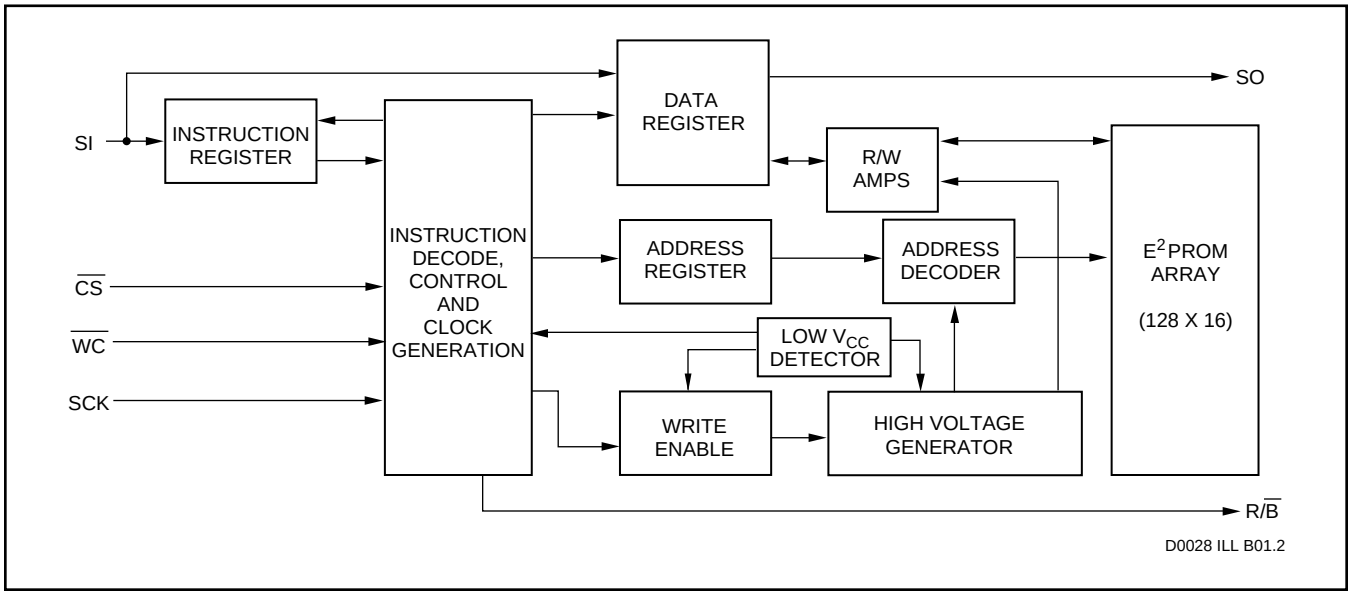
BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL25026 is designed for applications requiring up to 100,000 erase/write cycles. It provides 100 years of secure data retention, with or without power applied.

DEVICE OPERATION

The XL25026 is a synchronous serial port compatible E²PROM. It operates on a single power supply ranging from 2.7V to 5.5V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Input data is latched on the rising edge of the clock (SCK), and data is output on the falling edge of the clock.

Data is grouped in 8-bit bytes. The beginning 8 bits specify the mode, the next 8 bits specify the address, and subsequent 16 bits specify the I/O data. Each instruction sent to the device includes a 4 bit start sequence, 1010, a 4 bit opcode and a 7-bit address including one dummy bit at the end. For a WRITE operation, a 16 bit data field is required following the 8 bit address field. The device requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the 4 bit start sequence is given. Prior to the 4 bit start sequence (1010), inputs of all other logical sequence are ignored.

During the self-timed internal programming cycle that accompanies a write, the SCK clock is deactivated. It is needed only when instructions or data are being passed to or from the memory.

Any of the four modes (read, write, write enable, write disable) may be specified. The write time is set by an internal timer, and determination of whether a write operation is in progress or not can be made from the status of the READY/$\overline{BUSY}$ pin.

Read (READ)

The read instruction is the only instruction that outputs serial data on the SO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into the output register. The output on SO changes during the HIGH to LOW transition of SCK.

Write (WRITE)

After a write instruction and its address have been decoded, the device expects 16 bits of data. These are to be transferred into the specific memory register which has previously been automatically erased. After the last data bit has been clocked into SI on the 32nd clock edge, the self-timed internal programming cycle is initiated. The write cycle status can be monitored by observing the READY/$\overline{BUSY}$ pin. It will output the $\overline{BUSY}$ status (LOW) within 1µs after the rising edge of the 32nd clock (the last

data bit) and will stay LOW until the WRITE cycle is complete. It will then output a HIGH status until the next WRITE cycle is initiated. $\overline{CS}$ must be held HIGH for the minimum of t_{CS} before the next instruction is entered.

Another way to get READY/$\overline{BUSY}$ status is from the SO pin. During a WRITE cycle, asserting a LOW on the $\overline{CS}$ pin will cause the SO pin to output the READY/$\overline{BUSY}$ status. It is necessary for SCK to be brought into a LOW state 500ns prior to $\overline{CS}$ going LOW. Asserting a HIGH on $\overline{CS}$ will put the SO pin in a high impedance state again. After the WRITE cycle is completed, the SO pin will output HIGH when the device is deselected. The first rising edge of the SI pin will reset SO back into the high impedance state.

Write Control ($\overline{WC}$ PIN)

The $\overline{WC}$ pin provides hardware write control. When $\overline{WC}$ pin is low, the chip is enabled to execute WRITE functions. When $\overline{WC}$ pin is high, all WRITE functions are locked out. The device shows ready status on the R/$\overline{B}$ pin and on the SO pin, if $\overline{CS}$ and SCK are low. In addition, if $\overline{WC}$ pin changes state during the write cycle, the write operation will be aborted not guaranteeing the data. The $\overline{WC}$ pin does not have any effect on the READ, WREN and WRDI operations.

Write Enable/Disable

When the XL25026 is powered up, it comes up in the write disabled state. In order to be programmable, it must receive an enable instruction. The device remains programmable until a disable instruction is entered, or until it is powered down. The disable instruction provides protection against inadvertent writes. Read operation is not affected by this command.

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address Data	Input
READ	1010	1000	(A_6-A_0) 0	
WRITE	1010	0100	(A_6-A_0) 0	D_{15}-D_0
Write Enable (WREN)	1010	0011	XXXXXXXX	
Write Disable (WRDI)	1010	0000	XXXXXXXX	

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ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -40°C to +85°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... -0.3 to 7.0V
Voltage on Any Pin. ..... -0.3 to V_{CC} +0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 2.7 to 5.5 Volts

Symbol	Parameter	Conditions	V_{CC} = 3.0V±10%		V_{CC} = 5.0V±10%		Units
			Min.	Max.	Min.	Max.	
I_{CC1}	Operating Current – CMOS	$\overline{CS}$ = V_{CC} , SCK = 1MHz		0.5		1	mA
I_{CC2}	Operating Current – TTL	$\overline{CS}$ = V_{IH} , SCK = 1MHz		1.5		3	mA
I_{SB}	Standby Current	$\overline{CS}$ = DI = SCK = 0V		2		3	µA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC} ($\overline{CS}$, SCK, SI)		1		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC} , $\overline{CS}$ = 0V		1		1	µA
V_{IL1}	Input Low Voltage	SI Pin		0.3xV_{CC}		0.3xV_{CC}	V
V_{IH1}	Input High Voltage	SI Pin	0.7xV_{CC}		0.7xV_{CC}		V
V_{IL2}	Input Low Voltage	$\overline{CS}$, SCK, $\overline{WC}$ Pin		0.2xV_{CC}		0.2xV_{CC}	V
V_{IH2}	Input High Voltage	$\overline{CS}$, SCK, $\overline{WC}$ Pin	0.8xV_{CC}		0.8xV_{CC}		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA TTL			0	0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA TTL			2.4	V_{CC}	V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10 µA CMOS	$V_{CC}^{-0.2}$		$V_{CC}^{-0.2}$		V

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AC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 2.7 to 5.5 Volts

Symbol	Parameter	Conditions	V_{CC} = 3.0V±10%		V_{CC} = 5.0V±10%		Units
			Min.	Max.	Min.	Max.	
f_{SCK}	SCK Clock Frequency			1		1	MHz
t_{WH}	SCK HIGH Time		450		450		ns
t_{WL}	SCK LOW Time		450		450		ns
t_{CS}	Minimum $\overline{CS}$ HIGH Time		1000		1000		ns
t_{CSS}	$\overline{CS}$ Setup Time	Relative to SCK	200		200		ns
t_{SU}	SI Setup Time	Relative to SCK	150		150		ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to SCK	0		0		ns
t_H	SI Hold Time	Relative to SCK	150		150		ns
t_{PD1}	Output Delay to “1”	AC Test		350		350	ns
t_{PD0}	Output Delay to “0”	AC Test		350		350	ns
t_{SV}	$\overline{CS}$ to Status Valid	AC Test		1000		1000	ns
t_{OH}	$\overline{CS}$ to SO in 3-state	$\overline{CS}$ Hi to SO Hi-z	0	400	0	400	ns
$t_{E/W}$	Write Cycle Time			15		10	ms
t_{WCS}	Write Control Setup Time	Relative to $\overline{CS}$	0		0		ns
t_{WCH}	Write Control Hold TIme	Relative to $\overline{CS}$	0		0		ns

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CAPACITANCE

T_A = 25°C, f = 1MHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

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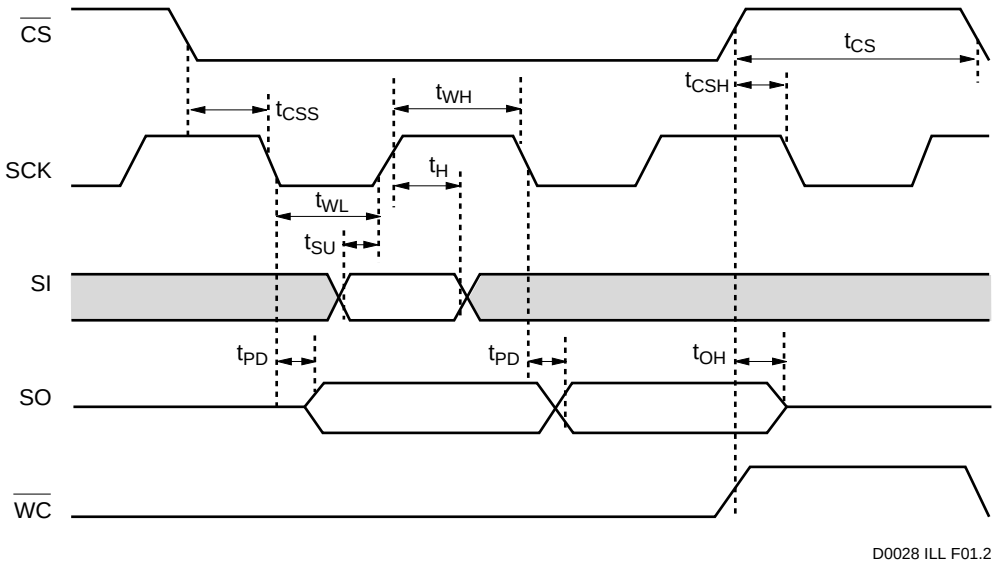

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FIGURE 1. SYNCHRONOUS DATA TIMING

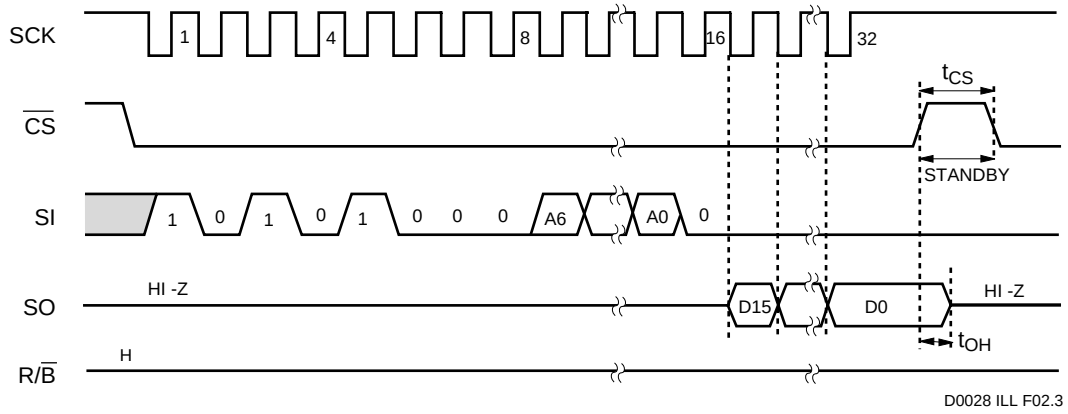


FIGURE 2. READ CYCLE TIMING

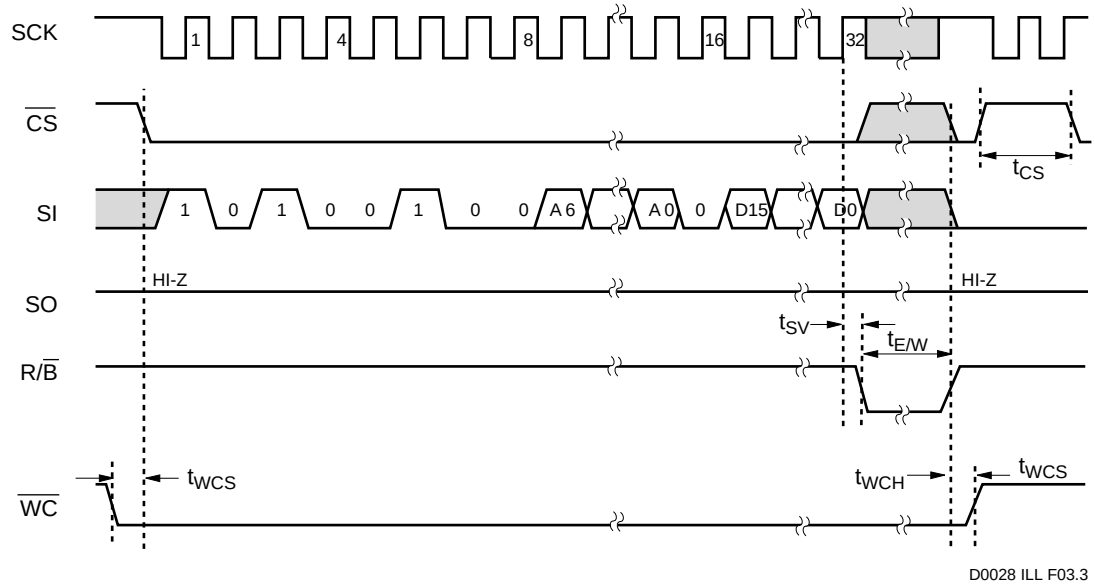


FIGURE 3. WRITE CYCLE TIMING

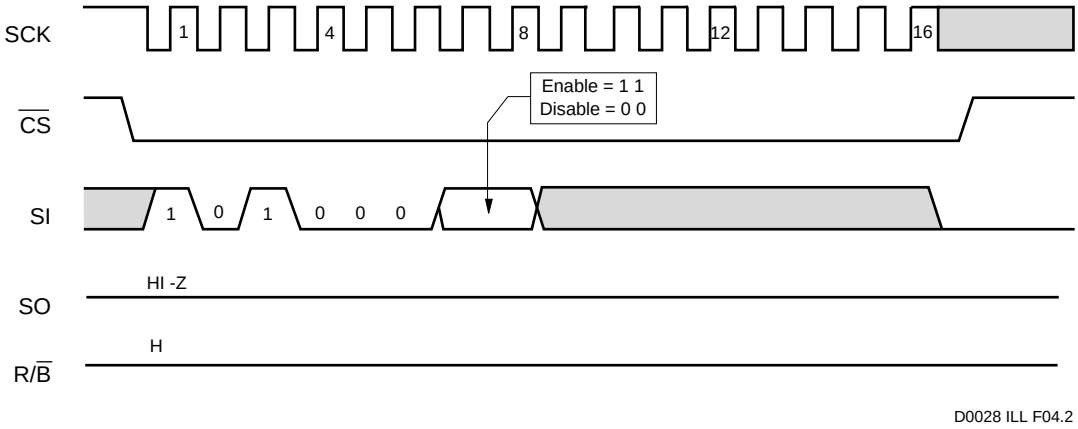


FIGURE 4. ERASE/WRITE ENABLE AND DISABLE CYCLE TIMING

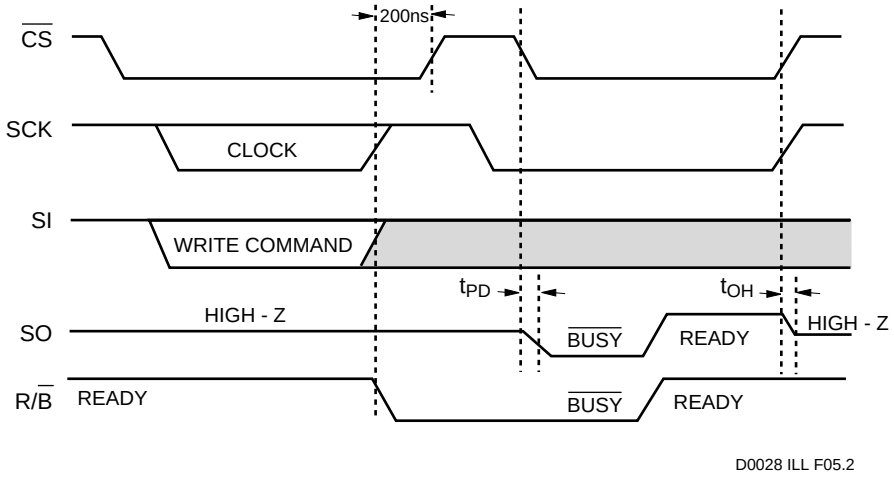
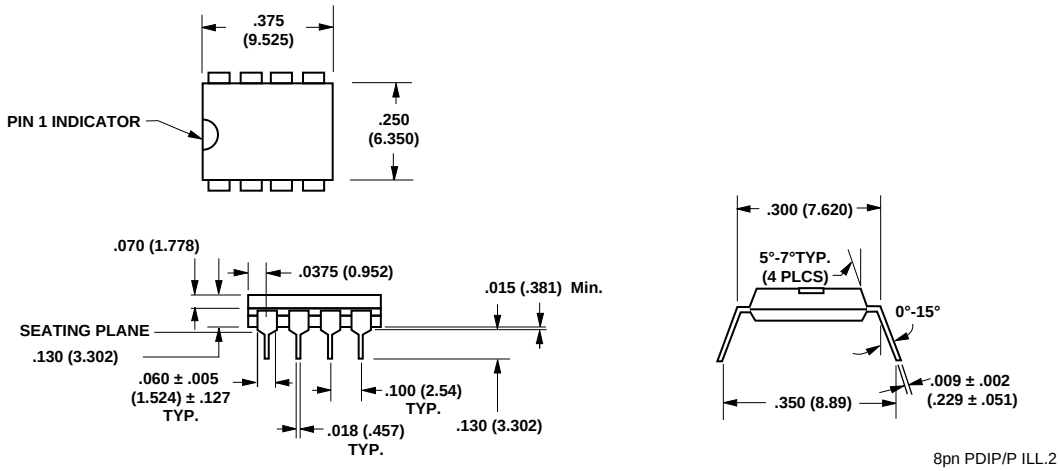


FIGURE 5. READY/BUSY STATUS OUTPUT TIMING

PACKAGE DIAGRAMS

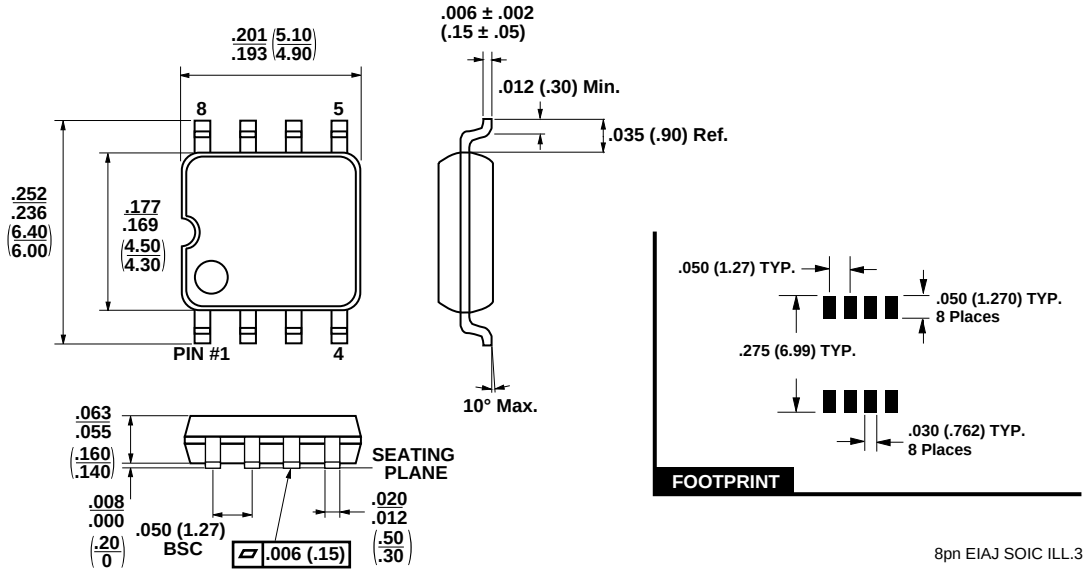
Plastic Dual-in-line (Type “P”) Package (PDIP)



8pn PDIP/P ILL.2

ALL DIMENSIONS IN INCHES (MM).

8 pin SOIC (Type “F”) Package EIAJ (175 mil Body Width)



8pn EIAJ SOIC ILL.3

ALL DIMENSIONS IN INCHES (MM).

* See cover page for pinout options.

ORDERING INFORMATION

Standard Configurations

Prefix	Part Type	Package Type
XL	25026	P, F

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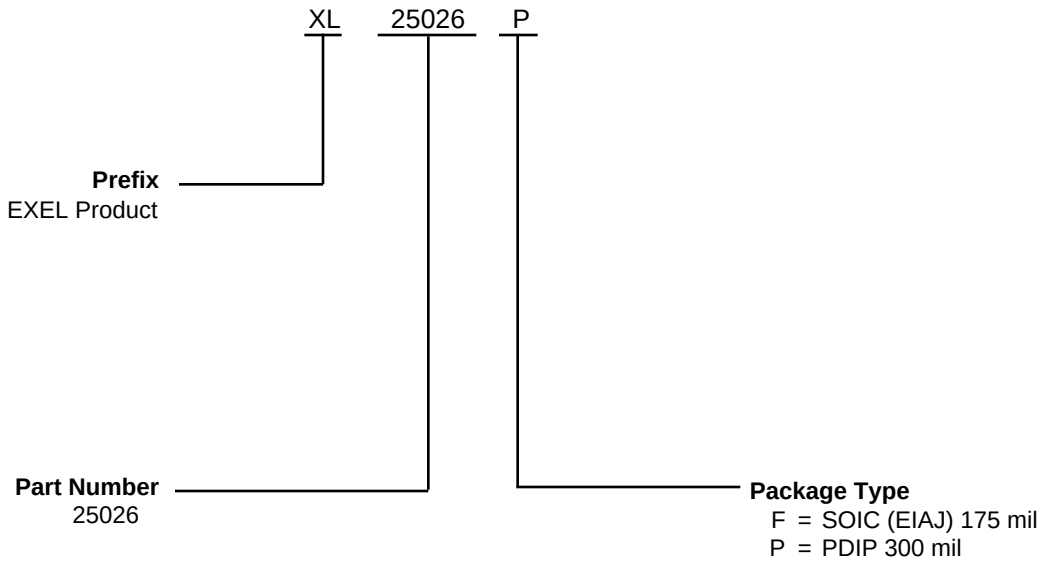
Part Numbers:

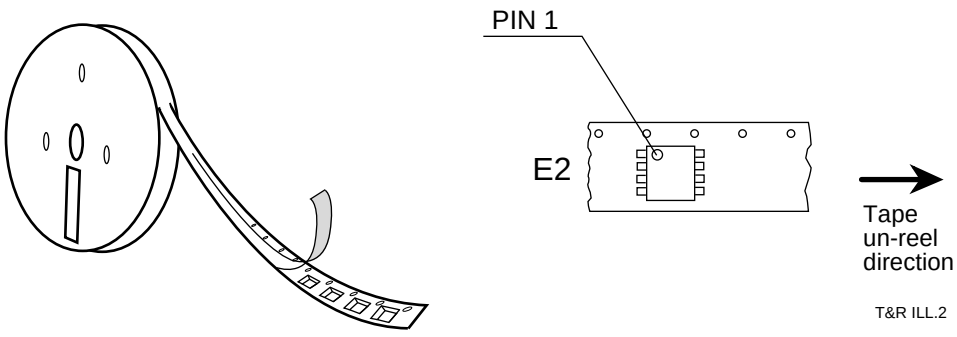


MARKING INFORMATION

* See cover page for pinout options.

TAPE AND REEL (EMBOSSED) INFORMATION

Surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The following diagram provides general information regarding the direction of the IC's. Tape "E2" shall be designated with PIN 1 at the trail direction.



Quantity per reel: 2,500 SOIC parts.

NOTES:

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