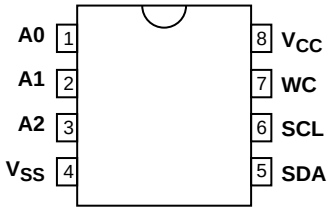
1,024-Bit Serial Electrically Erasable PROM
2.7 To 5.5 Volt Operation

FEATURES

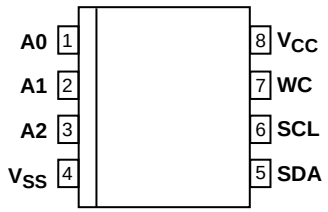
- **Low Power CMOS**
  - **— Active current less than 2mA**
  - **— Standby current less than 2μA**
- **Hardware Write Protection**
  - **— Write Control pin**
- **2.7V to 5.5V Operation**
- **Extended Temperature Range: -40°C to +85°C**
- **Internally Organized as 128 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **— Bidirectional data transfer protocol**
- **Four-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
- **High Reliability**
  - **— Endurance: 100,000 erase/write cycles**
  - **— Data retention: 100 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



JEDEC Small Outline
"Y" Package



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PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

OVERVIEW

The XL24C01A is a cost effective 1,024-bit serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. This part operates from a single supply over the range of 2.7 to 5.5 volts.

The XL24C01A is internally organized as a 128 x 8 memory bank. It features a I^2C serial interface and software protocol allowing operation on a simple two-wire bus. Up to eight XL24C01A s may be connected to the 2-wire bus by establishing their device address using the address input pins (A0, A1 and A2).

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

Address (A0, A1 and A2) - The address inputs are used to set the three bit device address of the XL24C01A which will identify it on the two-wire bus. These inputs may be tied HIGH or LOW, or they may be actively driven. These inputs allow up to eight XL24C01A devices to be distinguished on the bus.

Write Control (WC) - The Write Control input pin is used to disable write circuitry to the memory. When HIGH, the write function is disabled, protecting previously written data; when LOW, the write function is enabled.

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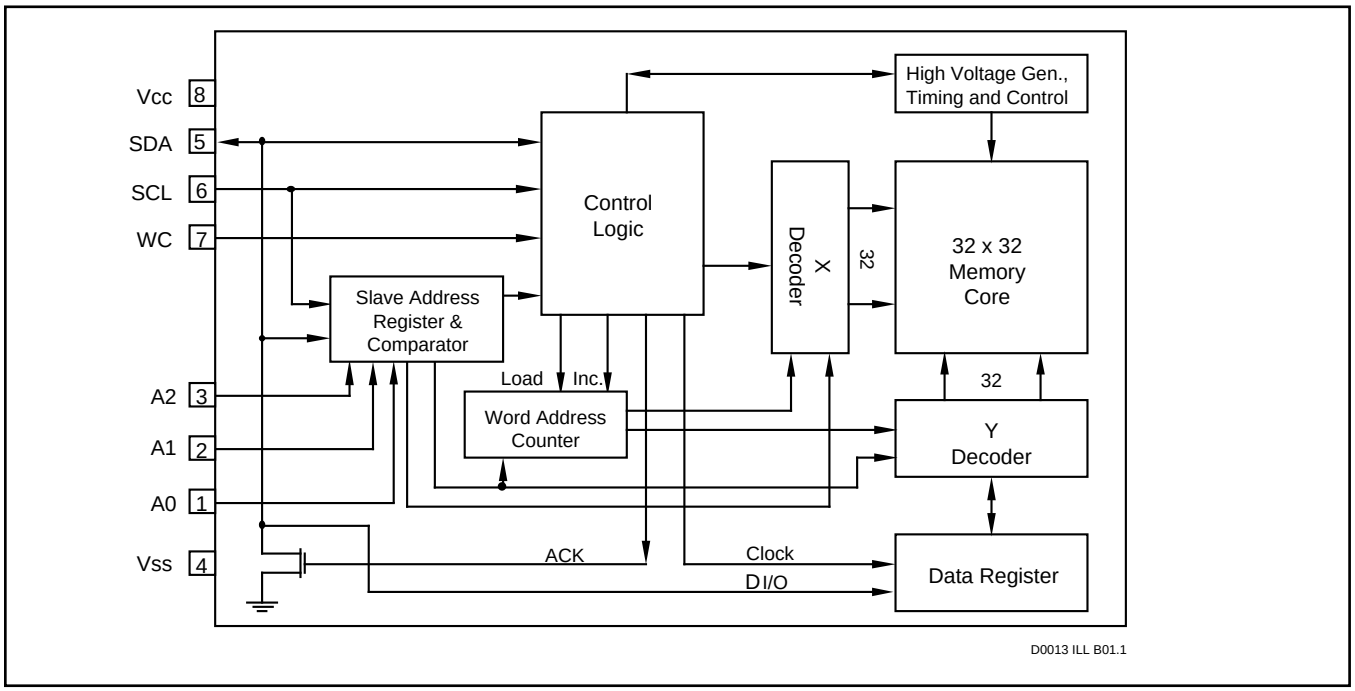
BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL24C01A is designed for applications requiring up to 100,000 write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C01A is ideal for high volume applications requiring low power and low density storage. This device uses a cost effective, space-saving 8-pin plastic package. Typical applications include robotics, alarm devices, electronic locks, meters and instrumentation.

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication for different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the clock HIGH time, because changes on the data line, while SCL is HIGH will be interpreted as “START” or “STOP” condition (See Figure 2).

START and STOP Conditions

When both data and clock lines are HIGH, the bus is known as “not busy.” A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the “START” condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the “STOP” condition (See Figure 3).

DEVICE OPERATION

The XL24C01A is a 1,024-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a “transmitter” and the receiving device as the “receiver.” The device controlling the data transmission is the “master” and the controlled device is the “slave.” In all cases, the XL24C01A will be a “slave” device, since it never initiates any data transfers.

Up to eight XL24C01As can be connected to the bus, selected by the A0, A1 and A2 device addresses. A0, A1 and A2 must be connected to either V_{CC}, V_{SS} or they may be actively driven. A0, A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

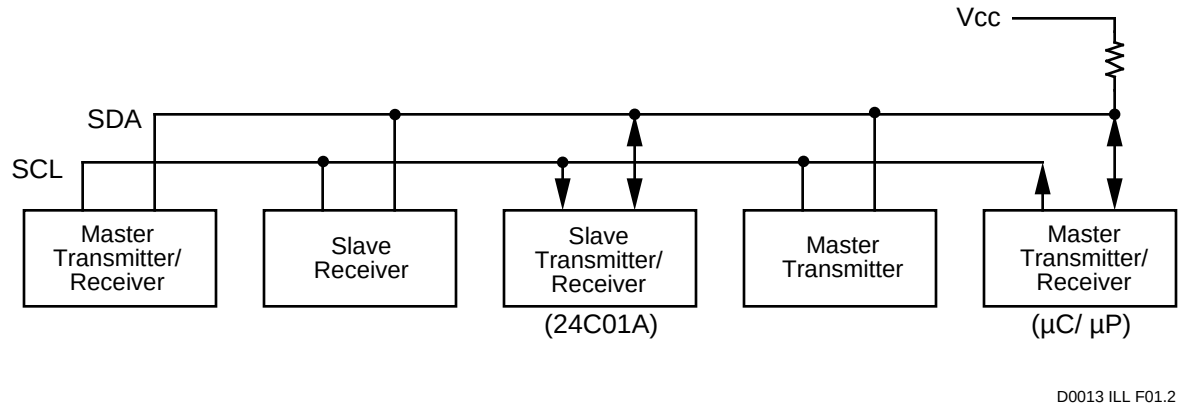


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

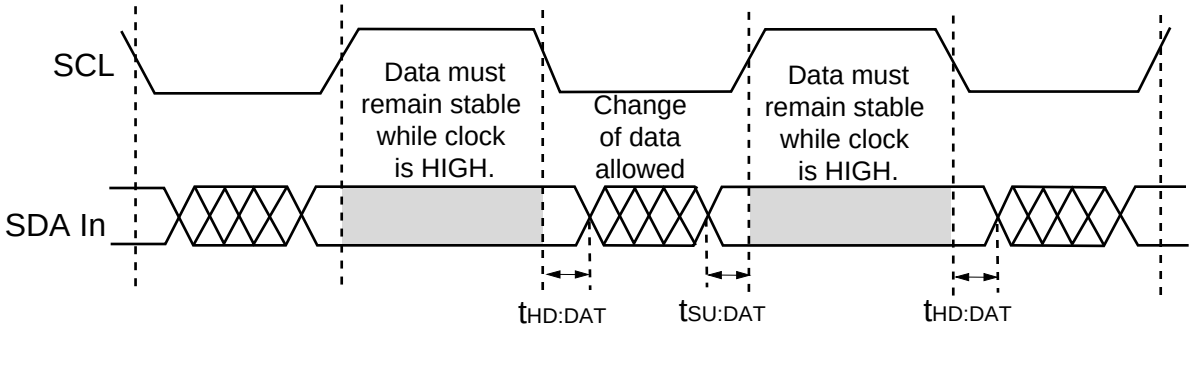


FIGURE 2. INPUT DATA PROTOCOL

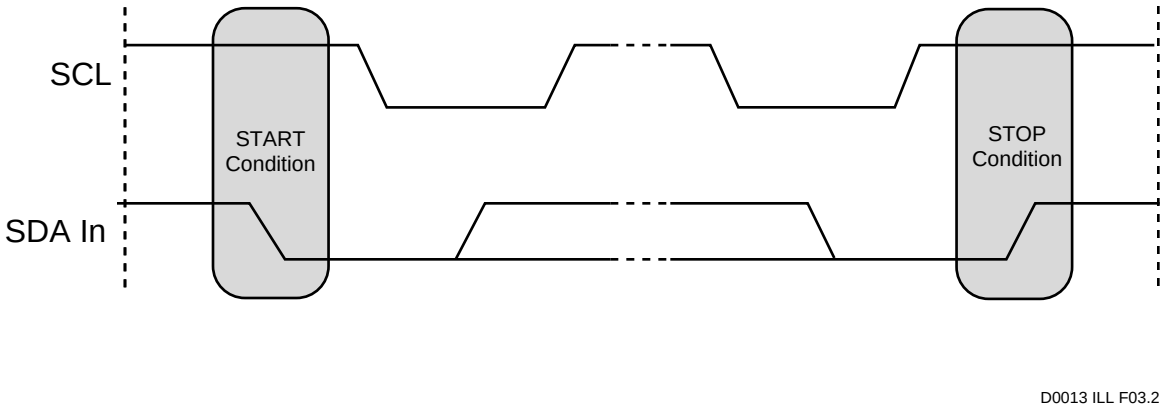


FIGURE 3. START AND STOP CONDITIONS

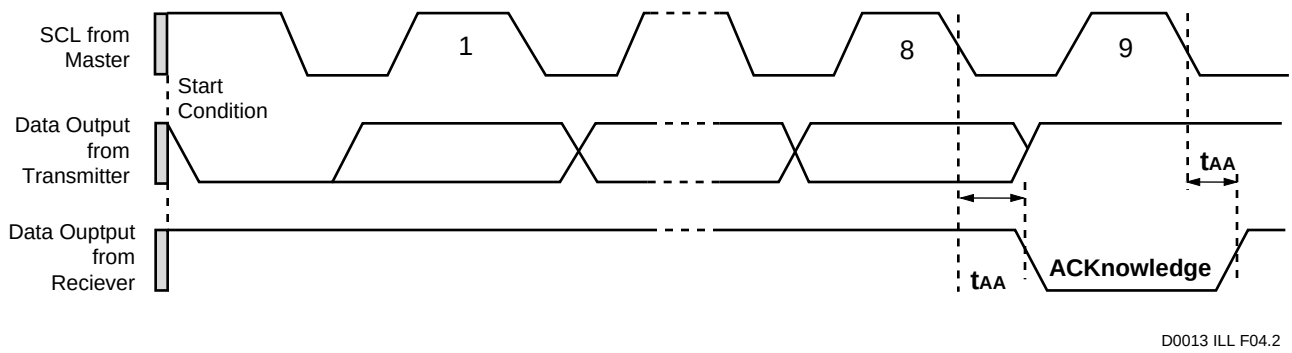


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4.)

The XL24C01A will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a WRITE operation have been selected, the XL24C01A will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C01A transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C01A will continue to transmit data. If an ACKnowledge is not detected, the XL24C01A terminates further data transmissions and awaits a STOP condition before returning to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the address to be accessed. The most significant four bits of the slave address are the “device type identifier.” For an XL24C01A address identifier is 1010 (See Figure 5).

The next three bits are device address, addressing a particular device. Using this addressing scheme, a system may cascade up to eight XL24C01A devices on the bus. The device address is defined by the state of the A0, A1 and A2 input pins.

Read/Write Bit

The last bit of the slave address defines the operation to be performed. When set to “1,” a READ operation is selected; when set to “0,” a WRITE operation is selected.

Device Type Identifier				Device Address			Read/ Write
1	0	1	0	A2	A1	A0	Read = 1 Write = 0

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FIGURE 5. SLAVE ADDRESS BYTE

WRITE OPERATIONS

The XL24C01A allows two types of write operation: byte write and page write. The byte write operations writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 4-byte in the same page to be stored during t_{WR}.

Byte WRITE

For a WRITE operation the XL24C01A requires a word address field after the slave address. This address field comprised of eight bits, with the most significant bit "don't care," provides access to any one of the 128 words of memory.

Upon receipt of the word address, the XL24C01A responds with an ACKnowledge, and waits for the next eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C01A begins the internal WRITE cycle to the nonvolatile array.

While the internal WRITE cycle is in progress, the XL24C01A inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge, and data transfer sequence.

Page WRITE

The XL24C01A is capable of a 4-byte page-WRITE operation. It is initiated in the same manner as the byte-WRITE operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the XL24C01A will respond with an ACKnowledge.

The XL24C01A automatically increments the address for subsequent data words. After the receipt of each word, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-WRITE operation, all inputs are disabled during the internal WRITE cycle. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

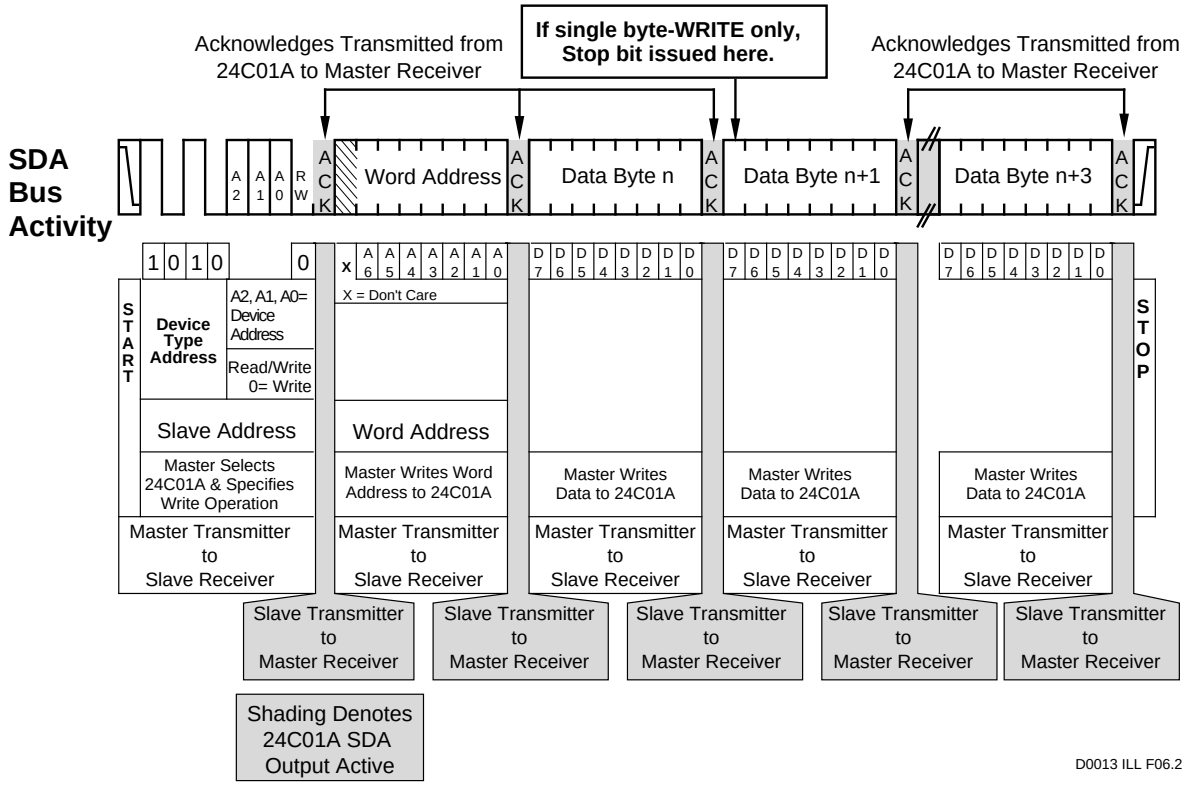

FIGURE 6. PAGE WRITE MODE

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Acknowledge Polling

When the XL24C01A is performing an internal WRITE operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

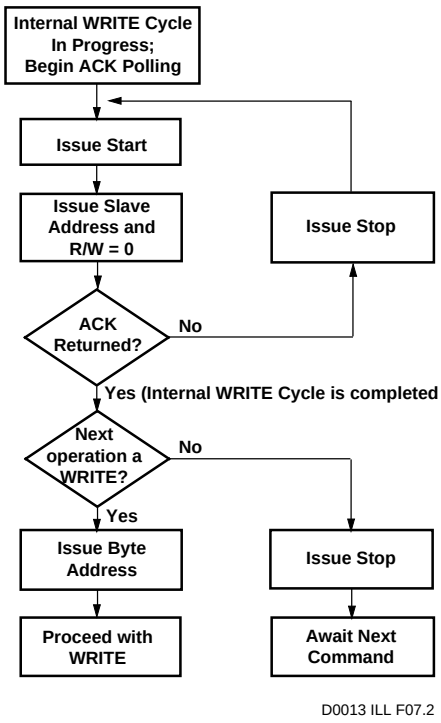

FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

READ operations are initiated with the R/W bit of the slave address byte set to "1." There are four different READ operation options:

1. Current Address Byte READ
2. Random Address Byte READ
3. Current Address Sequential READ
4. Random Address Sequential READ

Current Address Byte READ

The XL24C01A contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a READ or a WRITE) was to address location n, the next READ operation would access data from address n+1, and update the current address pointer. When the XL24C01A receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

The current address READ operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a STOP condition. At this point, the XL24C01A discontinues data transmission. See Figure 8 for the address, acknowledge, and data transfer sequence.

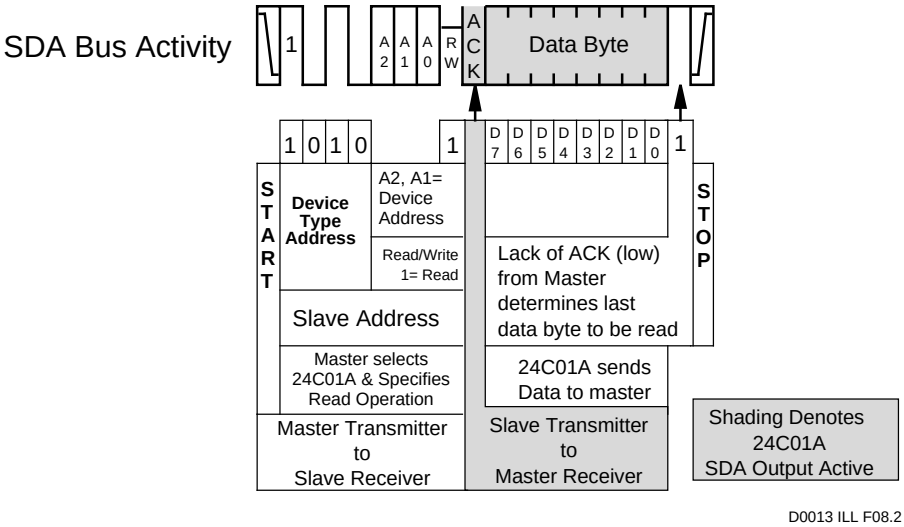

FIGURE 8. CURRENT ADDRESS BYTE READ MODE

Random Address Byte READ

Random address READ operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a WRITE command which includes the START condition and the slave address field (with the R/W bit set to WRITE), followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C01A to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to READ. The XL24C01A will respond with an acknowledge and transmit the eight data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the STOP condition. The XL24C01A discontinues transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge, and data transfer sequence.

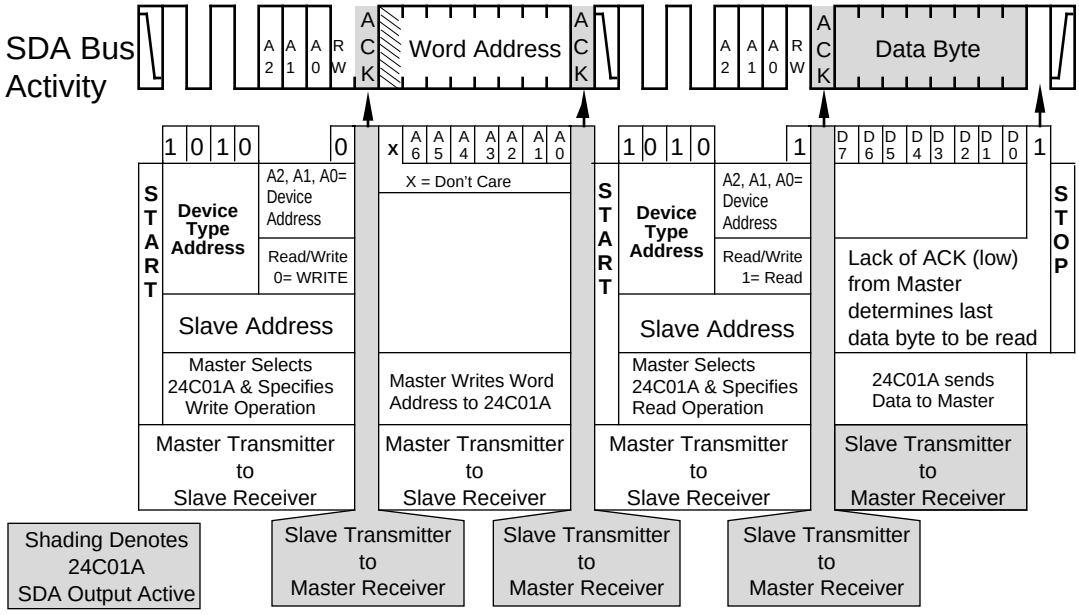

FIGURE 9. RANDOM ADDRESS BYTE READ MODE

Sequential READ

Sequential READs can be initiated as either a current address READ or random address READ. The first word is transmitted as with the other byte READ modes (current address byte READ or random address READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C01A. The XL24C01A continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP condition.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. When the counter reaches the top of the array, it will "roll over" to the bottom of the array and continue to transmit data for each acknowledge bit it receives. See Figure 10 for the address, acknowledge and data transfer sequence.

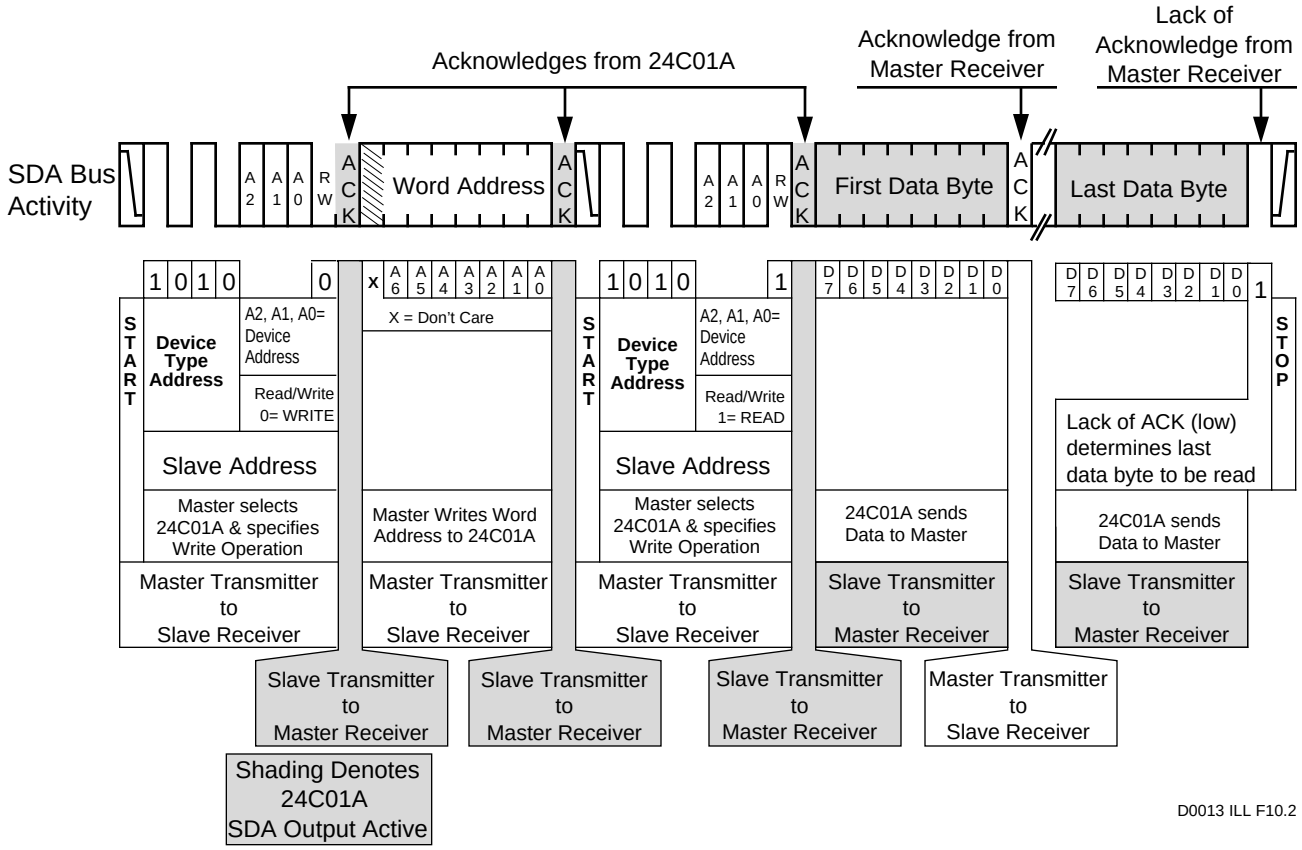

FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.5V to V_{CC}+0.5V
ESD Voltage (JEDEC method) 2,000V
Output Current ..... +5mA

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} = 5V±10%		2	mA
			V_{CC} = 3V±10%		1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND or V_{CC}			2	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	A0-A2, SCL, SDA			0.3xV_{CC}	V
V_{IH}	Input High Voltage	A0-A2, SCL, SDA		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V

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AC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1000	ns
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time Constant @ SCL, SDA Inputs		100	ns
t_{WR}	Write Cycle Time	V_{CC} = 5V±10%		10	ms
		V_{CC}= 3V±10%		15	ms

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CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

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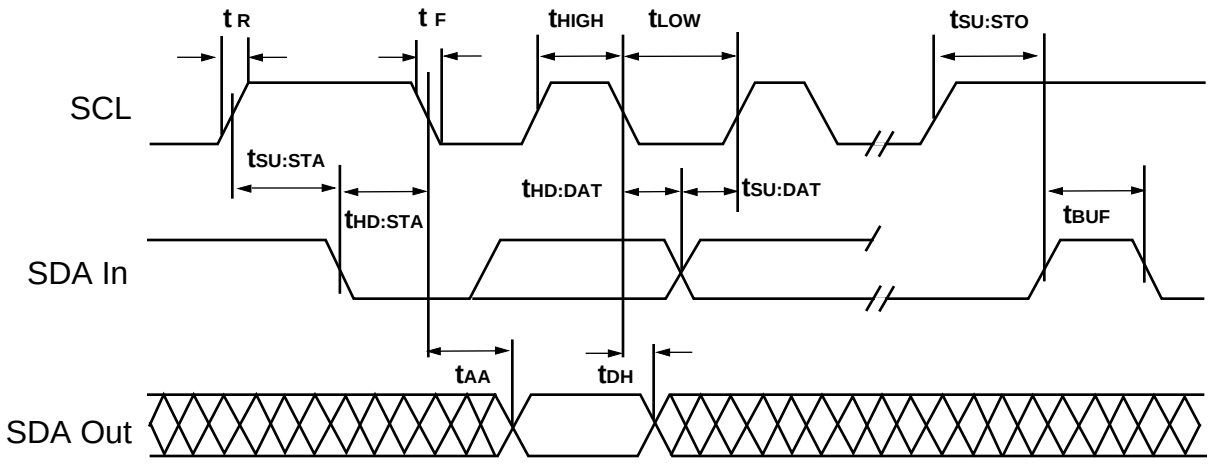

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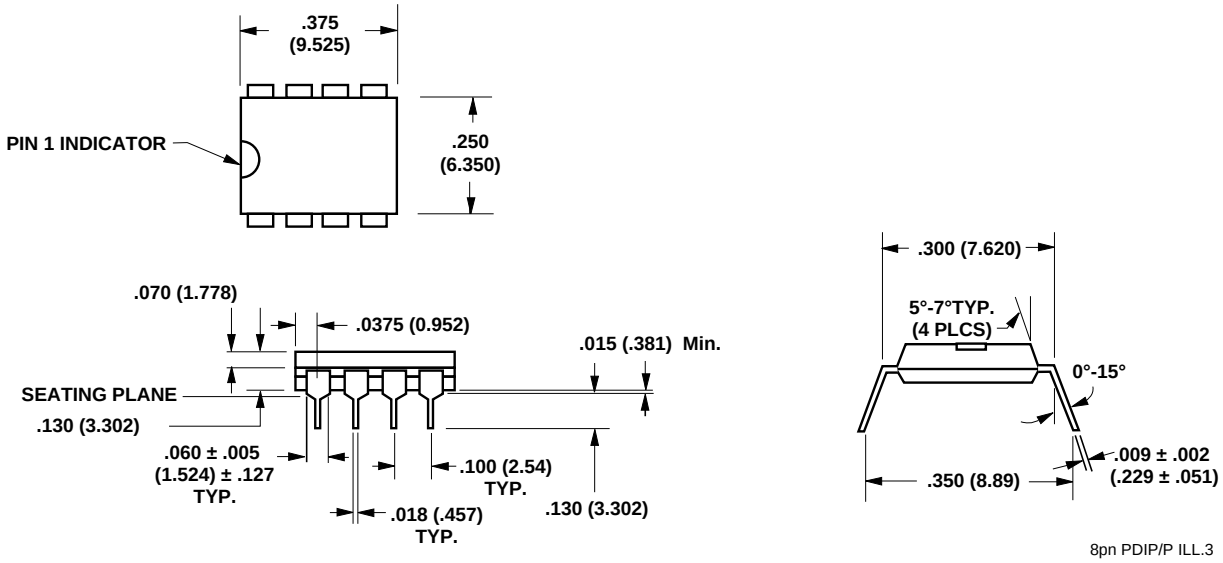
FIGURE 11. BUS TIMING

PACKAGE DIAGRAMS

Plastic Dual-in-line (Type "P") Package (PDIP)*



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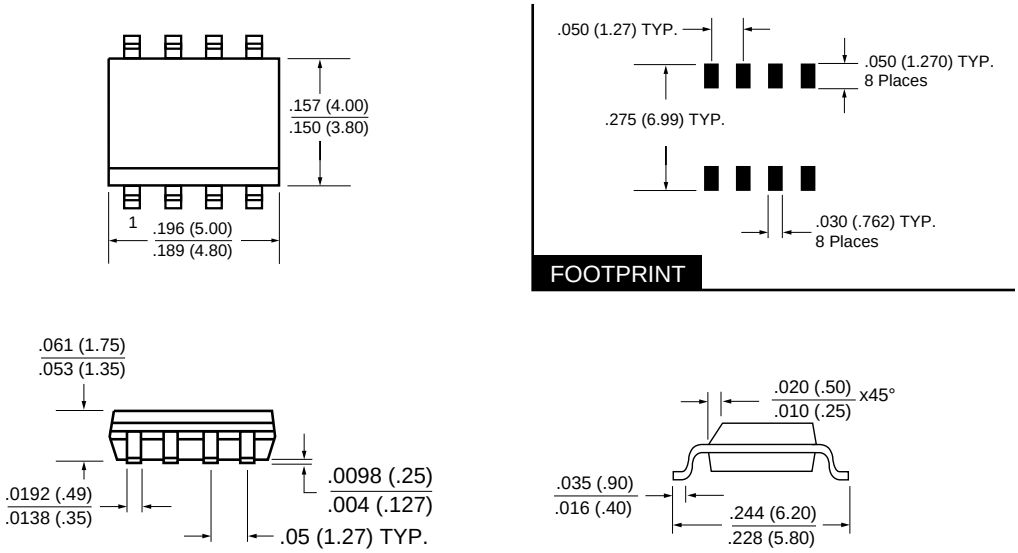
All dimensions in inches (mm).

*See cover page for pinout options.

8 Pin SOIC (Type "Y") Package* (JEDEC 150 mil body width)



All dimensions in inches (mm).

*See cover page for pinout options.

8pn JEDEC SOIC ILL.1

ORDERING INFORMATION

Prefix	Part Number	Package Type
XL	24C01A	Y, P

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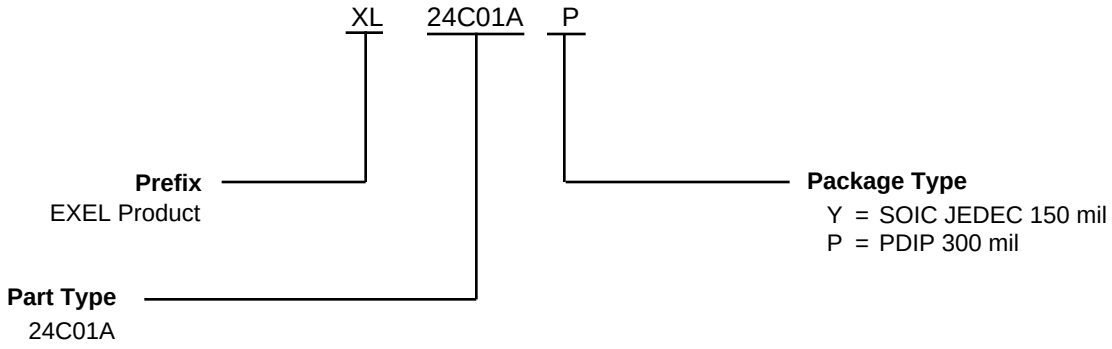
Part Numbers:



MARKING INFORMATION

*See cover page for pinout options.

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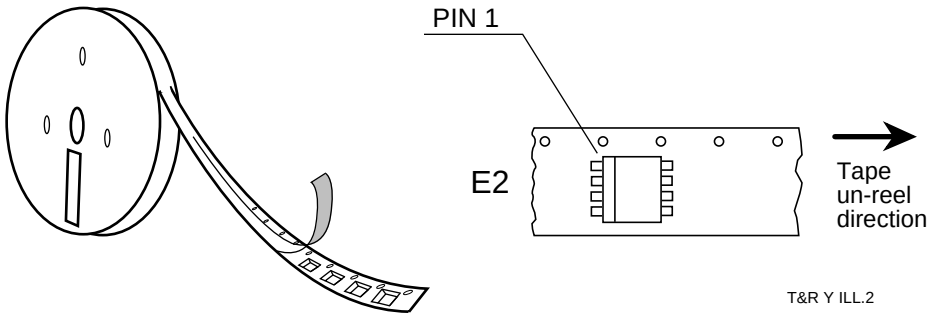
TAPE AND REEL (EMBOSSED) INFORMATION

Surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The following diagram provides general information regarding the direction of the IC's. Tape "E2" shall be designated with PIN 1 at the trail direction.



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