W9952Q

TV ENCODER

Publication Release Date: Febrary,1997
Revision A0.1

The information described in this document is the exclusive intellectual property of Winbond Electronics Corporation and shall not be reproduced without permission from Winbond.

Winbond is providing this document only for reference concerning the W9952Q design. Winbond assumes no responsibility for errors or omissions. All data and specifications are subject to change without notice.

Table of Contents

GENERAL DESCRIPTION

The W9952Q digital video encoder converts YCrCb (4:2:2) 8-bit data into analog composite video and Y/C video signals. The video format is 525-line (M) NTSC/PAL or 625-line (B,D,G,H,I,M,Nc) PAL.

The W9952Q can operate at master or slave mode. The data rate can be CCIR601 or square pixel. At slave mode, the W9952Q can auto detect the input video format from the HSYNCN and VSYNCN pins and generates the corresponding video signals. At master mode, it generates the required video timing internally according to the configuration.

The input YCrCb data are converted into YUV signals. The chroma data are then low passed by a 1.3 MHz filter and modulated by a color subcarrier.

The W9952Q has two DAC outputs which can output two composite video or Y/C S-video signal.

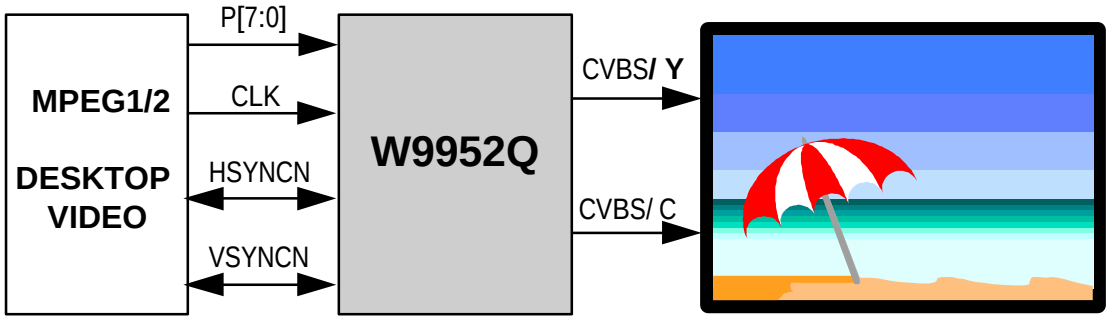
The W9952Q can operate at power-down mode by selecting the SLEEP pin. The W9952Q is designed for digital video applications such as VCD, DVD, and video games.

FEATURES AND APPLICATIONS

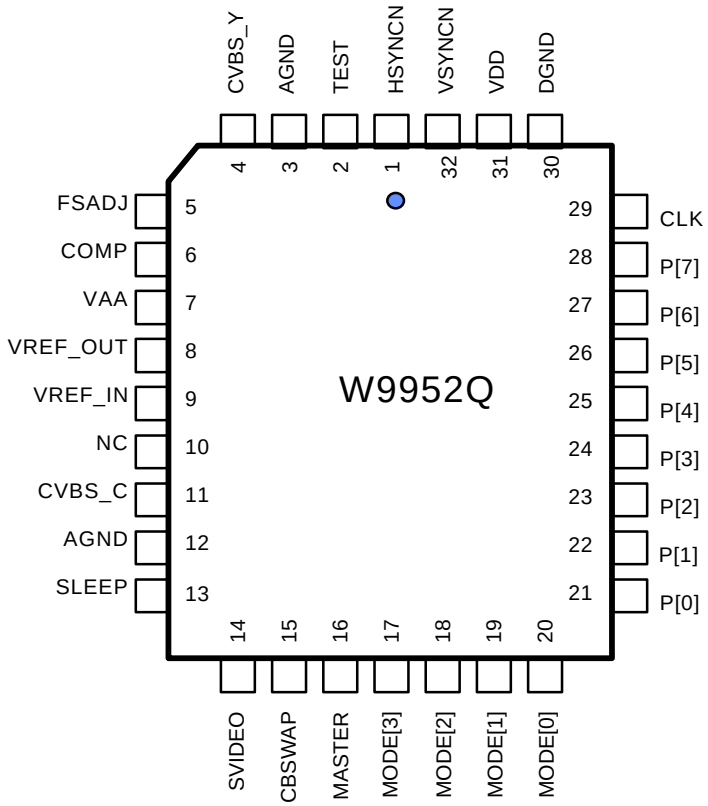
FEATURES

- Monolithic CMOS process
- Two composite outputs or Y/C video output (S video)
- Power-down mode
- CCIR601 or square pixel input data rates
- Master/slave sync signal switchable
- Interlaced and non-interlaced operation
- Optional internal voltage reference

APPLICATIONS



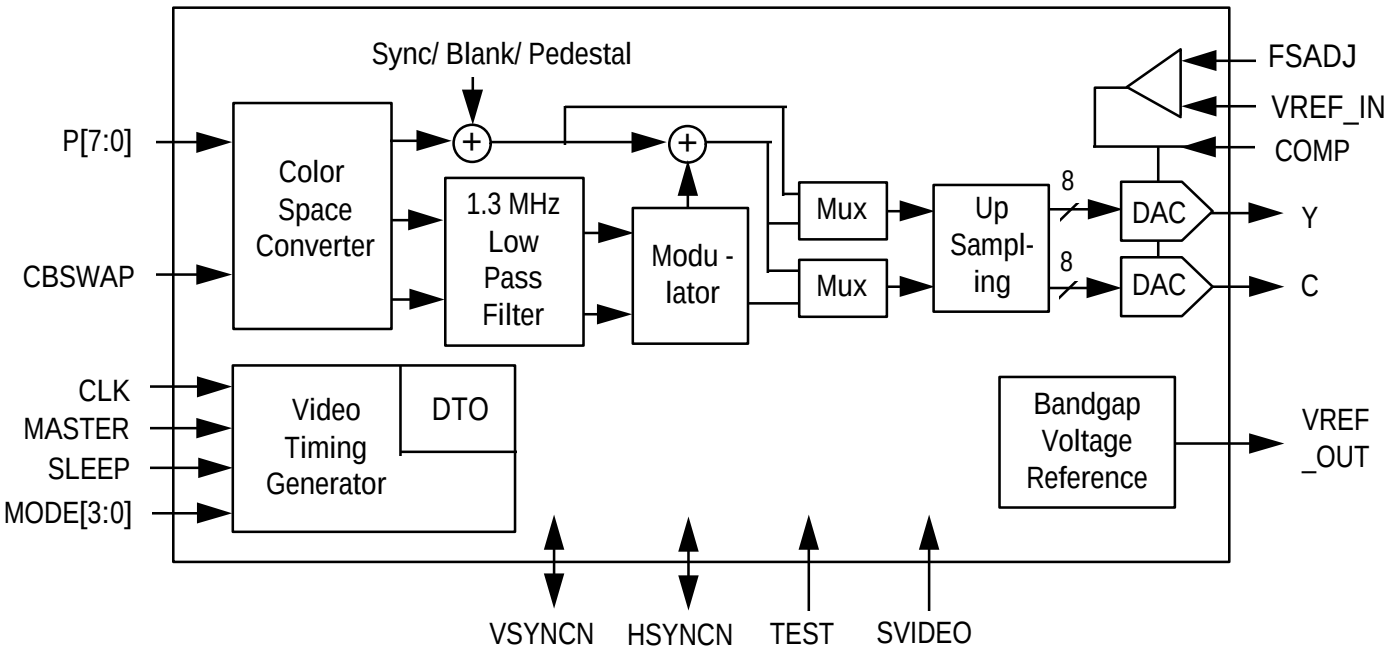
PINOUT AND DESCRIPTION



(All digital pins are TTL compatible)

PIN Number	PIN NAME	I/O	DESCRIPTION
21-28	P[7:0]	I	YCrCb pixel inputs. They are latched on the rising edge of CLK. YCrCb input data conform to CCIR 601.
29	CLK	I	Pixel clock input for 8-bit YCrCb data.
32	VSYNCN	I/O	Vertical sync input/output. VSYNCN is latched/output following the rising edge of CLK.
1	HSYNCN	I/O	Horizontal sync input/output. HSYNCN is latched/output following the rising edge of CLK.
16	MASTER	I	Master/slave mode select. A logical high for master mode operation. A logical 0 for slave mode operation
15	CBSWAP	I	Cr and Cb pixel sequence set up pin. A logic high swap the Cr and Cb sequence.
14	SVIDEO	I	SVIDEO select input pin. A logic high selects Y/C output. A logic low selects composite video output.
13	SLEEP	I	Power save mode. A logic high on this pin puts the chip into power-down mode.
17-20	Mode[3:0]	I	Mode configuration pin.
2	TEST	I	Test pin. These pins must be connected to DGND.
9	VREF_IN	I	Voltage reference input. An external voltage reference must supply typical 1.235V to this pin. A 0.1uF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close as possible to minimize the length of the load. This pin may be connected directly to VREF_OUT.
8	VREF_OUT	O	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive VREF_IN pin directly.
5	FSADJ	---	Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground. The relationship is $RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$.
6	COMP	---	Compensation pin. A 0.1uF ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
4	CVBS_Y	O	Composite/Luminance output. This is a high-impedance current source output. The output format can be selected by the PAL pin. The pin can drive a 37.5 W load. If unused , this pin must be connected directly to GND.
11	CVBS_C	O	Composite/Chroma output. This is a high impedance current source Output. The output format can be selected by the PAL pin. The pin can drive a 37.5 W load. If unused, this pin must be connected directly to GND.
10	NC	---	No connection
31	VDD	---	Digital power pin
30	DGND	---	Digital ground pin
7	VAA	---	Analog power pin
3,12	AGND	---	Analog ground pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input formatting

The input circuitry accepts 8-bit CCIR601 4:2:2 YCrCb data . The data are input via the P[7:0] inputs and latched on the rising edge of CLK.

The input YCrCb pixel sequence can be arranged by setting the CBSWAP pin and the YCSWAP mode register. If the CBSWAP pin and the YCSWAP mode register are all zero, the first pixel data latched by the CLK pin after the falling edge of HSYNCN is Cb. The sequence appears as Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 .... This can be swap by setting the CBSWAP pin and the YCSWAP mode register.

The input clock rate can be CCIR601 13.5MHz or square pixel rate . Color burst frequency is derived from the CLOCK input. Any jitter on the CLOCK pin may induce a color burst frequency error. A stable clock source is recommended.

The Y of the 16-bit YCrCb data has nominal range from 16-235 and Cr/Cb has a nominal range from 16-240, with 128 equal to zero. When the Y value is between 1-15, the internal circuit will clamp these values to 16. When the Y value is 0 and 255, the internal circuit will set the Y value as 38. When the Cr/Cb is between 1-15, the internal circuit will clamp these values to 16. When the Cr value is 0 and 255, the internal circuit will set the Cr value as 112. When Cb value is 0 and 255, the internal circuit will set the Cb value as 225. Thus when the external video source is reset to 0 or 255, the color at video output will appear blue.

Mode selection

There are 7 mode registers which can be programmed by setting the four MODE[3:0] pins and the MASTER pin. The following table illustrates the arrangement of the 7 mode registers.

Pin Description				
The MASTER pin	MODE[3]	MODE[2]	MODE[1]	MODE[0]
0	YCSWAP	SETUP	PALSA	--
1	EFIELD	PAL625	INTERLACED	SQUARE

Mode Register Name	set to 0	set to 1	Comments
EFIELD	The VSYNCN pin will output field signal. Low at VSYNCN pin for even field, high for odd field	The VSYNCN pin will output normal vertical synchronization signal.	This is only used at master mode.
PAL625	525-line operation will be select	The 625-line operation will be select	This is only used at master mode
INTERLACED	Non-interlace operation will be select	The interlace operation will be select	This is only used at master mode
SQUARE	CCIR-601 timing is selected.	The square pixel timing is selected.	This is only used at master mode
YCSWAP	Do not swap Y and Cr/Cb	Swap Y and Cr/Cb sequence	----
SETUP	Disable the 7.5 IRE setup	Enable the 7.5 IRE setup	----
PALSA	When PAL625 register is set to high, PAL-BDGHI mode is selected. When PAL625 register is set to low, NTSC mode is selected.	When PAL625 register is set to high, PAL-Nc mode is selected. When PAL625 register is set to low, PAL-M mode is selected.	----

At slave mode, the W9952Q will automatically detect the input video timing. The EFIELD,PAL625, INTERLACE, and SQUARE register will not be necessary. At master mode, the MODE[3:0] pins will set EFIELD, PAL625, INTERLACED and SQUARE registers. The YCSWAP, SETUP,and PALSA registers can be programmed by switching the W9952Q to slave mode, then back to the master mode. At power-on, the YCSWAP, SETUP,and PALSA are set to zero.

Color space conversion

The 8-bit 4:2:2 YCrCb data input are linearly interpolated to 4:4:4 format and then converted to YUV format.

Low-pass filter

The U/V signal is lowpassed by a digital filter specified by CCIR 624.

Modulator

The U and V color difference signals are modulated by a subcarrier frequency generated by an internal DTO. After modulation, they are summed together to produce luminance signal.

Video timing

The W9952Q can operate in master mode and slave mode. This is done by setting the MASTER pin. When the MASTER pin is set to logical low, the W9952Q operates at slave mode. When The MASTER pin is set to logical high, the W9952Q operates at master mode.

At master mode, the W9952Q automatically generates the required timing from the CLK input. The HSYNCN and VSYNCN pins are output following the rising edge of CLK. Coincident falling edges of HSYNCN and VSYNCN indicates the beginning of an odd field. A falling edge of VSYNC without a coincident falling edge of HSYNCN indicates the beginning of an even field.

At slave mode, the W9952Q accepts external horizontal and vertical synchronization signals via the HSYNCN and VSYNCN pins and automatically detects the input video format. The W9952Q then generates the detected video timing.

The W9952Q automatically calculates the width of the horizontal sync pulse and the start and end of color burst. Color burst is automatically disabled on appropriate lines. Serration and equalization pulses are automatically inserted into appropriate lines.

Video and Burst Blanking

Video and burst information is automatically disabled according to the Rec. CCIR624.

Power Down

When the SLEEP pin is logical high, the W9952Q enters sleep mode. The clock input and DAC outputs are disabled.

Analog outputs

There are two 8-bit D/A converter outputs: CVBS_Y and CVBS_C. These two outputs are specified to drive 37.5 Ω load. When the SVIDEO pin is connected to high, the CVBS_Y will output luminance signal and CVBS_C will output signal which can be interface to the S-Video machine. When the SVIDEO pin is connected to low, both the CVBS_Y and CVBS_C will output composite videos.

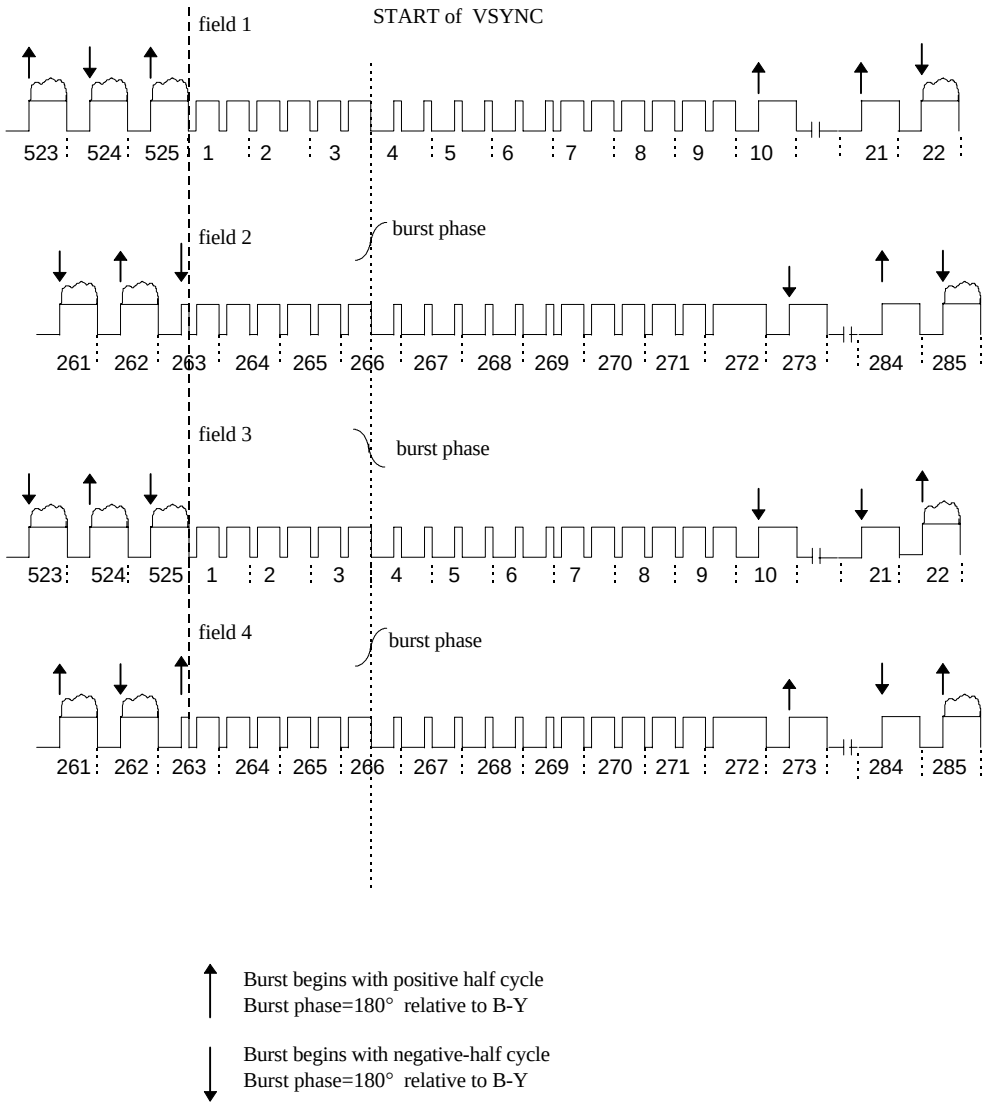


Figure 1. NTSC Interlace Video Timing
(SMPTE line conversion rather than CCIR-624 is used)

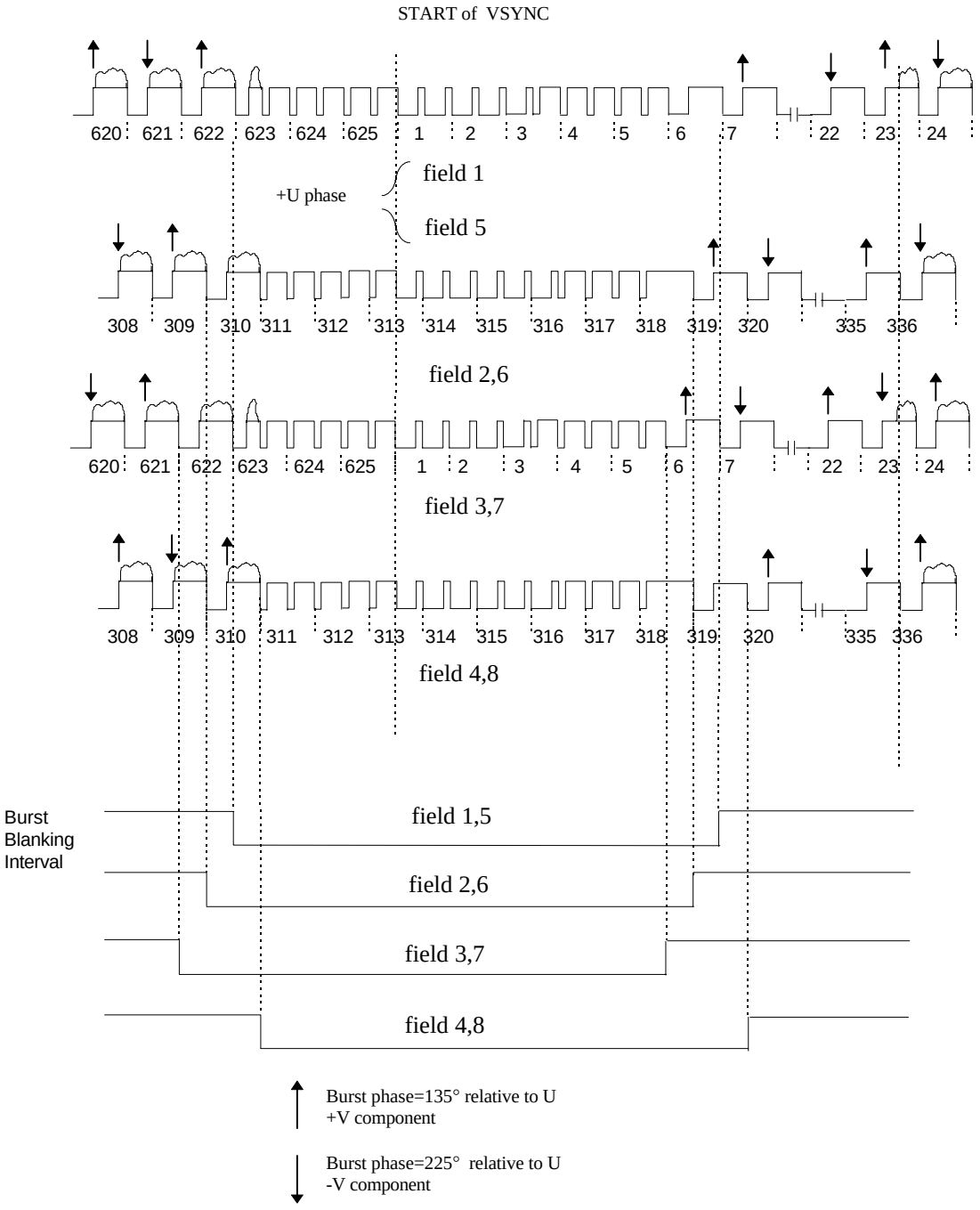


Figure 2. B,D,G,H,I/PAL Interlace Video Timing

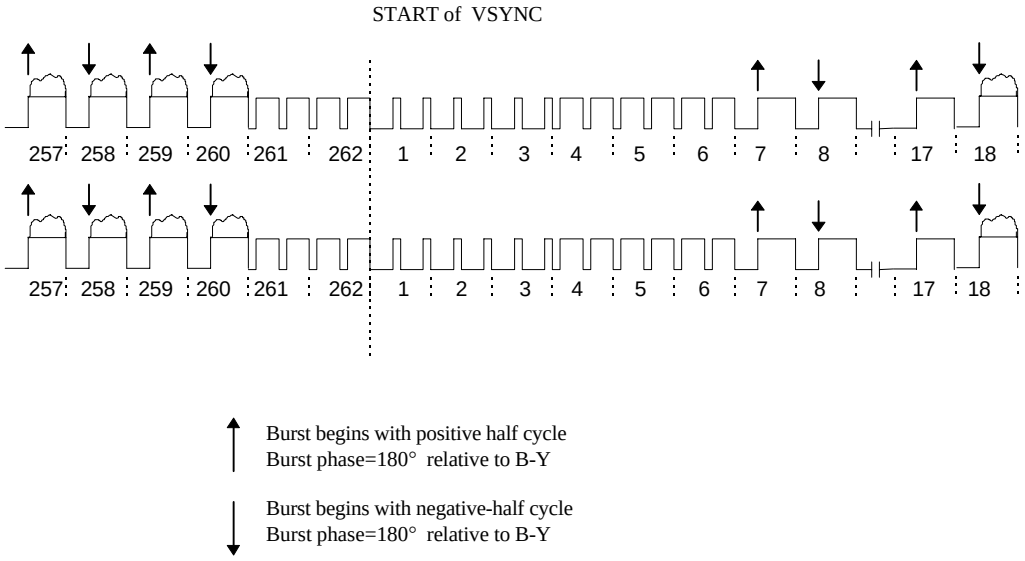


Figure 3. NTSC Non-interlace Video Timing

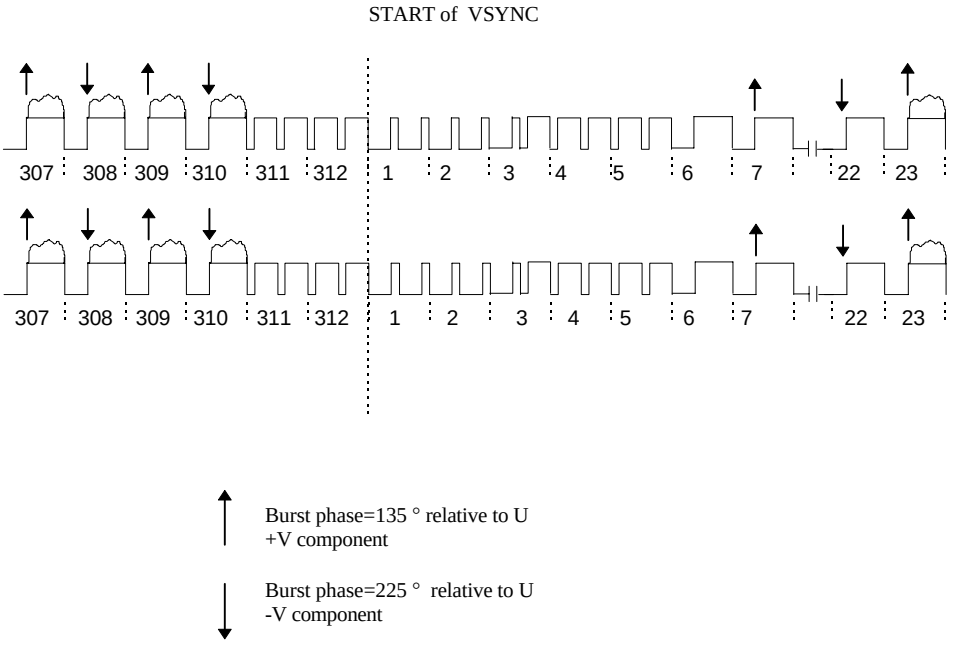


Figure 4. PAL Non-interlace Video Timing

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0	--	70	°C
DAC Output Load	RL	50	--	--	Ω
External Voltage Reference	VREF_IN	1.14	1.235	1.26	V

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply (Measured to ground)	VAA	--	--	7	V
Ambient Operating Temperature	TA	-55	--	125	°C
Voltage on Any Signal Pin		GND-0.5		VAA+0.5	V
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latchup.					

DC Characteristics

(Recommended operating conditions using external voltage reference with RSET= 67 Ω, VREFIN= 1.235V, NTSC CCIR601 operation and clock frequency= 27 MHz at 25°C, +5V)

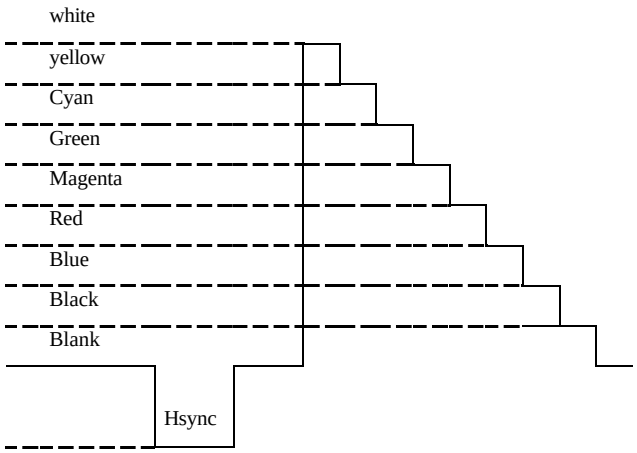
Parameter	Symbol	Min.	Typ.	Max.	Unit
VAA Supply Current	IAA@ 70 C IAA@ 0 C		100 100	tbd tbd	mA mA
Video D/A Resolution		8	8	8	Bits
Integral Nonlinearity	INL			+/- 1	LSB
Differential Nonlinearity	DNL			+/- 1	LSB
Maximum Output Current				26.04	mA
Output Compliance	VOC	0		1.5	V
Video level Error					
Using External Reference				5	%
Using Internal Reference				10	%
Full-Scale DAC Output			182.5		IRE
Digital Inputs					
Input High Voltage	VIH	2.0		VAA+0.5	V
Input Low Voltage	VIL	GND-0.5		0.8	V
Input High current (Vin=2.4V)	IIH			1	uA
Input Low current (Vin=0.4V)	IIL			-1	uA
Digital Outputs					
Output High Voltage (IOH=-400uA)	VOH	2.4			V
Output Low Voltage (IOL=3.2mA)	VOL			0.4	V
Three-State Current	IOZ			50	uA
VREF_IN Input Current	IREF_IN		10		uA
VREF_OUT Output Voltage	VREF_OUT	1.064	1.18	1.298	V
VREF_OUT current	IREF_OUT		10		uA

AC Characteristics

(Recommended operating conditions using external voltage reference with RSET=67 Ω, VREFIN=1.235V, NTSC CCIR601 operation and clock frequency=27 MHz at 25 °C, +5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Luminance Bandwidth			Fin/4		MHz
Chrominance Bandwidth			1.3		MHz
Differential Gain			1		%
Differential Phase			1		°
SNR			60		dB
Hue Accuracy			1.5	3	°
Color Saturation Accuracy			1.5	3	%
Analog Output Delay	5		30		ns
Analog Output Rise Time			3		ns
Analog Output Settling Time			30		ns
Pixel/Control Setup Time	1	0			ns
Pixel/Control Hold Time	2	6			ns
Control Output Delay Time	3		15		ns
CLOCK Frequency	Fin	24.54	27	29.5	MHz
CLOCK Pulse Width Low Time		10			ns
CLOCK Pulse Width High Time		10			ns
Pipeline Delay	4		28		Clocks

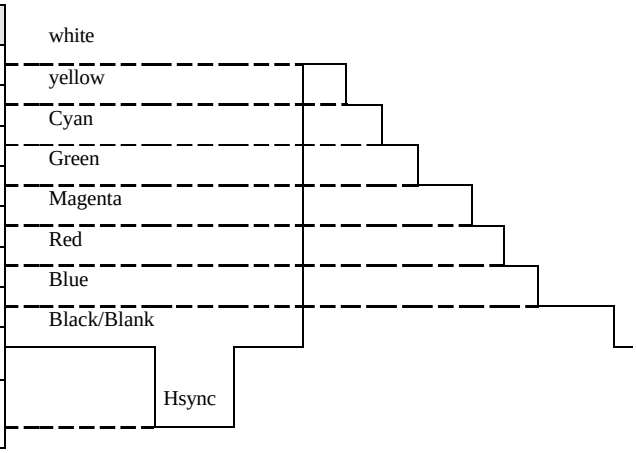
Level	HSYNC	BLANK	mA	V	IRE
White	1	1	20.42	1.021	100
Yellow	1	1	18.81	0.944	
Cyan	1	1	16.34	0.817	
Green	1	1	14.91	0.745	
Magen	1	1	12.56	0.628	
Red	1	1	11.13	0.556	
Blue	1	1	8.58	0.429	
Black	1	1	7.20	0.360	7.5
Blank	1	0	6.13	0.306	0
Sync	0	0	0.41	0.02	-40



Note: 37.5Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

Figure 5. NTSC Y (Luminance) Output Waveform

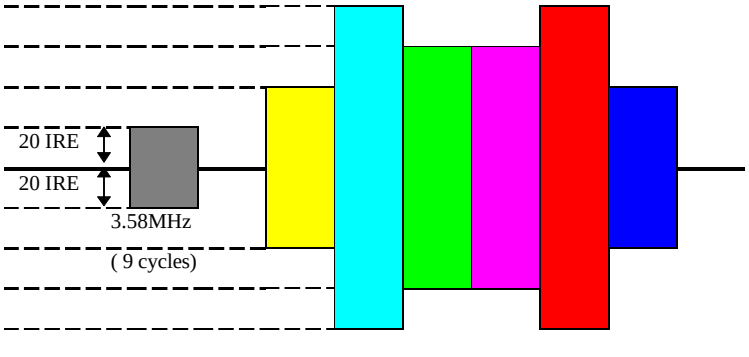
Level	HSYNC	BLANK	mA	V	IRE
White	1	1	20.82	1.041	100
Yellow	1	1	19.19	0.960	
Cyan	1	1	16.54	0.827	
Green	1	1	14.91	0.745	
Magen	1	1	12.06	0.623	
Red	1	1	10.72	0.536	
Blue	1	1	8.17	0.408	
Black/	1	1	6.53	0.327	0
Sync	0	0	0.41	0.020	-43



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIR624 levels and tolerance are assumed.

Figure 6. PAL-BDGHI Y (Luminance) Output Waveform

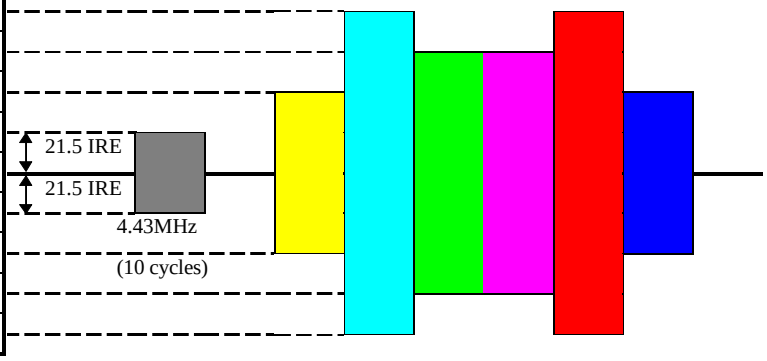
Color	mA	V
Cyan/Red	21.44	1.071
Green/magen	20.93	1.047
Yellow/Blue	28.99	0.950
Peak Burst	15.92	0.794
Blank	13.07	0.653
Peak Burst	10.21	0.510
Yellow Blue	7.15	0.357
Green/Mage	5.21	0.260
Cyan/Red	4.7	0.235



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

Figure 7. NTSC C (Chroma) Output Waveform

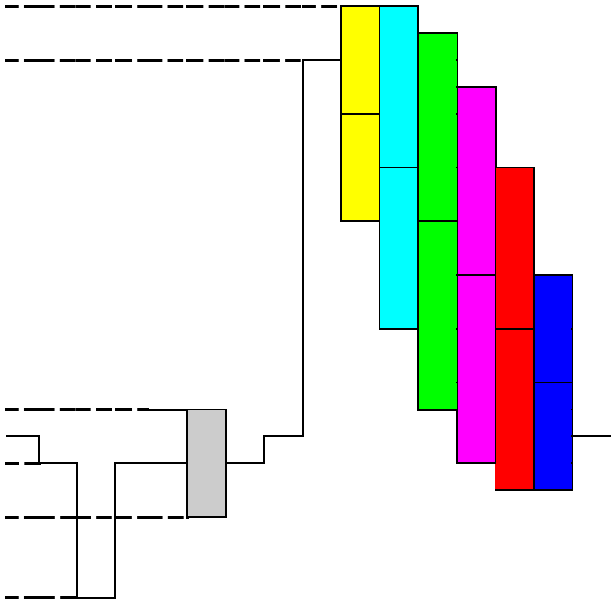
Color	mA	V
Cyan/Red	22.15	1.107
Green/magen	21.54	1.077
Yellow/Blue	19.50	0.975
Peak Burst	16.13	0.806
Blank	13.07	0.653
Peak Burst	10.00	0.500
Yellow Blue	6.64	0.332
Green/Mage	4.59	0.230
Cyan/Red	3.98	0.199



Note: 37.5 Ω load is used. VREF_IN=1.235V RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIR 624 levels and tolerance are assumed.

Figure 8. PAL-BDGHI C (Chroma) Output Waveform

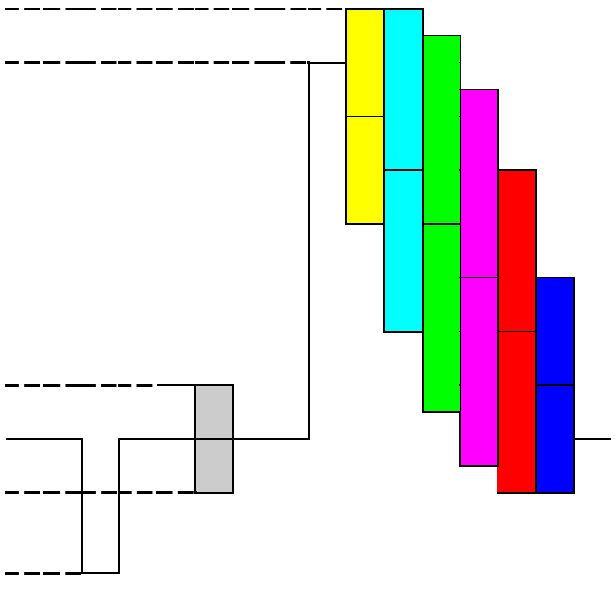
	1	1	24.8	1.24	134
	1	1	20.4	1.02	100
	1	1	8.99	0.44	20
	1	1	7.20	0.36	7.5
	1	0	6.13	0.30	0
	1	0	3.27	0.16	-20
	0	0	0.41	0.02	-40



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. RS170A levels and tolerance are assumed.

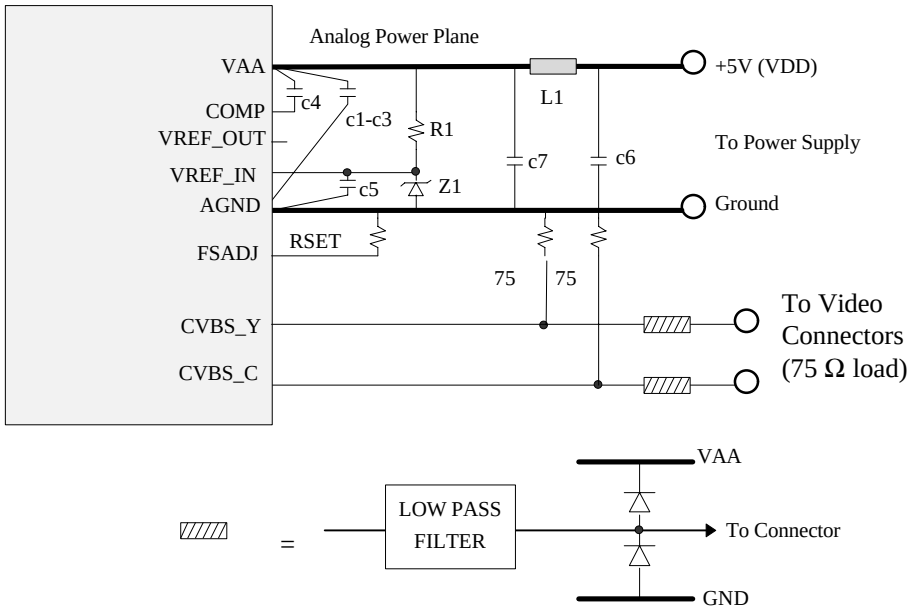
Figure 9. NTSC Composite Output Waveform

	1	1	25.6	1.28	133
	1	1	20.8	1.04	100
	1	1	9.59	0.48	21.5
	1	0	6.53	0.32	0
	1	0	3.47	0.17	-21.5
	0	0	0.41	0.02	-43



Note: 37.5 Ω load is used. VREF_IN=1.235V, RSET=67 Ω. 100% amplitude, 100% saturation are shown. CCIR 624 levels and tolerance are assumed.

Figure 10. PAL-BDGHI Composite Output Waveform

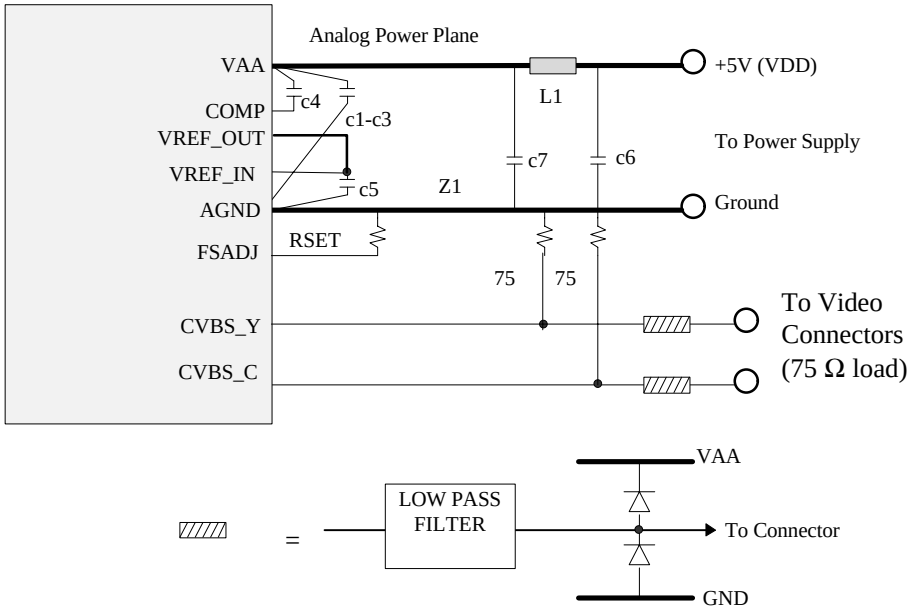


Part Number	Value	Vendor number
c1-c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
R1	1KW (5%)	
RSET	1% Metal Film	Dale CMF-55C
Z1	1.2V Zener Diode	LM358BZ-1.2

Note: 1. The vendor number is only for reference.
2. RSET is determined by (Iout=full scale output current)

$$RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$$

Figure 11. Typical connection diagram and part list
(using external voltage reference)



Part Number	Value	Vendor number
c1-c6	0.1uF (Ceramic)	Erie RPE112Z5U104M50V
c7	47uF	Mallory CSR13F476KM
L1	Ferrite bead	Fair-Rite 2743001111
RSET	1% Metal Film	Dale CMF-55C
Note: 1. The vendor number is only for reference. 2. RSET is determined by (Iout=full scale output current) $RSET(\Omega) = 2015 * VREF\_IN(V) / Iout(mA)$		

Figure 12. Typical connection diagram and part list
(using internal voltage reference)

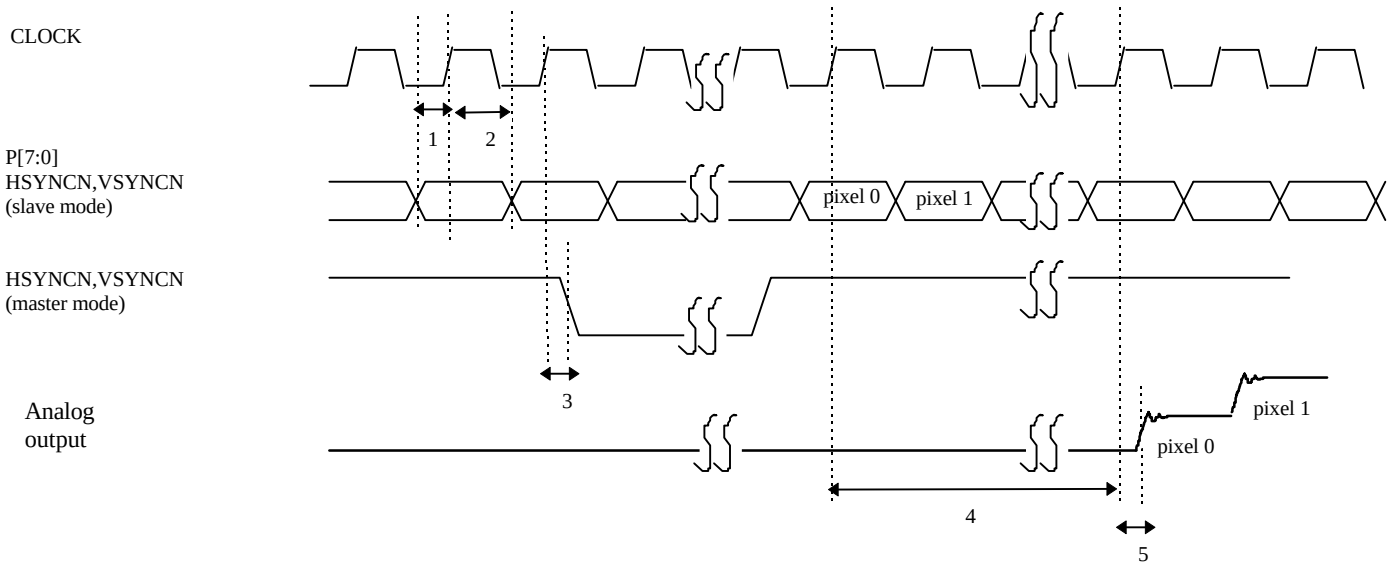


Figure 13. Video Input and Output Timing

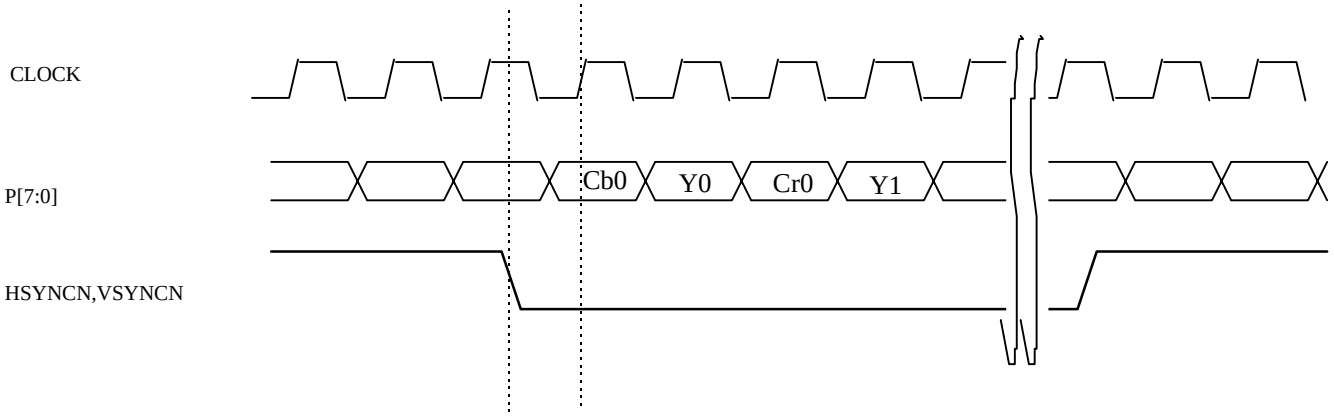
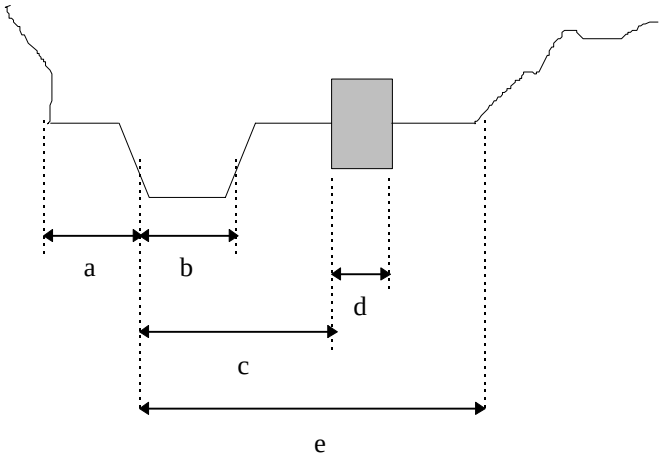


Figure 14. pixel sequence at power on reset
(The pixel sequence can be swap by setting the CBSWAP pin and the MODE[3] pin at slave mode)

Operating Mode	Active pixels	Total Pixels	CLK Frequency (MHz)
NTSC/PAL-M CCIR601	720 x 240	858 x 262	27
PAL-B,D,G,H,I,Nc	720 x 288	864 x 313	27
NTSC/PAL-M Square pixel	640 x 240	780 x 262	24.545454
PAL-B,D,G,H,I,Nc Square pixel	768 x 288	944 x 312	29.5

Table1. Field Resolution and clock Rates for Various Modes of Operation

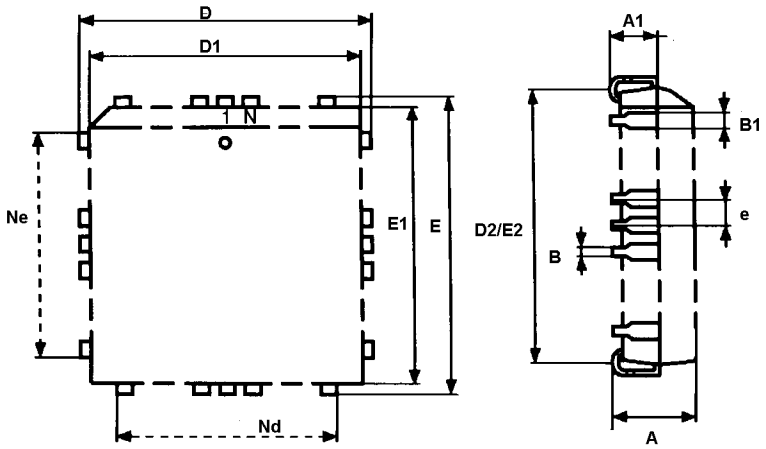


Operation Mode	Front porch (e)	Horizontal Sync Width (b)	Start of Burst (c)	Duration of Burst (d)	Back porch (e)
NTSC CCIR601	20	63	72	34	127
PAL-M CCIR610	20	63	78	34	127
PAL-B CCIR601	20	63	76	30	142
PAL-Nc CCIR601	20	63	76	34	142
NTSC SQUARE	18	58	65	31	115
PAL-M SQUARE	18	58	71	31	115
PAL-B SQUARE	22	69	83	33	155
PAL-Nc SQUARE	22	69	83	37	155
Notes: (1) The unit is the number of luminance pixel.					

Table 2. Various Video Timing

PACKAGE INFORMATION

Model Number	Package	Ambient Temperature Range
W9952Q	32-pin PLCC	0° C -70° C



Symbol	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.1		0.14	2.54		3.56
A1	0.06		0.09	1.52		2.41
B	0.013		0.02	0.33		0.53
B1	0.026		0.03	0.66		0.81
D	0.485		0.49	12.3		12.57
D1	0.447		0.45	11.3		11.56
D2	0.39		0.43	9.91		10.92
E	0.585		0.59	14.8		15.11
E1	0.547		0.55	13.8		14.1
E2	0.49		0.53	12.5		13.46
e		0.05			1.27	
N					32	
Nd					7	
Ne					9	