Winbond
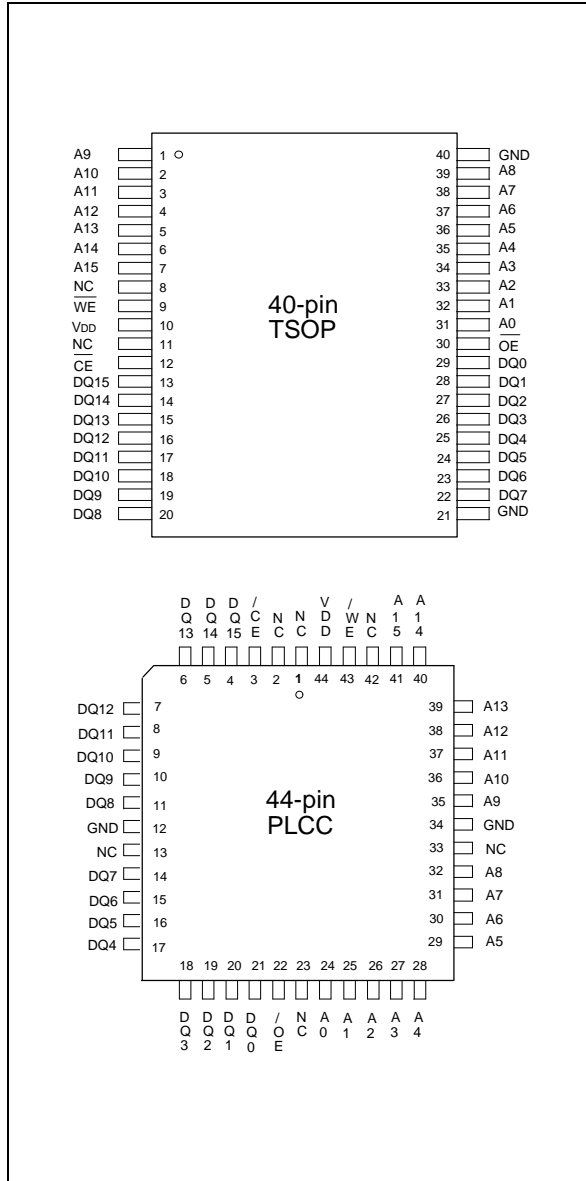Electronics Corp.

64K × 16 CMOS 3.3V FLASH MEMORY

GENERAL DESCRIPTION

The W29N102C is a 1-megabit, 3.3-volt only CMOS flash memory organized as 64K × 16 bits. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29N102C results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.
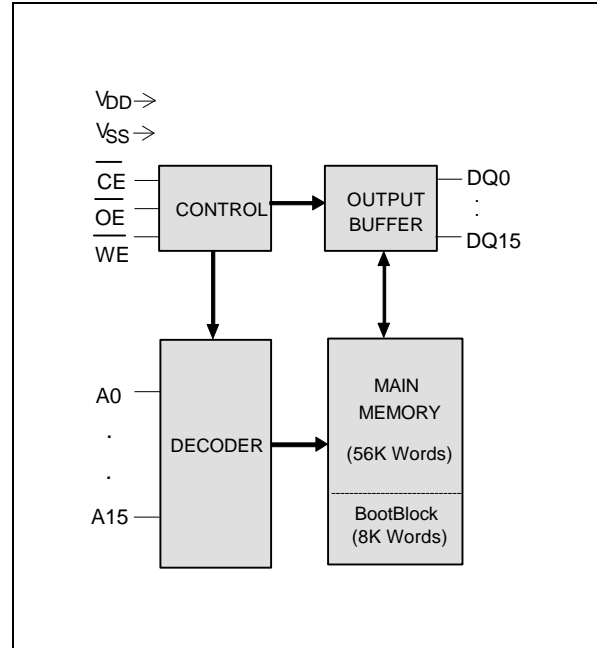
FEATURES

- Single 3.3-volt operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast Program operation:
  - Word-by-Word programming: 50 μS (max.)
- Fast Erase operation: 100 mS (typ.)
- Fast Read access time: 55/70/90 nS
- Endurance: 1K/10K cycles (typ.)
- Twenty-year data retention
- Hardware data protection
- 8K word Boot Block with Lockout protection

- Low power consumption
  - Active current: 15 mA (typ.)
  - Standby current: 10 μA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 40-pin TSOP and 44-pin PLCC

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PIN CONFIGURATIONS

40-pin TSOP

A9	1	40	GND
A10	2	39	A8
A11	3	38	A7
A12	4	37	A6
A13	5	36	A5
A14	6	35	A4
A15	7	34	A3
NC	8	33	A2
$\overline{WE}$	9	32	A1
V$_{DD}$	10	31	A0
NC	11	30	$\overline{OE}$
$\overline{CE}$	12	29	DQ0
DQ15	13	28	DQ1
DQ14	14	27	DQ2
DQ13	15	26	DQ3
DQ12	16	25	DQ4
DQ11	17	24	DQ5
DQ10	18	23	DQ6
DQ9	19	22	DQ7
DQ8	20	21	GND

44-pin PLCC

BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A15	Address Inputs
DQ0–DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V$_{DD}$	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29N102C is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000 hex to 1FFF hex.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block can not be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will only affect the main memory.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Input Levels

While operating with a 3.0V-3.6V power supply, the address inputs and control inputs ($\overline{OE}, \overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to 3.6V.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the main memory will be erased to FF(hex), and the data in the boot block will not be erased (remains same as before the chip erase operation). The entire memory array (main memory and boot block) will be erased to FF hex. by the chip erase operation if the boot block programming lockout feature is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Main Memory Erase Operation

The main memory erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal main-memory erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal

read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Program Operation

The W29N102C is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0" The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will interally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 μS max. - T_{BP}) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W29N102C is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 1.8V typical.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 10 mS before any write (erase/program) operation.

Data Polling (DQ7 & DQ15)- Write Status Detection

The W29N102C includes a data polling feature to indicate the end of a program or erase cycle. When the W29N102C is in the internal program or erase cycle, any attempt to read DQ_7 or DQ_{15} of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 or DQ_{15} will show the true data. Note that DQ_7 or DQ_{15} will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.

Toggle Bit (DQ6 & DQ14)- Write Status Detection

In addition to data polling, the W29N102C provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 or DQ_{14} will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (00DAh). A read from address 0001H outputs the device code (00BFh). The product ID operation can be terminated by a three-word command sequence or an altenate one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V $\pm$0.5V)

MODE	PINS				
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1–A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1–A15 = V_{IL}; A9 = V_{HH}	Device Code 00BF (Hex)

TABLE OF COMMAND DEFINITION

Command Description	No. of Cycles	1st Cycle Addr. Data	2nd Cycle Addr. Data	3rd Cycle Addr. Data	4th Cycle Addr. Data	5th Cycle Addr. Data	6th Cycle Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Main Memory Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 30
Word Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit [1]	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit [1]	1	XXXX F0					

Note: Address Format: A14–A0 (Hex); Data Format: DQ15–DQ8 (Don't Care); DQ7-DQ0 (Hex)

Either one of the two Product ID Exit commands can be used.

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Command Codes for Word Program

WORD SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-Address	Programmed-Data

Word Program Flow Chart

**Word Program
Command Flow**

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

↓

Load data A0
to
address 5555

↓

Load data Din
to
programmed-
address

↓

Pause 50 μS

↓

Exit
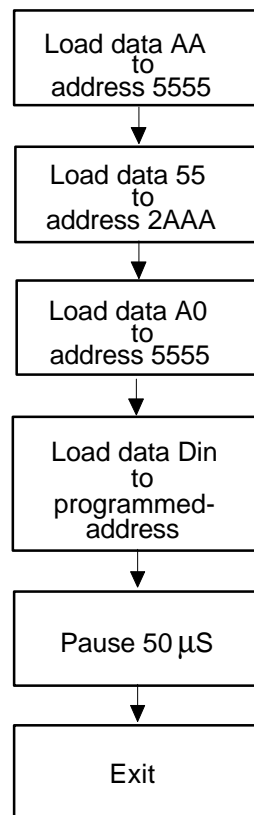
Notes for software program code:

Data Format: DQ15–DQ0 (Hex); XX = Don't Care

Address Format: A14–A0 (Hex)

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Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H

Chip Erase Acquisition Flow

```
┌─────────────────┐
│  Load data AA   │
│       to        │
│  address 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│  Load data 55   │
│       to        │
│  address 2AAA   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│  Load data 80   │
│       to        │
│  address 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│  Load data AA   │
│       to        │
│  address 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│  Load data 55   │
│       to        │
│  address 2AAA   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│  Load data 10   │
│       to        │
│  address 5555   │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│   Pause 1 Sec.  │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│      Exit       │
└─────────────────┘
```
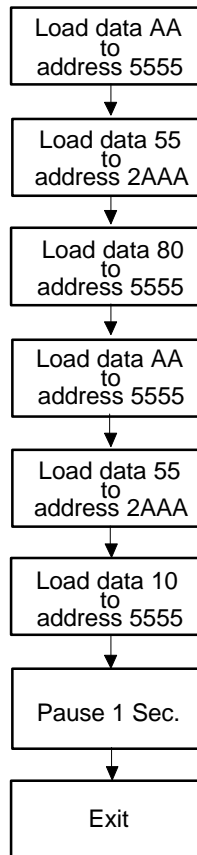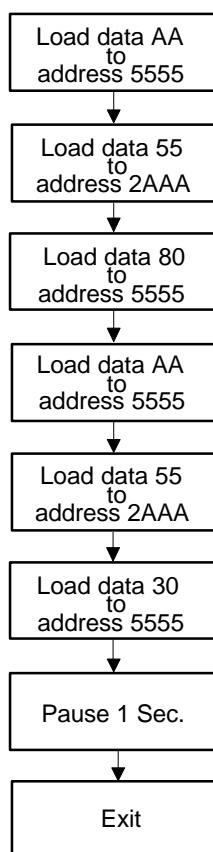
Notes for chip erase:

Data Format: DQ15-DQ8: Don't Care; DQ7−DQ0 (Hex)

Address Format: A14−A0 (Hex)

Command Codes for Main Memory Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	30H

Main Memory Erase Acquisition Flow

```
Load data AA
     to
address 5555
     ↓
Load data 55
     to
address 2AAA
     ↓
Load data 80
     to
address 5555
     ↓
Load data AA
     to
address 5555
     ↓
Load data 55
     to
address 2AAA
     ↓
Load data 30
     to
address 5555
     ↓
Pause 1 Sec.
     ↓
   Exit
```

Notes for chip erase:

Data Format: DQ15-DQ8: Don't Care; DQ7−DQ0 (Hex)
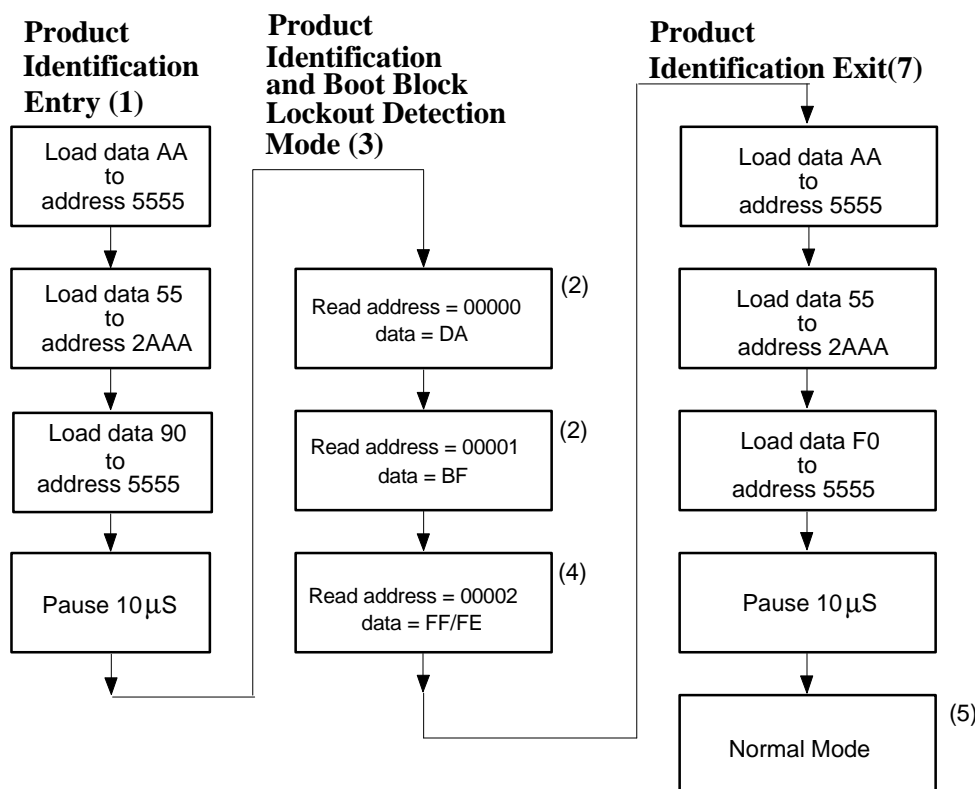
Address Format: A14−A0 (Hex)

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Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (6) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT (7)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 20μS		Pause 20μS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow

Product Identification Entry (1)

Load data AA to address 5555

Load data 55 to address 2AAA

Load data 90 to address 5555

Pause 10μS

Product Identification and Boot Block Lockout Detection Mode (3)

Read address = 00000 data = DA (2)

Read address = 00001 data = BF (2)

Read address = 00002 data = FF/FE (4)

Product Identification Exit(7)

Load data AA to address 5555

Load data 55 to address 2AAA

Load data F0 to address 5555

Pause 10μS

Normal Mode (5)

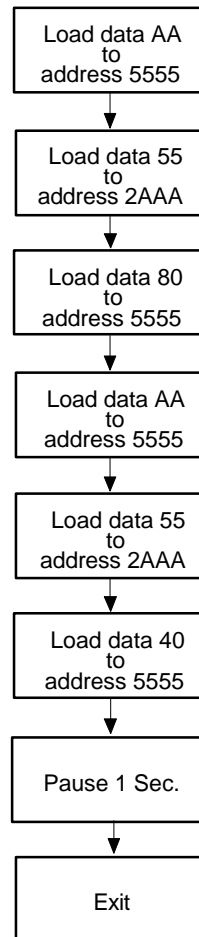Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ15-DQ8 (Don't Care), DQ7−DQ0 (Hex); Address Format: A14−A0 (Hex)

(2) A1−A15 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.

(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
	Pause 1 Sec.	

Boot Block Lockout Enable Acquisition Flow

**Boot Block Lockout
Feature Set Flow**

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

↓

Load data 80
to
address 5555

↓

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

↓

Load data 40
to
address 5555

↓

Pause 1 Sec.

↓

Exit

Notes for boot block lockout enable:
Data Format: DQ15-DQ8 Don't Care), DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

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DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$=$\overline{OE}$= V_{IL}, $\overline{WE}$= V_{IH}, all I/Os open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	15	25	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all I/Os open Other inputs = V_{IL}/V_{IH}	-	-	1	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all I/Os open Other inputs = V_{DD} -0.3V/GND	-	10	50	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.6	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1 mA	2.4	-	-	V

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Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	T_{PU}. READ	200	μS
Power-up to Write Operation	T_{PU}. WRITE	10	mS

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.4V/2.4V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF for 55/70 nS
	C_L = 100 pF for 90 nS

AC Test Load and Waveform

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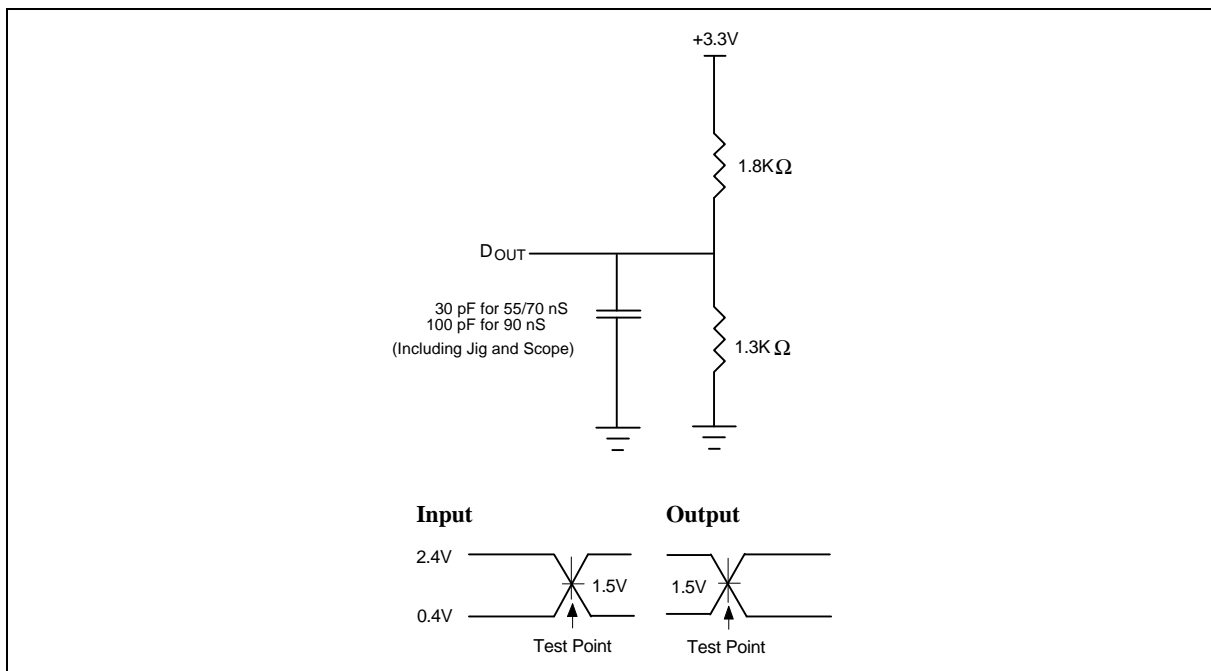
AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W29N102C-55		W29N102C-70		W29N102C-90		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	55	-	70	-	90	-	nS
Chip Enable Access Time	T_{CE}	-	55	-	70	-	90	nS
Address Access Time	T_{AA}	-	55	-	70	-	90	nS
Output Enable Access Time	T_{OE}	-	30	-	35	-	40	nS
$\overline{CE}$ Low to Active Output	T_{CLZ}	0	-	0	-	0	-	nS
$\overline{OE}$ Low to Active Output	T_{OLZ}	0	-	0	-	0	-	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	25	-	30	-	30	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	25	-	30	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	10	-	-	nS
Address Hold Time	T_{AH}	100	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	200	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	200	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	200	-	-	nS
Data Setup Time	T_{DS}	100	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Word Programming Time	T_{BP}	-	30	50	μS
Erase Cycle Time	T_{EC}	-	0.1	1	Sec.

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W29N102C-55		W29N102C-70		W29N102C-90		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{OE}$ to Data Polling Output Delay	T_{OEP}	-	30	-	35	-	40	nS
$\overline{CE}$ to Data Polling Output Delay	T_{CEP}	-	55	-	70	-	90	nS
$\overline{OE}$ to Toggle Bit Output Delay	T_{OET}	-	30	-	35	-	40	nS
$\overline{CE}$ to Toggle Bit Output Delay	T_{CET}	-	55	-	70	-	90	nS

TIMING WAVEFORMS

Read Cycle Timing Diagram
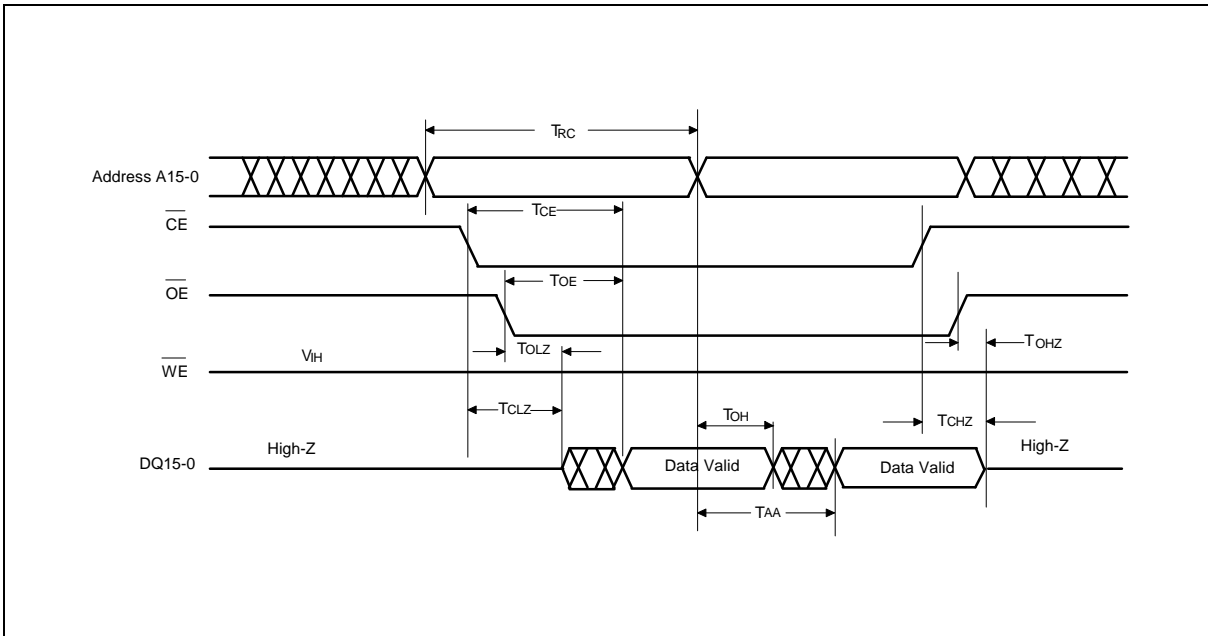
Timing Waveforms, continued

$\overline{\text{WE}}$ Controlled Command Write Cycle Timing Diagram
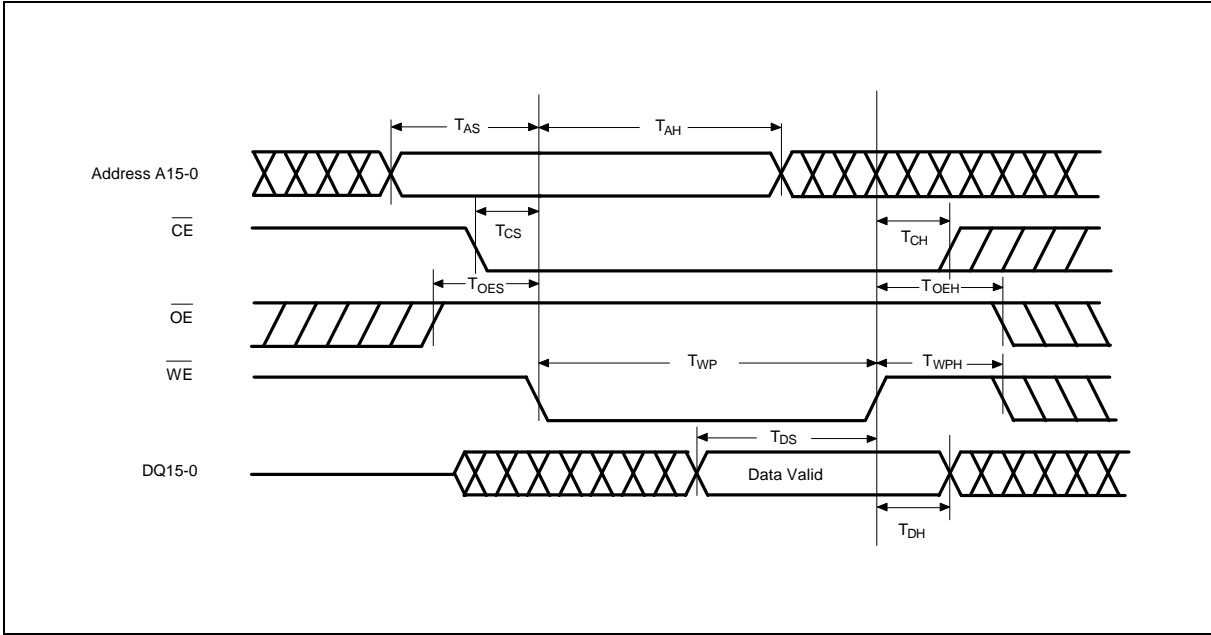
$\overline{\text{CE}}$ Controlled Command Write Cycle Timing Diagram
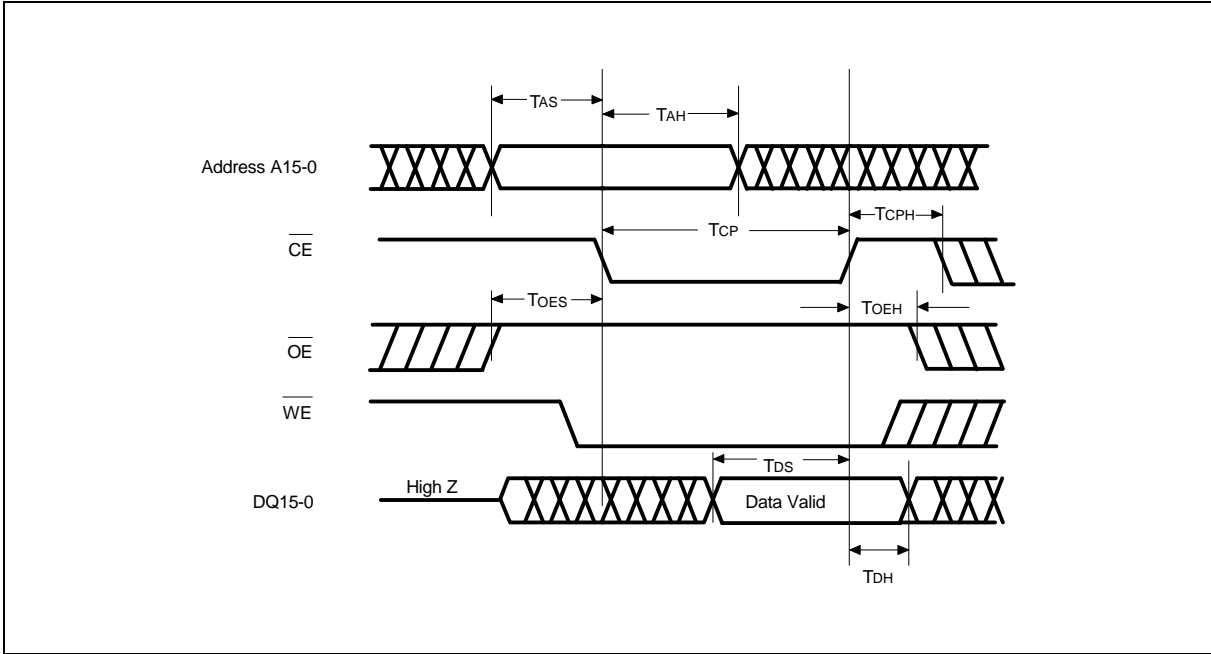
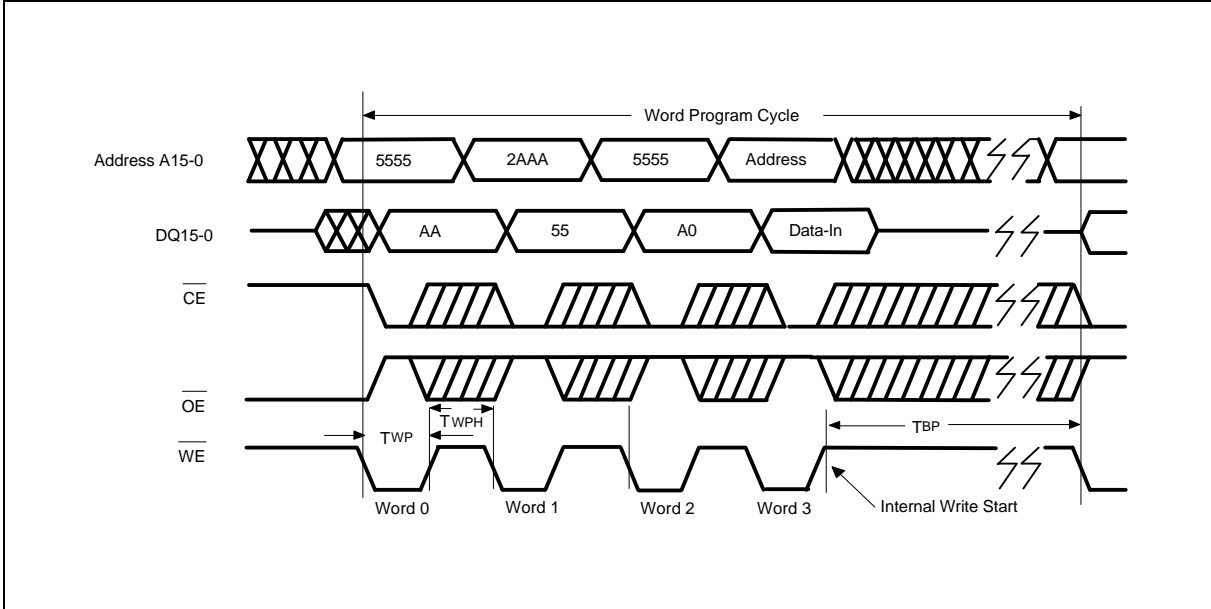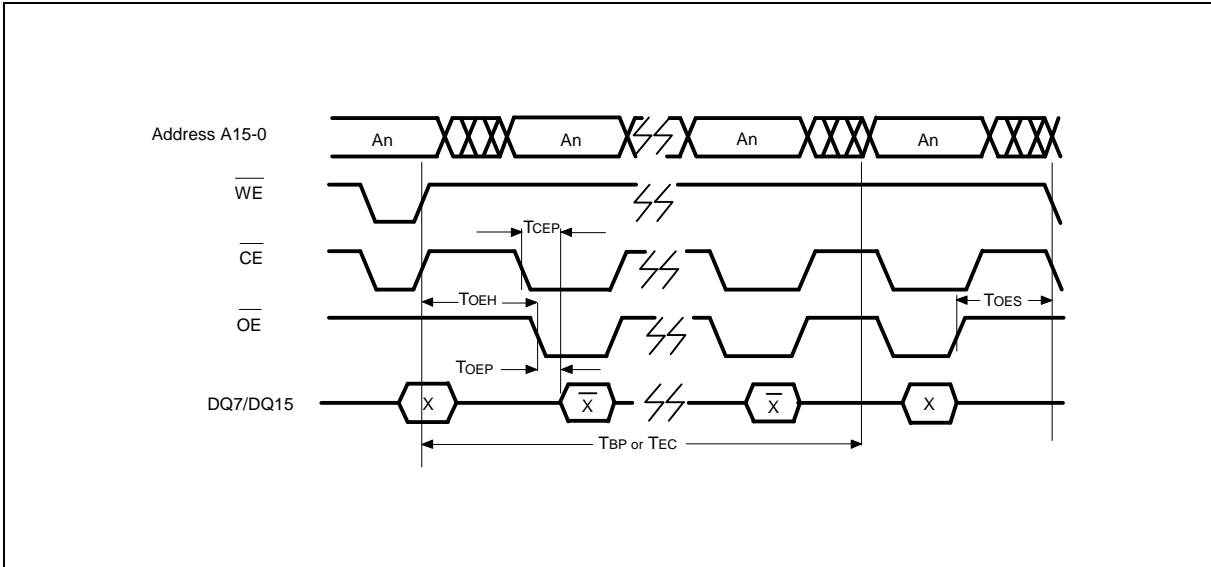Timing Waveforms, continued

Program Cycle Timing Diagram

DATA Polling Timing Diagram

Timing Waveforms, continued
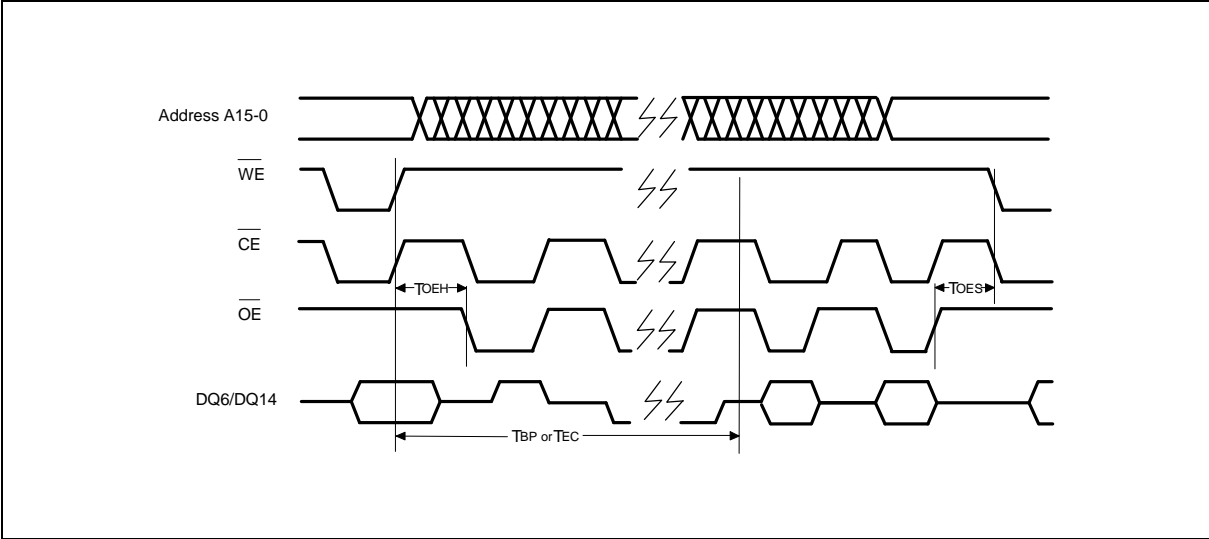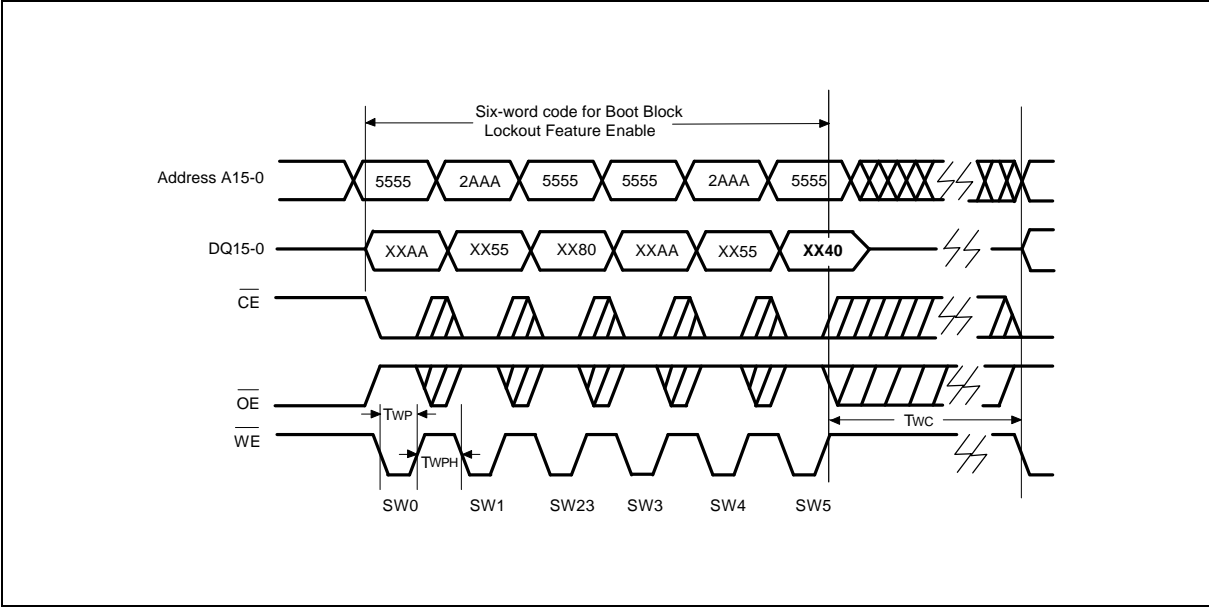
Toggle Bit Timing Diagram
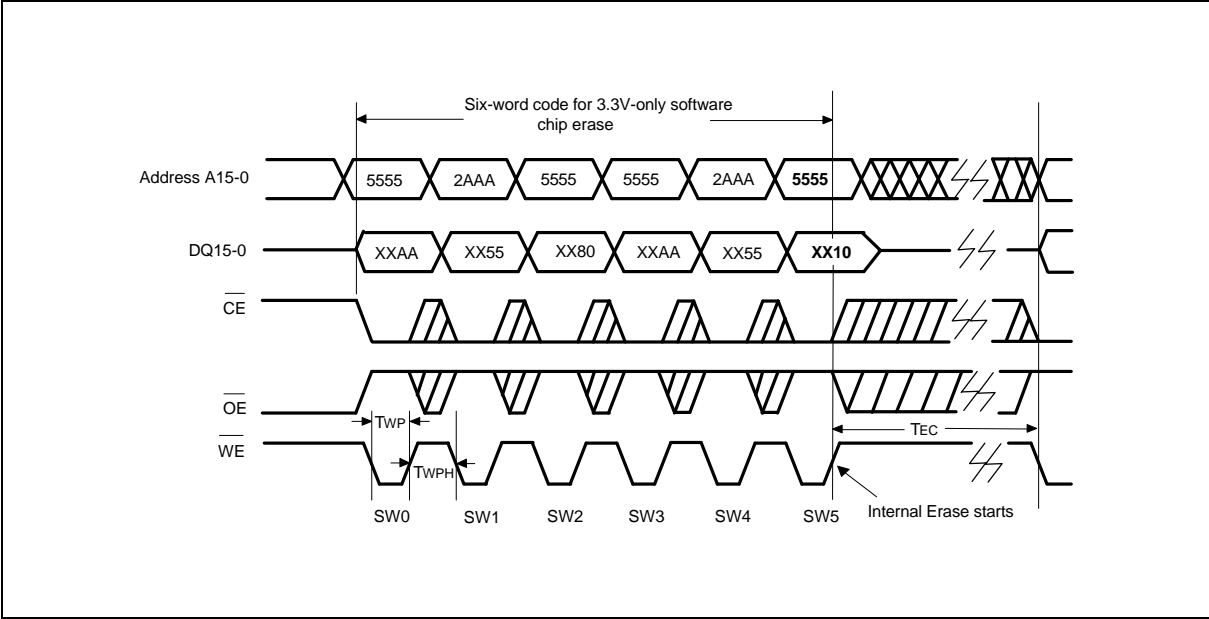

Boot Block Lockout Enable Timing Diagram
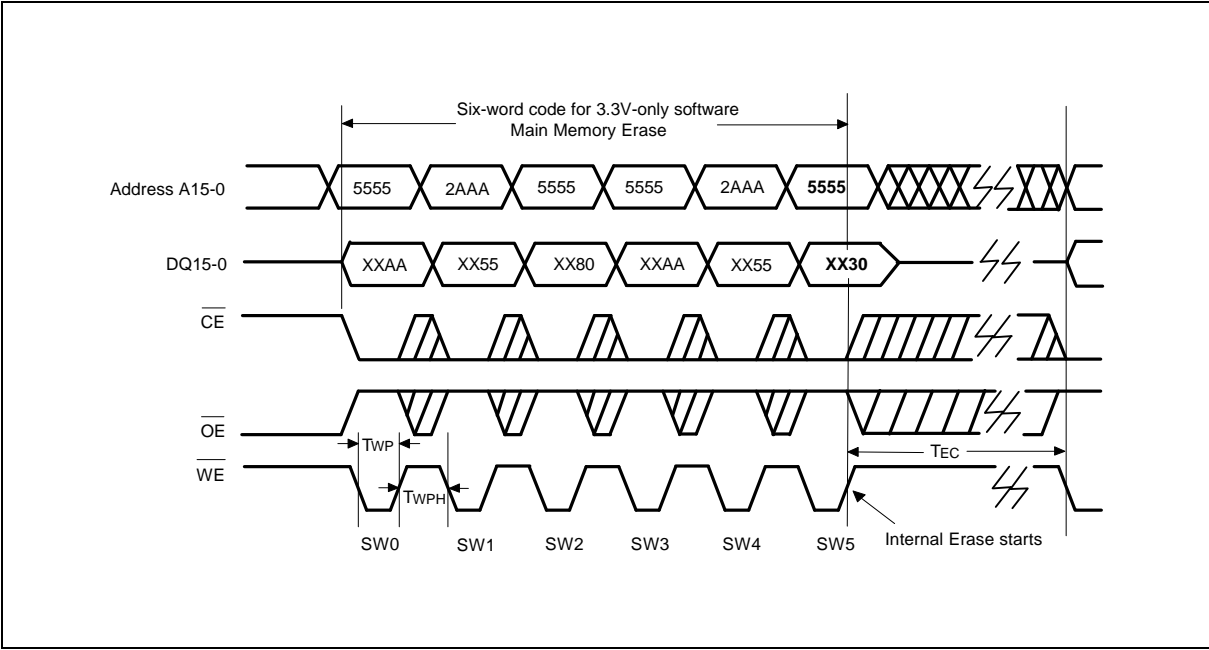
Timing Waveforms, continued

Chip Erase Timing Diagram

Main Memory Erase Timing Diagram

ORDERING INFORMATION

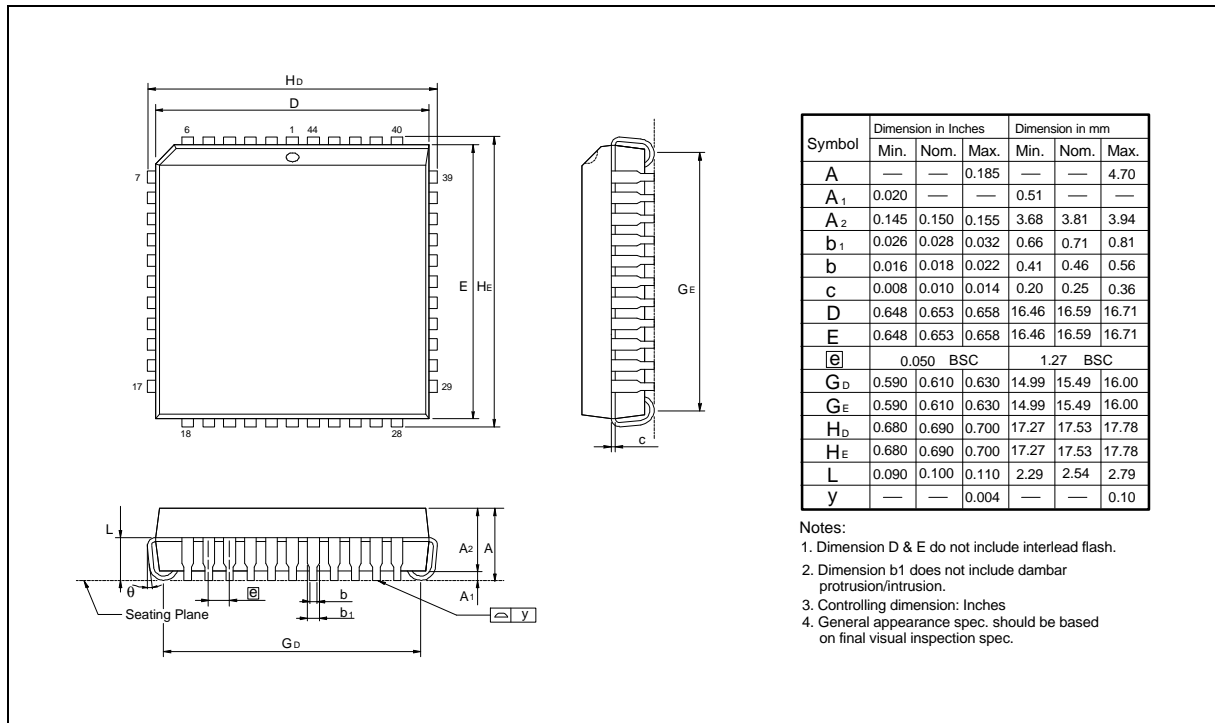| PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V$_{DD}$ CURRENT MAX. (mA)	PACKAGE	CYCLE
W29N102CQ-55	55	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	1K
W29N102CQ-70	70	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	1K
W29N102CQ-90	90	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	1K
W29N102CP-55	55	25	50 (CMOS)	44-pin PLCC	1K
W29N102CP-70	70	25	50 (CMOS)	44-pin PLCC	1K
W29N102CP-90	90	25	50 (CMOS)	44-pin PLCC	1K
W29N102CQ-55B	55	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	10K
W29N102CQ-70B	70	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	10K
W29N102CQ-90B	90	25	50 (CMOS)	40-pin TSOP (10 mm × 14 mm)	10K
W29N102CP-55B	55	25	50 (CMOS)	44-pin PLCC	10K
W29N102CP-70B	70	25	50 (CMOS)	44-pin PLCC	10K
W29N102CP-90B	90	25	50 (CMOS)	44-pin PLCC	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.

2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

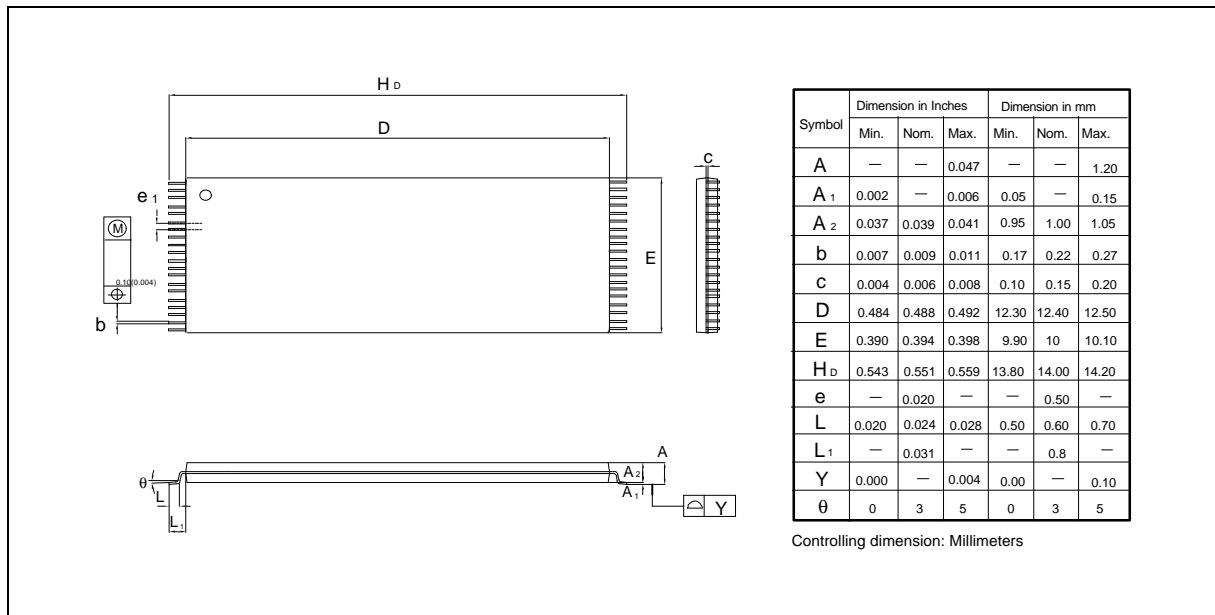## 44-pin PLCC

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A1	0.020	—	—	0.51	—	—
A2	0.145	0.150	0.155	3.68	3.81	3.94
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
GD	0.590	0.610	0.630	14.99	15.49	16.00
GE	0.590	0.610	0.630	14.99	15.49	16.00
HD	0.680	0.690	0.700	17.27	17.53	17.78
HE	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

40-pin TSOP (10 mm · 14 mm)

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.484	0.488	0.492	12.30	12.40	12.50
E	0.390	0.394	0.398	9.90	10	10.10
HD	0.543	0.551	0.559	13.80	14.00	14.20
e	—	0.020	—	—	0.50	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L1	—	0.031	—	—	0.8	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Feb. 1999	-	Initial Issued