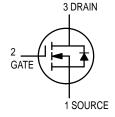
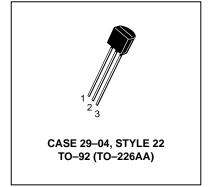
TMOS FET Transistor

N-Channel — Enhancement



VN2222LL Motorola Preferred Device



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	60	Vdc
Drain–Gate Voltage (R _{GS} = 1.0 M Ω)	V _{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	I _D	150 1000	mAdc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	TL	300	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			•	•
Drain–Source Breakdown Voltage (V _{GS} = 0, I _D = 100 μAdc)	V(BR)DSS	60	_	Vdc
Zero Gate Voltage Drain Current $(V_{DS} = 48 \text{ Vdc}, V_{GS} = 0)$ $(V_{DS} = 48 \text{ Vdc}, V_{GS} = 0, T_J = 125^{\circ}\text{C})$	I _{DSS}	_	10 500	μAdc
Gate–Body Leakage Current, Forward (VGSF = 30 Vdc, VDS = 0)	l _{GSSF}	_	-100	nAdc
ON CHARACTERISTICS(1)	•			
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0 mAdc)	VGS(th)	0.6	2.5	Vdc
Static Drain–Source On–Resistance ($V_{GS} = 10 \text{ Vdc}$, $I_{D} = 0.5 \text{ Adc}$) ($V_{GS} = 10 \text{ Vdc}$, $I_{D} = 0.5 \text{ Vdc}$, $T_{C} = 125^{\circ}\text{C}$)	^r DS(on)	_ _	7.5 13.5	Ω

^{1.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1



VN2222LL

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS ⁽¹⁾ (Continued)					
Drain-Source On-Voltage (V _{GS} = 5.0 Vdc, I _D = 200 mAdc) (V _{GS} = 10 Vdc, I _D = 500 mAdc)		VDS(on)	_ _	1.5 3.75	Vdc
On–State Drain Current $(V_{GS} = 10 \text{ Vdc}, V_{DS} \ge 2.0 \text{ V}_{DS}(on)$))	I _{D(on)}	750	_	mA
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 500 mAdc)		9fs	100	_	μmhos
DYNAMIC CHARACTERISTICS		•			
Input Capacitance		C _{iss}	_	60	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz})$	C _{oss}	_	25	
Reverse Transfer Capacitance	,	C _{rss}	_	5.0	
SWITCHING CHARACTERISTICS ⁽¹⁾					
Turn-On Delay Time	(V _{DD} = 15 Vdc, I _D = 600 mA,	ton	_	10	ns
Turn-Off Delay Time	$R_{gen} = 25 \Omega, R_L = 23 \Omega$	t _{off}	_	10	

^{1.} Pulse Test: Pulse Width $\leq 300~\mu s$, Duty Cycle $\leq 2.0\%$.

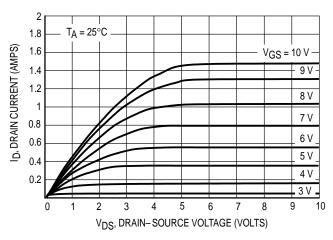


Figure 1. Ohmic Region

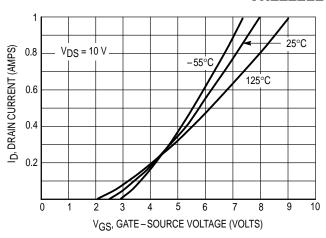


Figure 2. Transfer Characteristics

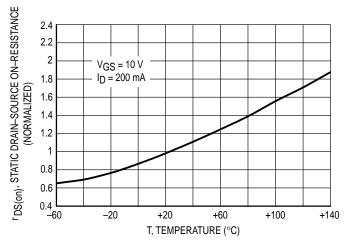


Figure 3. Temperature versus Static Drain–Source On–Resistance

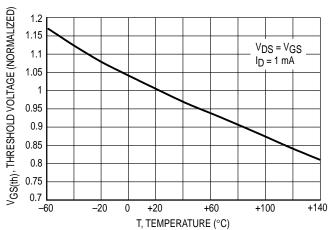
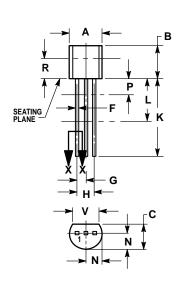


Figure 4. Temperature versus Gate Threshold Voltage

PACKAGE DIMENSIONS



SECTION X-X

CASE 029-04 (TO-226AA) **ISSUE AD**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.

 DIMENSION F APPLIES BETWEEN P AND L.
- DIMENSION D AND J APPLY BETWEEN L AND K
 MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.175	0.205	4.45	5.20
В	0.170	0.210	4.32	5.33
С	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
Н	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500		12.70	
L	0.250		6.35	
N	0.080	0.105	2.04	2.66
Р		0.100		2.54
R	0.115		2.93	
V	0 135		3 43	

STYLE 22:

PIN 1. SOURCE

2 GATE

3. DRAIN

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