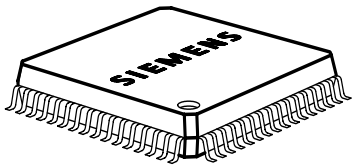
Carradio IC
FM Car Radio IC with PLL

TUA 4401

Specification **B6CA**

1 Features

- Double balanced RF mixer with low noise figure, high IP3 and wide dynamic range
- Strictly symmetrical RF circuitry
- IF amplifier with adjustable gain
- 7 stage limiter amplifier with dB linear field-strength output
- Low distortion coincidence demodulator
- Multipath detector with analog output
- CMOS PLL-Synthesizer
- Resolution between 100 kHz and 6.25kHz
- Search tuning stop with IF counter and Fieldstrength/Multipath evaluation
- ADC's for fieldstr. and Multipath detector
- SOCCAR Bus
  I^2C Bus and 3 Wire Bus operation possible



MQFP 64

Package

2 Ordering Information

Type	Ordering Code	Package
TUA 4401		MQFP-64

3 General Description

The TUA 4401 is the first Infineon Carradio IC using BICMOS technology.
The combination of an analog FM receiver circuit and a digital PLL synthesizer on the same chip reduces the over all pin count in comparision to two separate IC's and in addition the number of necessary external components. This gives the flexibility both for high performance and low cost applications.
The recommended applications for this device are FM only carradios and background receivers, capable for all world standards.

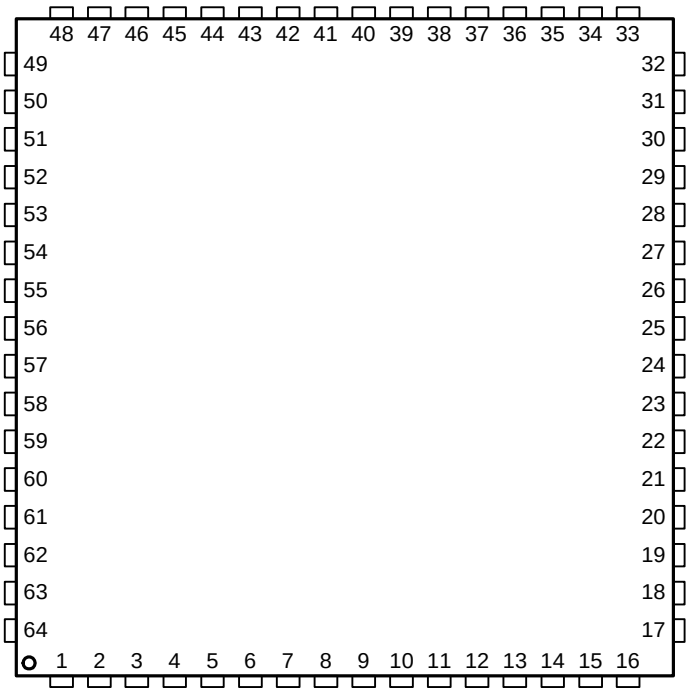
TUA 4401 features:

Frontend
- High level, high impedance mixer input with improved dynamic range
- High input / output 3rd order intercept point
- Integrated prestage AGC generation and control for PIN diodes and MOS tetrode
- Bus controlled AGC threshold
- 2 pin 1st local oscillator with improved low phase noise, internally coupled to PLL
- Strictly symmetrical RF parts
- PLL with fast acquisition mode
- Resolution 100 kHz, 50 kHz, 25 kHz, 12,5 kHz, 10 kHz and 6.25 kHz
- High running (61.5 MHz) crystal oscillator to avoid interference with bus controlled adjustment

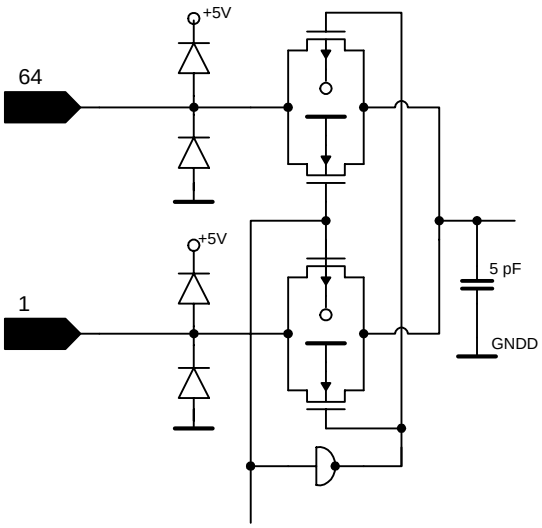
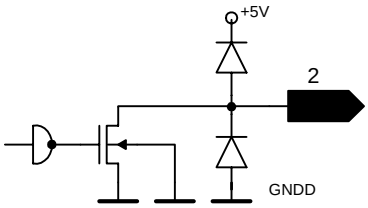
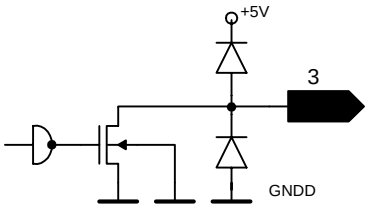
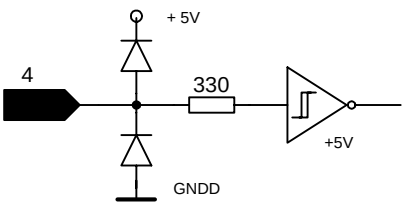
IF amplification, demodulation and STS
- Low noise IF amplifier
- Gain adjust with DC control voltage or serial bus possible
- 7 stage IF limiter with extended fieldstrength range suitable for the IF frequency range of 10.7 MHz ... 21.4 MHz
- Fieldstrength DC output and ADC output available
- Low distortion coincidence demodulator (using short loop AFC principle) with MPX output
- Soft mute for weak signal conditions with adjustable bus controlled mute depth
- Multipath detector with high pass filter, analog output and ADC output
- IF counter for search tuning stop with selectable IF center frequency and window width
- STS informations -in window-,-below-,-beyond- available

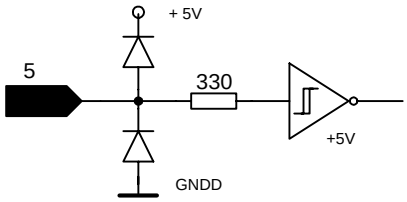
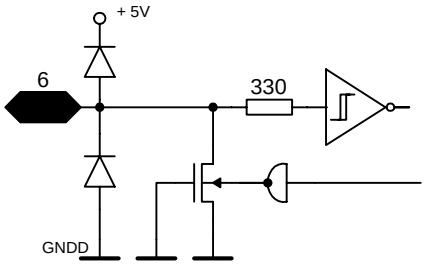
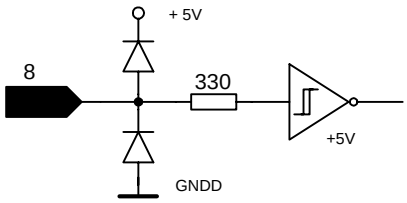
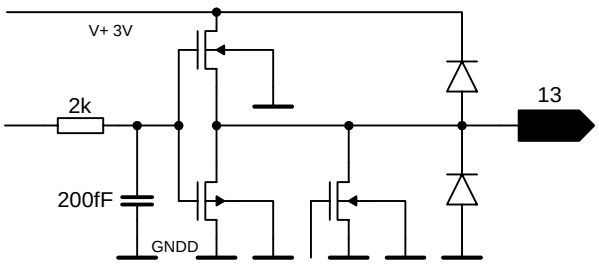
SOCCAR Bus (Siemens **O**ne **C**hip **CA**r **R**adio **Bus)**
- I^2C bus (2 wire, fast mode device with 400 kbit/s) and 3 Wire bus (3 or 4 wire) operation possible
- Bus interface with low threshold voltage Schmitt-Trigger inputs for interfacing 3V or 5V microprocessors

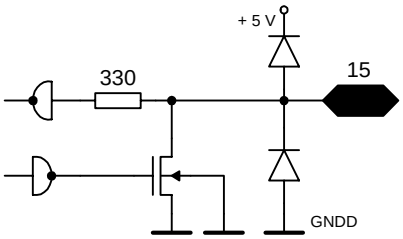
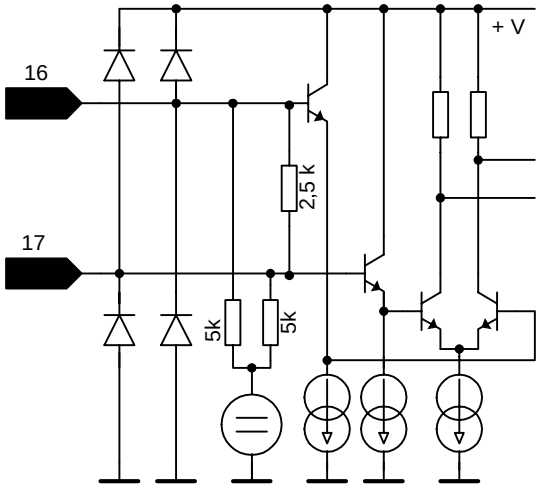
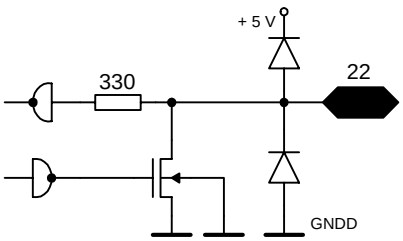
4 Pin Configuration

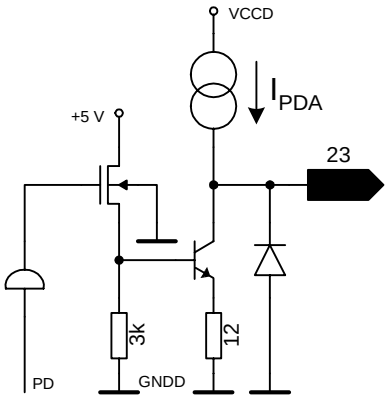
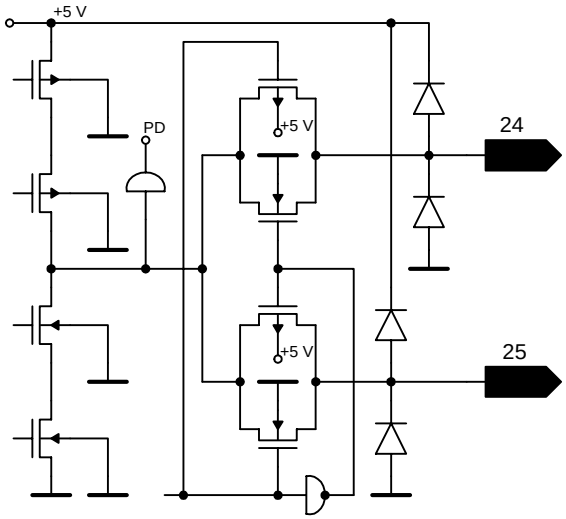
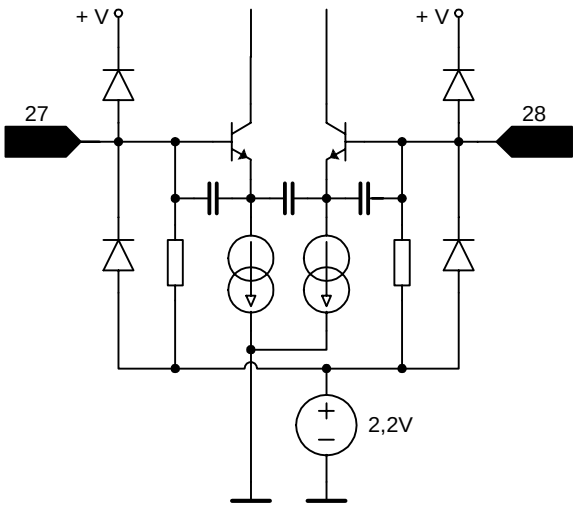


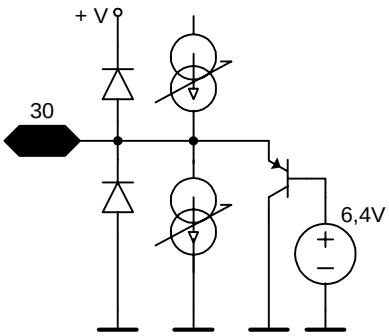
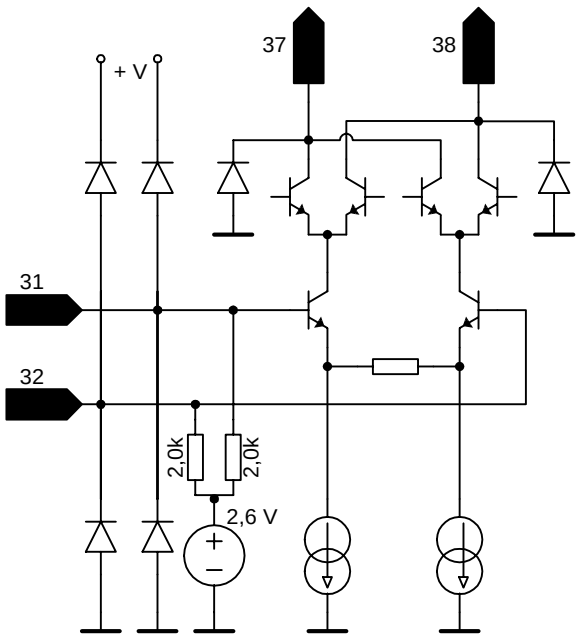
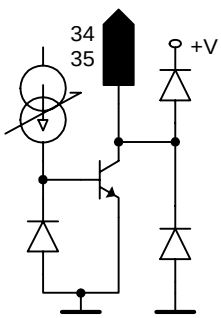
5 Pin Definitions and Functions

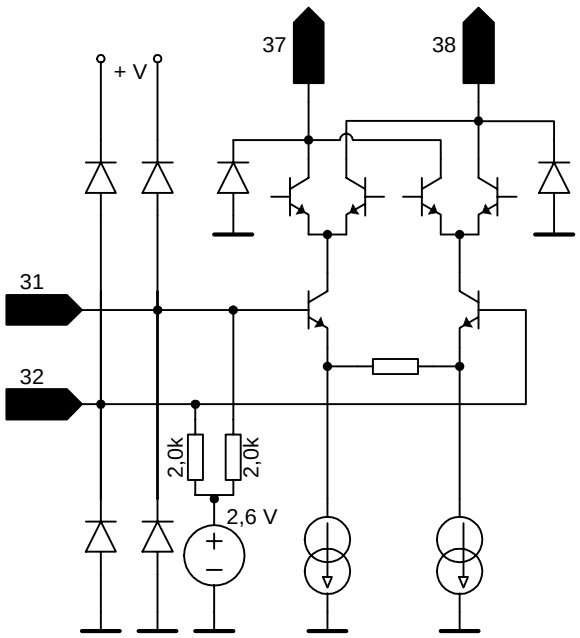
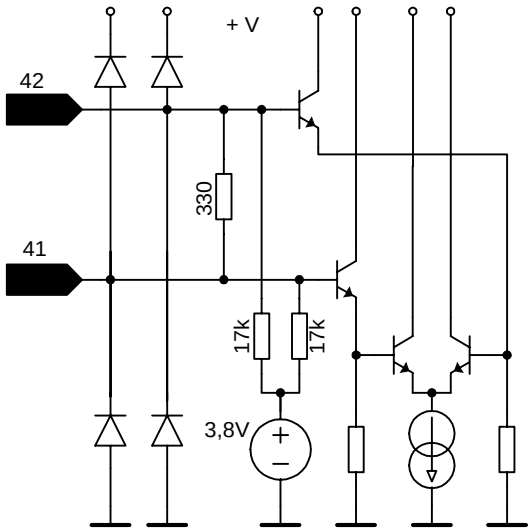
Pin No.	Symbol		Function
1 64	MP_ADC FS_ADC		1: ADC input multipath detector 64: ADC input fieldstrength
2	IF_CENT		2: IF counter output IF center
3	IF_WINDOW		3: IF counter detect output (below beyond window)
4	BUS_MODE		4: SOCCAR bus select input (I^2C or 3 Wire mode)

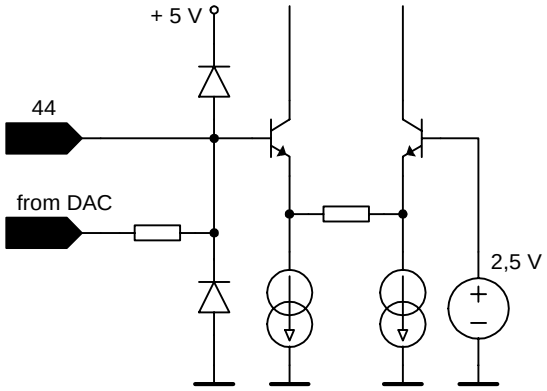
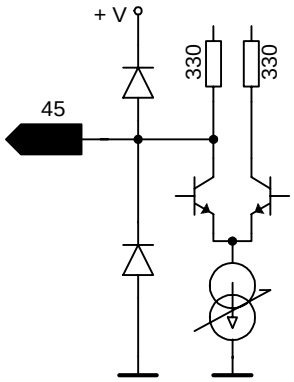
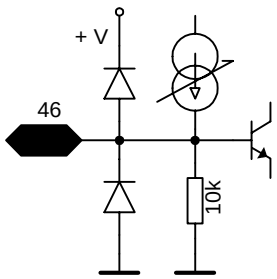
5	SCL		5: SOCCAR bus clock input
6	SDA		6: SOCCAR bus data in/output (I^2C mode), data input (3 Wire mode)
7	NC		7: not connected
8	BUS_ENA		8: SOCCAR bus enable input
9	NC		9: not connected
10	VREFD5V		10: Reference voltage digital section (5V)
11	VREFD3V		11: Reference voltage digital section (3V)
12	NC		12: not connected
13	XTAL_DIV6		13: Crystal oscillator auxiliary output (10.25 MHz)
14	NC		14: not connected

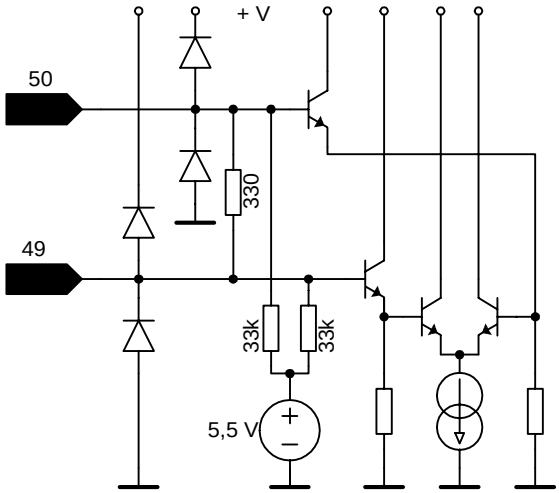
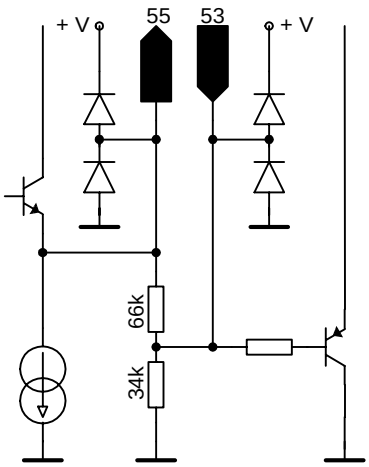
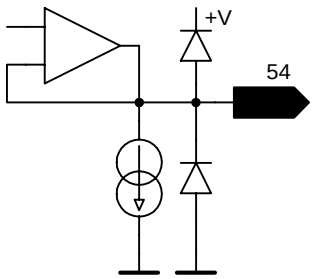
15	PORT_2		15: Switch port output 2(open drain)
16 17	QUARTZ1 QUARTZ2		16: Reference oscillator input / Crystal 17: Reference oscillator input / Crystal
18	VCCD		18: Positive power supply voltage for serial bus und synthesizer
19	GNDD		19: Ground for serial bus und synthesizer
20	NC		20: Not connected
21	NC		21: Not connected
22	PORT_1		22: Switch port output 1 (open drain)

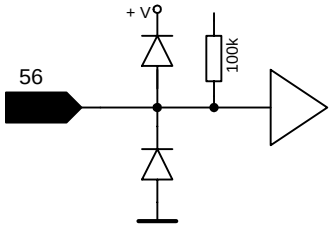
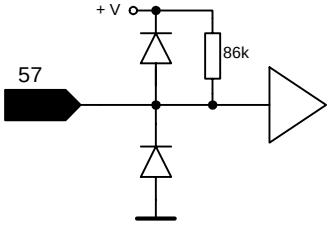
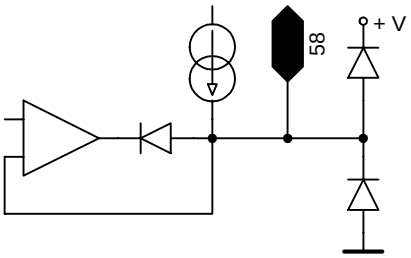
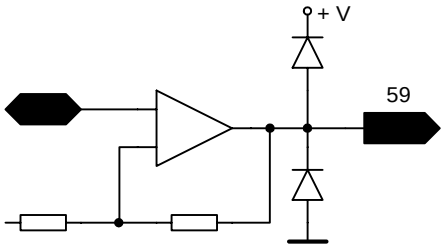
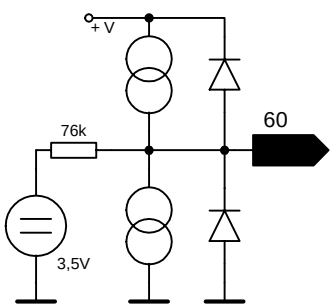
23	PDA		23: PLL phasedetector output analog (Tuningvoltage)
24 25	PD_0 PD_1		24: PLL chargepump output 0 (Phase detector tristate chargepump output) 25: PLL chargepump output 1 (Phase detector tristate chargepump output)
26	GNDRF		26: Ground for RF part
27 28	OSC1 OSC2		27: 1st local oscillator circuit 28: 1st local oscillator circuit
29	VCCRF		29: Positive power supply voltage for RF part

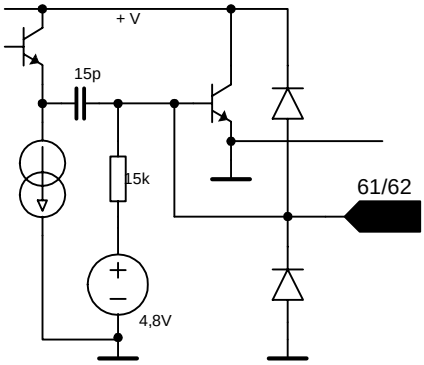
30	PRE_CAP		30: Prestage AGC time constant capacitor; output for MOS tetrode gate 2
31 32	FM1 FM2		31: FM 1st mixer symmetrical input 32: FM 1st mixer symmetrical input
33	NC		33: not connected
34 35	AGCOUNT_N AGCOUNT_P		34: Prestage AGC current output for PIN diode inverse polarity 35: Prestage AGC current output for PIN diode normal polarity
36	NC		not connected

37 38	IF2 IF1		37: 1st mixer output (open collector) 38: 1st mixer output (open collector)
39	VREFRF		39: Reference voltage RF section (4.8V)
40	GNDIF1		40: Ground for IF amplifier
41 42	IFINFM IFIN		41: 10.7 MHz IF amplifier input 42: 10.7 MHz IF amplifier operation point
43	VREFIF		43: Reference voltage IF section (4.8V)

44	IFAMPG		44: 10.7 MHz IF amplifier DC gain control adjust, over-write of DAC
45	IFOUTFM		45: 10.7 MHz IF amplifier out-put
46	IFAMPC		46: 10.7 MHz IF amplifier DC gain control adjust block-ing capacitor
47	VCCIF		47: Positive power supply voltage for IF amplifier
48	NC		48: not connected

49 50	FMIFIN FMIFBIAS2		49: FM limiter input 50: FM limiter input bias decoupling cpacitor
51	GNDIF2		51: Ground for limiter amplifier
52	NC		52: not connected
53 55	MUTE FSOUT		53: Dynamic soft mute control blocking capacitor 55: Fieldstrength output
54	MPXOUT		54: FM MPX signal output

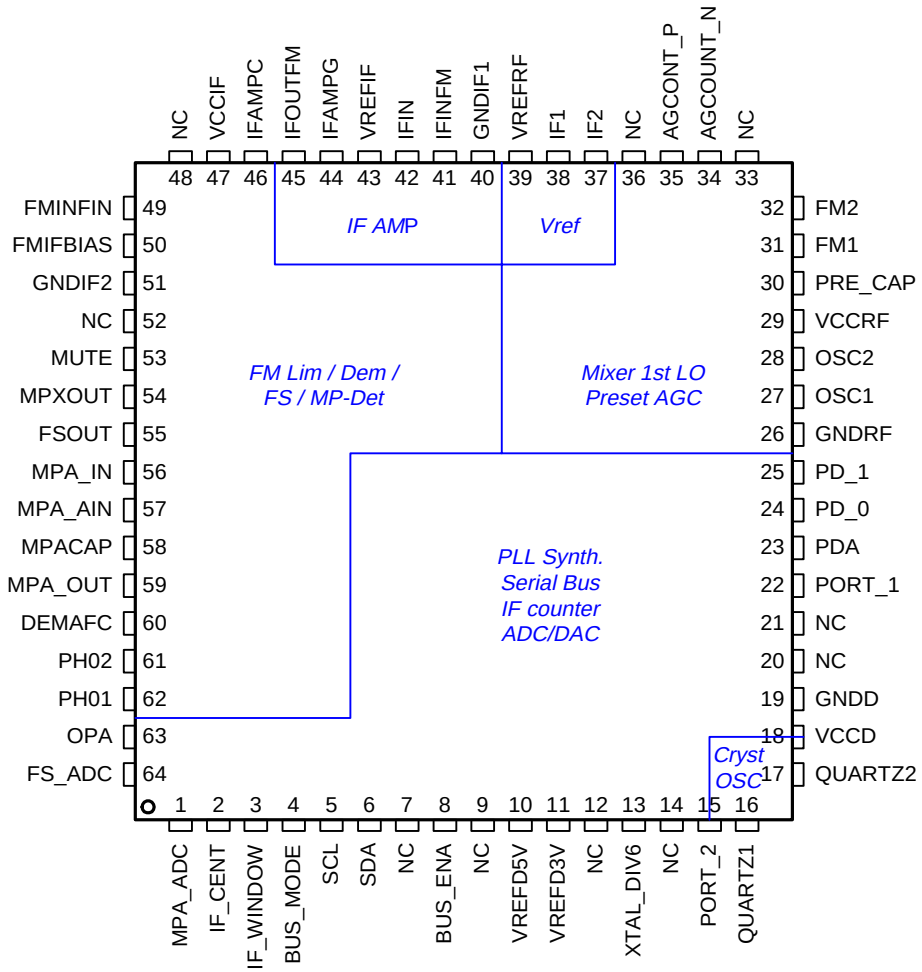
56	MPA_IN		56: Multipath detector high-pass filter input
57	MPA_AIN		57: Multipath detector auxiliary input
58	MPACAP		58: Multipath detector rectifier capacitor
59	MPA_OUT		59: Multipath detector output
60	DEMAFC		60: Demodulator AFC blocking capacitor

61 62	PH02 PH01		61: Demodulator circuit 62: Demodulator circuit
63	OPA		Test pin

6 Applications

- FM only car radio receiver, background receiver

7 Block Diagram



8 Circuit Description

The TUA 4401 is a one chip FM car radio system consisting of RF frontend, gain adjustable IF amplifier, FM-IF limiter amplifier, demodulator, PLL synthesizer, IF counter for STS and ADC's for fieldstrength and multipath detector.The serial bus is switchable between I^2C and 3 Wire bus mode.

8.1 FM frontend

The frontend consists of a two pin varactor tuned oscillator, a double balanced mixer and a prestage AGC control circuit. The mixer has an improved intermodulation behaviour and convertes the RF signal to the 10,7 MHz IF range. Two inputs allow both symmetrical and unsymmetrical operation. The integrated AGC stage for prestage control drives MOSFETS as well as PIN diodes with current drivers for normal and inverse polarity. The AGC threshold can be set with aserial bus controlled 2 Bit DAC.

8.2 FM IF amplifier

After the mixer an IF amplifier is present for IF post amplification. Input and output impedance are both 330 Ohms for matching with ceramic filters. For adjusting the over all gain the IF amplifier gain can be adjusted with a serial bus controlled 4 Bit DAC. The DAC output is available at a pin and can be overwritten by an external control voltage for a not bus controlled gain adjust.

8.3 FM limiter and demodulator

The FM IF amplifier includes a seven stage capacitive coupled limiter amplifier and a fieldstrength generator with high linearity and increased dynamic range.
The coincidence demodulator has an additional AFC short loop circuit with integrated varactor diode in parallel to the external tank circuit to improve the distortion bahaviour in case of detuning.
For decreasing noise a soft mute circuit is available. Noise can be continueasly decreased controlled by the fieldstrength value. Mute depth is adjustable with a serial bus controlled 7 bit DAC. The adjustment range includes a full mute feature.

8.4 Multipath detector

A multipath detector with analog output is available. Its input signal is fed through a 200 kHz 2nd order highpass filter and a 80 kHz 1st order highpass filter.

8.5 A/D converter for fieldstrength and multipath detector

The 7 bit A/D converter has two input channels and works as successive approximation converter. The conversion time for both input signals is t = 32 µs. The 7-bit digital-words from both channels (14 bit) are read out together via bus into two bytes with the read subadress 82H.
The input voltage range for both channels is 0...VREFD5V.

8.6 IF counter and multipath/fieldstrength evaluation for STS

FM center frequencies ar available in two ranges set by bit D7 in subaddress 05H.
For D7=1 the range of centerfrequency is 20.800 MHz...22.3875 MHz in 128 steps (12.5 kHz per step). For D7=0 the range of centerfrequency is 10.400 MHz...11.1937 MHz in 128 steps (6.25 kHz per step).
The gate time is adjustable in 8 steps from 320us...40.96ms and the tolerance of the accepted count value, the window is adjustable in 5 steps from +/- (6.25kHz...100kHz) for D7=0 in sub-address 05H and +/- (12.5 kHz...200 kHz) for D7=1 in subaddress 05H. The results IF_CENT and IF_WINDOW are read out via bus (read-subadress 82H) or pin IF_CENT.
If the IF frequency is into the preselected window, IF_CENT goes from high to low level.
If the IF frequency is outside the preselected window, IF_CENT is high. The bit IF_WINDOW is a hint IF-frequency that is to low (IF_WINDOW=high) or is to high (IF_WINDOW=low).
In addition to the frequency measurement, thresholds for multipath and fieldstrength voltages can be programmed via bus (subaddress 0BH). IF_CENT will only go to low level in case of field-strength and multipath voltages are beyond the thresholds and the frequency is inside the window. When setting the thresholds to zero multipath and fieldstrength evaluation is disabled.

8.7 Crystal oscillator

A master crystal oscillator provides all necessary clock frequencies for the whole IC. A 61.5 MHz crystal is used in 3rd harmonic mode.
The oscillator frequency can fine tuned with a serial bus controlled 4 bit D/A converter.
The crystal frequency is used as reference frequency for the PLL oscillator and IF counter. It is also used as clock for the ADC's. Finally the crystal frequency divided by 6 (10.25 MHz) is available at a pin as low pass filtered voltage, it can be disabled with the serial bus.

8.8 Output ports

PORT_1 / 2 are NMOS Open drain outputs.

8.9 SOCCAR Bus

The TUA4401 supports the I^2C bus protocol (2 wire) or 3 Wire bus protocol (3 or 4 wire) operation selectable by pin 4: BUS_MODE (I^2C=low, 3W=high). All bus pins (BUS_MODE, SCL, SDA, BUS_ENA) are Schmitt-triggered input buffer for 3V or 5V µC.
The bit stream begins with the most significant bit (MSB), is shifted in (write mode) on the low to high transition of CLK and is shifted out (read mode) on the high to low transition of CLK.

I^2C bus mode

In this mode pin4 (BUS_MODE) = low and pin8 (BUS_ENA)=low. In this mode SDA is a bidirectional input / output pin.

Data Transition:

Data transition on the pin SDA must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as start or stop condition.

Start Condition (STA):

A start condition is defined by a high to low transition of the SDA line while SCL is at a stable high level.This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):

A stop condition is defined by a low to high transition of the SDA while the SCL line is at a stable high level. This condition terminate the communication between the devices and forces the bus interface into the initial conditions.

Acknowlage (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to low level to indicate it has receive the 8 bits of data correctly.

Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition, followed by the 8bit chip address (write). The chip address for the TUA 4401 is fixed as "1100110" (MSB at first). The last bit (LSB=A0) of the chip address byte defines the typ of operation to be performed:
A0=1, a read operation is selected and A0=0, a write operation is selected. After this comparision the TUA 4401 will generate an ACK.
After this device addressing the desired sub address byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H...07H,0BH) is transmitted first. At the end of data transition the master must be generate the stop condition.

Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition, followed by the 8bit chip address (write: A0=0), followed by the sub address read (82H or 83H), followed by the chip address (read: A0=1). After that procedure the 16bit data register 82H or the 8bit data register 83H is read out. After the first 8 bit read out, the uP mandatory send LOW during the ACK-clock. After the second 8 bit read out the uP mandatory send HIGH during the ACK-clock.
At the end of data transition the master must be generate the stop condition.

3W bus mode

In this mode pin4 (BUS_MODE) =high. Pin6 (SDA) is in this mode a bidirectional input / output. Pin8 (BUS_ENA) is used to activate the bus interface to allow the transfer of data (SDA) to / from the device. When BUS_ENA is in an inactive high state, shifting is inhibited. Data Transition: Data transition on the pin SDA must only occur when the clock SCL is low. To transfer data to / from the device, BUS_ENA (which must start inactive high) is taken low, a serial transfer is made via SDA, DOUT and CLK and BUS_ENA is taken back high. The bit stream needs neither the chip address.

Data Transfer Write Mode:

To start the communication, the BUS_ENA is taken low. The desired sub address byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H...07H,0BH) is transmitted first. At the end of data transition the BUS_ENA must be high.

Data Transfer Read Mode:

To start the communication in the read mode, the BUS_ENA is taken low, followed by the sub address read (82H). After that the device is ready to read out the 16bit data register 82H. At the end of data transition the BUS_ENA must be high.

8.10 PLL Synthesizer

R / N Counter

The TUA 4401 has 2 identical 16bit counter for R and N path. Input frequency for the R-counter is the buffered XTAL-frequency (61.5MHz). Tuning steps can be selected by the 16bit R-counter from f_R= 6.25kHz...100kHz. Input frequency for the N-counter is the buffered LO-frequency (in FM mode 98.2MHz...118.7MHz).

Three State Phase Comparator

The phase comparator generates a phase error signal according to phase difference between f_R (R counter output) and f_N (N counter output).This phase error signal drives the charge pump current generator. Polarity is fixed positiv for this application note.

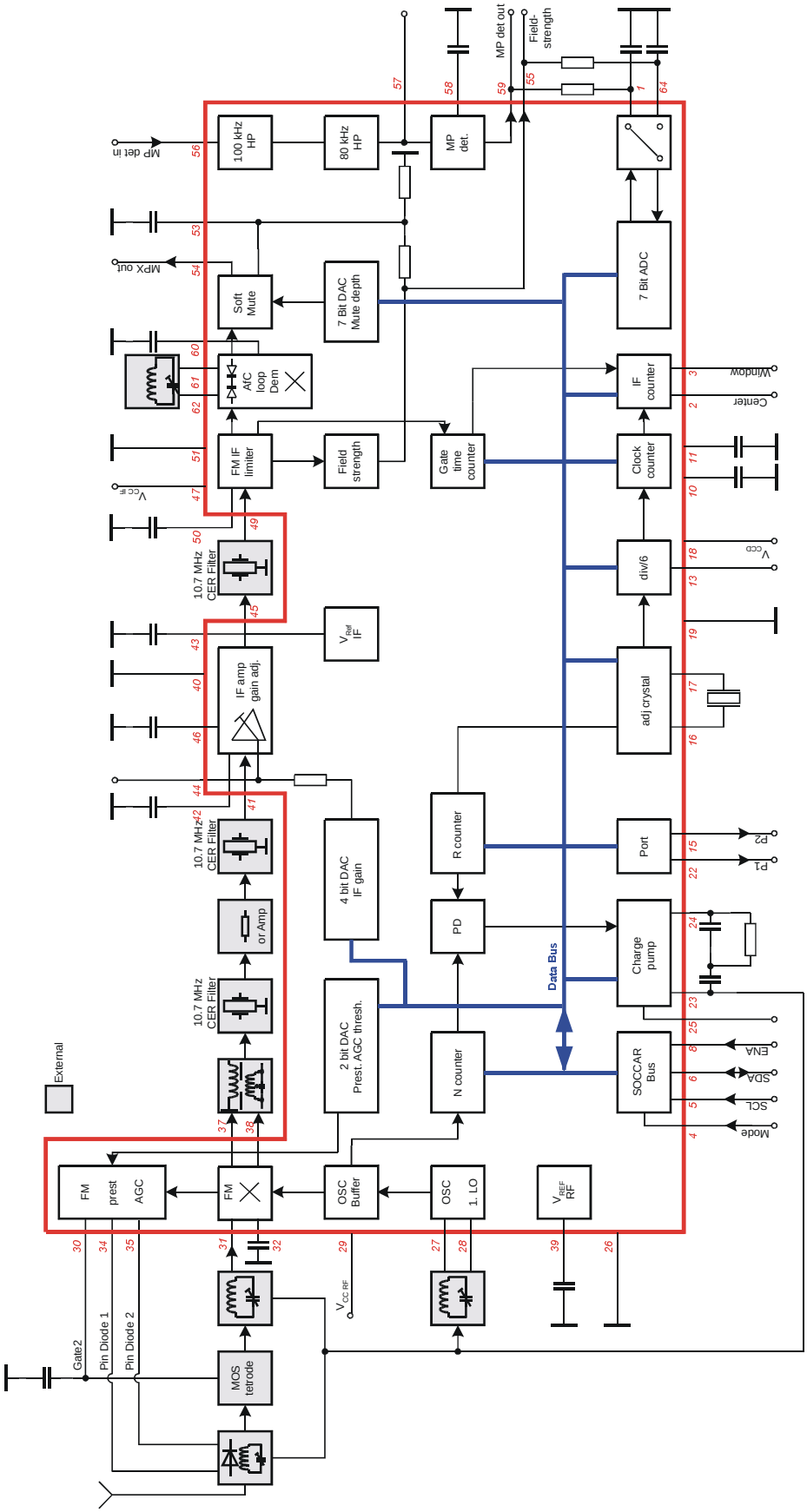
Charge Pump

The charge pump generates signed pulses of current. 4 current values and 2 outputs are available.

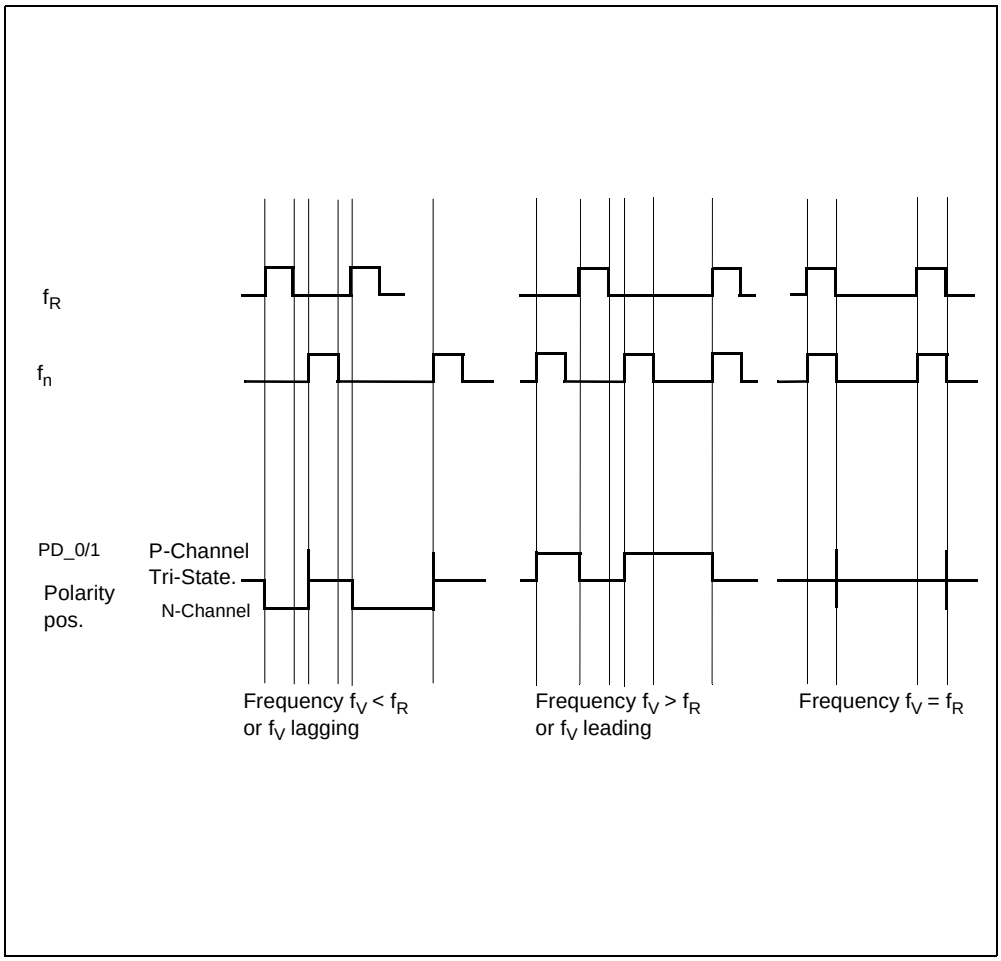
Loop Amp

The integrated rail to rail loop amplifier allows an active loop filter design with external components. Two modes are avialiable with status bit D11: high speed and normal mode.

8.11 Functional Block Diagram



8.12 Phase detector outputs



8.13 Bus Interface

Pin Function

Pin name	BUS_MODE	BUS_ENA	SCL	SDA
Function	Bus mode select	Enable	Serial clock	Serial data
I2C-mode	Low	High=Inactiv Low=Activ	Clock input	Data in / out
3Wire mode	High			Data in

8.13.1 Bus Data Format

I²C Bus Write Mode

	MSB	CHIP ADDRESS (WRITE)					LSB		MSB	SUB ADDRESS (WRITE) 00H...07H, 0BH							LSB		MSB	DATA IN X...0 (X=7 or 15)						LSB		
STA	1	1	0	0	1	1	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	DX	...	D5	D4	D3	D2	D1	D0	ACK	STO

I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)					LSB		MSB	SUB ADDRESS (READ) 82H, 83H							LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	0	0	1	1	0	0	ACK	1	0	0	0	0	0	1	0	ACK	STA	1	1	0	0	1	1	0	1	ACK

MSB	DATA OUT FROM SUB ADD 82H						LSB		MSB	DATA OUT FROM SUB ADD 82H, 83H							LSB		
R15	R14	R13	R12	R11	R10	R9	R8	ACK[1)]	R7	R6	R5	R4	R3	R2	R1	R0	ACK[2)]	STO

1): mandatory LOW send by uP, 2): mandatory HiGH send by uP

3W Bus Write Mode

MSB	SUB ADDRESS (WRITE) 00H...07H, 0BH						LSB	MSB	DATA IN X...0 (X=7 or 15)						LSB
S7	S6	S5	S4	S3	S2	S1	S0	DX	...	D5	D4	D3	D2	D1	D0

3W Bus Read Mode

MSB	SUB ADDRESS (READ) 82H, 83H						LSB	MSB	DATA OUT FROM SUB ADD 82H (MSB)							LSB	MSB	DATA OUT FROM SUB ADD 82H (LSB) / 83H (LSB)							LSB
1	0	0	0	0	0	1	0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

Chipaddress Organisation

Chip Address (only I²C mode)								
MSB							LSB	Function
1	1	0	0	1	1	0	0	Chip Address Write
1	1	0	0	1	1	0	1	Chip Address Read

Subaddress Organisation

Sub Addresses of Data Registers Write									
MSB	Bin						LSB	Hex	Function
0	0	0	0	0	0	0	0	00H	Status
0	0	0	0	0	0	0	1	01H	R_Counter
0	0	0	0	0	0	1	0	02H	N_Counter
0	0	0	0	0	0	1	1	03H	Mute_DAC7
0	0	0	0	0	1	0	0	04H	IF_COUNT_P1
0	0	0	0	0	1	0	1	05H	IF_COUNT_P2
0	0	0	0	0	1	1	0	06H	Specials
0	0	0	0	0	1	1	1	07H	Gain_DAC4
0	0	0	0	1	0	1	1	0BH	COMP_PRESET

Sub Address of Data Register Read									
MSB	Bin						LSB	Hex	Function
1	0	0	0	0	0	1	0	82H	Result Multipath, Field-strength, IF_Window and IF_Center
1	0	0	0	0	0	1	1	83H	Result-MISC

Data Byte Specification

Status Subaddress 00H	
Bit	Function
MSB D15	not used (must be=0)
D14	Port_2 (0=low, 1=high)
D13	Port_1 (0=low, 1=high)
D12	not used (must be=0)
D11	Loopamp current
D10	not used (must be=0)
D9	not used (must be=0)
D8	not used (must be=0)
D7	ADC_Single
D6	ADC_Mode
D5	ADC_ON
D4	IF_DAC4
D3	PD_select
D2	CP_Current 2
D1	CP_Current 1
D0 LSB	CP_Mode

R_Counter Subaddress 01H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

N_Counter Subaddress 02H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

Results Fieldstrength, Multipath and IF counter Subaddress 82H (read address)	
Bit	Function
MSB D15	IF_window
D14	Multipath_2^{6}
D13	Multipath_2^{5}
D12	Multipath_2^{4}
D11	Multipath_2^{3}
D10	Multipath_2^{2}
D9	Multipath_2^{1}
D8	Multipath_2^{0}
D7	IF_center
D6	Fieldstrength_2^{6}
D5	Fieldstrength_2^{5}
D4	Fieldstrength_2^{4}
D3	Fieldstrength_2^{3}
D2	Fieldstrength_2^{2}
D1	Fieldstrength_2^{1}
D0 LSB	Fieldstrength_2^{0}

Mute_DAC7 Subaddress 03H	
Bit	Function
MSB D7	Enable
D6	MDAC_6
D5	MDAC_5
D4	MDAC_4
D3	MDAC_3
D2	MDAC_2
D1	MDAC_1
D0 LSB	MDAC_0

IF_Count_P1 Subaddress 04H	
Bit	Function
MSB D7	Enable
D6	not used
D5	Win_2
D4	Win_1
D3	Win_0
D2	Gate_2
D1	Gate_1
D0 LSB	Gate_0

IF_Count_P2 Subaddress 05H	
Bit	Function
MSB D7	CF_Mode
D6	CF_6
D5	CF_5
D4	CF_4
D3	CF_3
D2	CF_2
D1	CF_1
D0 LSB	CF_0

Specials Subaddress 06H	
Bit	Function
MSB D7	XTAL_DIV6
D6	VCO_2
D5	AGC_1
D4	AGC_0
D3	XTAL_3
D2	XTAL_2
D1	XTAL_1
D0 LSB	XTAL_0

IF_DAC4 Subaddress 07H	
Bit	Function
MSB D7	not used
D6	not used
D5	not used
D4	not used
D3	GDAC_3
D2	GDAC_2
D1	GDAC_1
D0 LSB	GDAC_0

COMP_PRESET Subaddress 0BH	
Bit	Function
MSB D15	not used
D14	Fieldstrength_2^{6}
D13	Fieldstrength_2^{5}
D12	Fieldstrength_2^{4}
D11	Fieldstrength_2^{3}
D10	Fieldstrength_2^{2}
D9	Fieldstrength_2^{1}
D8	Fieldstrength_2^{0}
D7	not used
D6	Multipath_2^{6}
D5	Multipath_2^{5}
D4	Multipath_2^{4}
D3	Multipath_2^{3}
D2	Multipath_2^{2}
D1	Multipath_2^{1}
D0 LSB	Multipath_2^{0}

Result Misc Subaddress 83H	
Bit Function	
MSB D7	IF_Window
D6	IF_Center
D5	Fieldstrength_Comp
D4	Multipath_Comp
D3	Res
D2	Res
D1	Res
D0 LSB	Res

Status, Subaddress 00H																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0			0		0	0	0									these bits must be = 0
0	1															opendrain Port_2 output = high level
0	0															opendrain Port_2 output = low level
0		1														opendrain Port_1 output = high level
0		0														opendrain Port_1 output = low level
0				1												Loopamp currentsource high ($I_{LOOPAMP}$=2.4mA) for high speed tuning
0				0												Loopamp currentsource low ($I_{LOOPAMP}$=1.2mA)
0								0	0	1						7 bit AD Converter enabled for single mode, stop
0								1	0	1						7 bit AD Converter enabled for single mode start. To restart single mode write the same bits once more.
0								0	1	1						7 bit AD Converter enabled for continuos mode run.
0								x	x	1						7 bit AD Converter enabled for single or continous mode
0								x	x	0						7 bit AD Converter disabled for single and continous mode
0											1					IF_DAC4 enabled (see subaddress 07H)
0											0					IF_DAC4 disabled (see subaddress 07H)
0												1				Phase detector 1
0												0				Phase detector 0
0													1	1		Chargepump current I_{cp3} = 4mA
0													1	0		Chargepump current I_{cp2} = 2mA
0													0	1		Chargepump current I_{cp1} = 1mA
0													0	0		Chargepump current I_{cp0} = 500uA
0															1	Chargepump enabled
0															0	Chargepump disabled

Subaddress 01H, R_Counter and Subaddress 02H, N_Counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Divider by 65535
0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	Divider by 2000
0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	0	Divider by 1230
0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	Divider by 1000
0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	Divider by 615
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	Divider by 100
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	Divider by 10
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Divider by 2

Subaddress 03H, Mute_DAC7								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								Mute_DAC7 enabled
0	x	x	x	x	x	x	x	Mute_DAC7 disabled, full mute
1	1	1	1	1	1	1	1	Mute_DAC full scale mute off
								typical attenuation
1	1	1	1	0	0	0	1	Mute -5 dB
1	1	1	0	1	0	0	1	Mute - 10 dB
1	1	1	0	0	0	1	0	Mute - 15 dB
1	1	0	1	1	0	1	1	Mute - 20 dB
1	1	0	1	0	0	1	1	Mute - 25 dB
1	1	0	0	1	1	0	0	Mute - 30 dB
1	1	0	0	0	1	0	0	Mute - 35 dB
1	0	1	1	1	1	0	1	Mute - 40 dB
1	0	0	1	0	0	0	0	Full mute
1	0	0	1	0	0	0	0	Full mute
1	0	0	1	0	0	0	0	Full mute

Subaddress 04H, IF_Count_P1								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								IF_Count enabled
0								IF_Count disabled
	0							not used (must be=0)
		1	0	0				Window=+/-100kHz*
		0	1	1				Window=+/-50kHz*
		0	1	0				Window=+/-25kHz*
		0	0	1				Window=+/-12.5kHz*
		0	0	0				Window=+/-6.25kHz*
					1	1	1	Gatetime= 40.96ms
					1	1	0	Gatetime= 20.48ms
					1	0	1	Gatetime= 10.24ms
					1	0	0	Gatetime= 5.12ms
					0	1	1	Gatetime= 2.56ms
					0	1	0	Gatetime= 1.28ms
					0	0	1	Gatetime= 640us
					0	0	0	Gatetime= 320us

* Valid for D7= 0 in subaddress 05H

Multiply window value with 2 for D7= 1 in subaddress 05H

(e. g. D7= 0 Window =+/- 6.25 kHz

D7= 1 Window =+/- 12.5 kHz)

Subaddress 05H, IF_Count_P2, Centerfrequency = CF, CF_{step}= 6.25kHz / 12.5kHz)								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								Centerfequency CF1
0								Centerfequency CF0
1	1	1	1	1	1	1	1	CF1= 22.3875 MHz
0	1	1	1	1	1	1	1	CF0= 11.1937 MHz
1	1	0	0	0	0	0	0	CF1= 22.600 MHz
0	1	0	0	0	0	0	0	CF0= 10.800 MHz
1	0	1	1	0	0	0	1	CF1= 21.4125 MHz
0	0	1	1	0	0	0	1	CF0= 10.70625 MHz
1	0	1	1	0	0	0	0	CF1= 21.400 MHz
0	0	1	1	0	0	0	0	CF0= 10.700 MHz
1	0	1	0	1	1	1	1	CF1= 21.3875 MHz
0	0	1	0	1	1	1	1	CF0= 10.69375 MHz
1	0	1	0	0	0	0	0	CF1= 21.200 MHz
0	0	1	0	0	0	0	0	CF0= 10.600 MHz
1	0	0	1	0	0	0	0	CF1= 21.000 MHz
0	0	0	1	0	0	0	0	CF0= 10.500 MHz
1	0	0	0	0	0	0	0	CF1= 20.800 MHz
0	0	0	0	0	0	0	0	CF0= 10.400 MHz

Centerfrequencies for

D7=1 CF1= 20.800 MHz +n*12.5 kHz, CF_{Step}=12.5kHz

D7=0 CF0= 10.400 MHz +n*6.25 kHz, CF_{Step}=12.5kHz

n=0...127

Subaddress 06H, Specials								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								XTAL_DIV6 enabled
0								XTAL_DIV6 disabled
	1							1st LO divided by 1
	0							1st LO divided by 2
		0	0					Prest. AGC threshold typ. 15 mV
		0	1					Prest. AGC threshold typ. 30 mV
		1	0					Prest. AGC threshold typ. 45 mV
		1	1					Prest. AGC threshold typ. 60 mV
				1	1	1	1	XTAL_adjust C_L = 15 pF
				1	1	1	0	XTAL_adjust C_L = 14pF
				1	1	0	1	XTAL_adjust C_L = 13 pF
				1	1	0	0	XTAL_adjust C_L = 12 pF
				1	0	1	1	XTAL_adjust C_L = 11 pF
				1	0	1	0	XTAL_adjust C_L = 10 pF
				1	0	0	1	XTAL_adjust C_L = 9 pF
				1	0	0	0	XTAL_adjust C_L = 8 pF
				0	1	1	1	XTAL_adjust C_L = 7 pF
				0	1	1	0	XTAL_adjust C_L = 6 pF
				0	1	0	1	XTAL_adjust C_L = 5 pF
				0	1	0	0	XTAL_adjust C_L = 4 pF
				0	0	1	1	XTAL_adjust C_L = 3 pF
				0	0	1	0	XTAL_adjust C_L = 2 pF
				0	0	0	1	XTAL_adjust C_L = 1pF
				0	0	0	0	XTAL_adjust C_L = 0pF

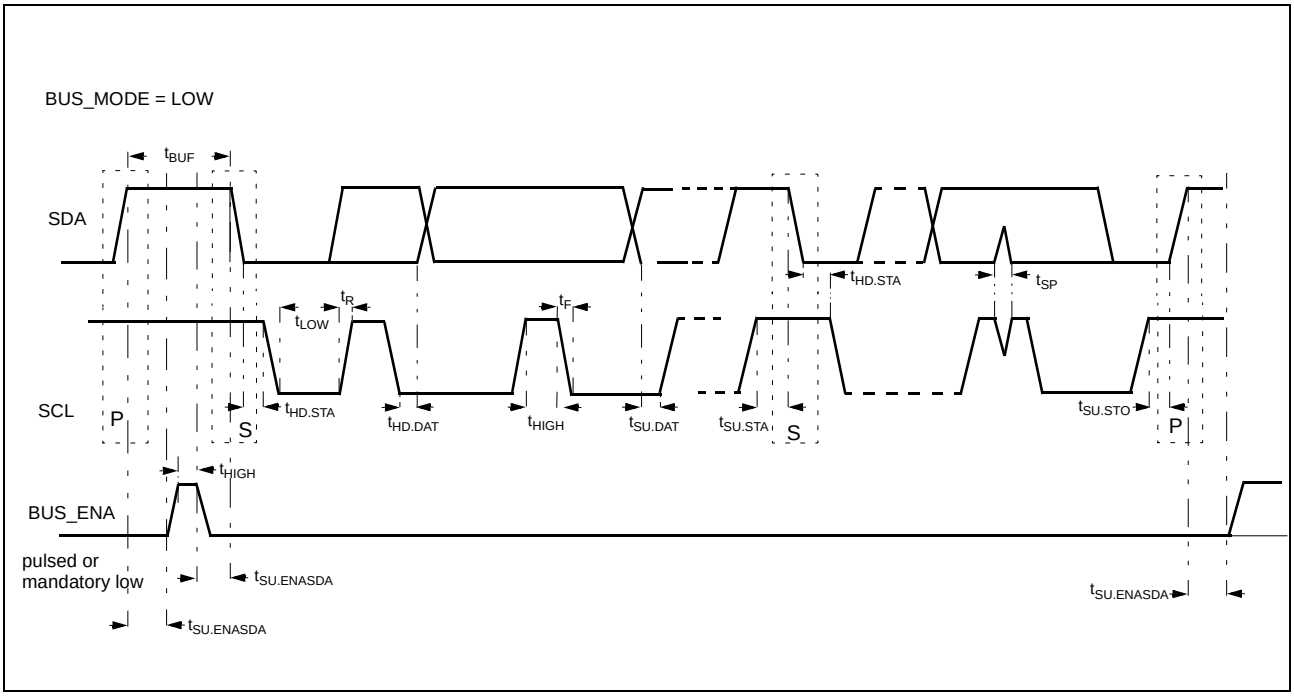
Subaddress 07H, IF_DAC4								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
x	x	x	x					not used
				1	1	1	1	IF_DAC Gain adj. typ. 16 dB
				1	1	1	0	IF_DAC Gain adj.
				1	1	0	1	IF_DAC Gain adj.
				1	1	0	0	IF_DAC Gain adj.
				1	0	1	1	IF_DAC Gain adj. typ. 21 dB
				1	0	1	0	IF_DAC Gain adj.
				1	0	0	1	IF_DAC Gain adj.
				1	0	0	0	IF_DAC Gain adj.
				0	1	1	1	IF_DAC Gain adj.
				0	1	1	0	IF_DAC Gain adj.
				0	1	0	1	IF_DAC Gain adj.
				0	1	0	0	IF_DAC Gain adj. typ. 24 dB
				0	0	1	1	IF_DAC Gain adj.
				0	0	1	0	IF_DAC Gain adj.
				0	0	0	1	IF_DAC Gain adj.
				0	0	0	0	IF_DAC Gain adj. typ. 26 dB

Subaddress 0BH, Comp preset																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X								X								not used
	$FP2^6$	$FP2^5$	$FP2^4$	$FP2^3$	$FP2^2$	$FP2^1$	$FP2^0$									Preset value Fieldstrength
									$MP2^6$	$MP2^5$	$MP2^4$	$MP2^3$	$MP2^2$	$MP2^1$	$MP2^0$	Preset value Multipath

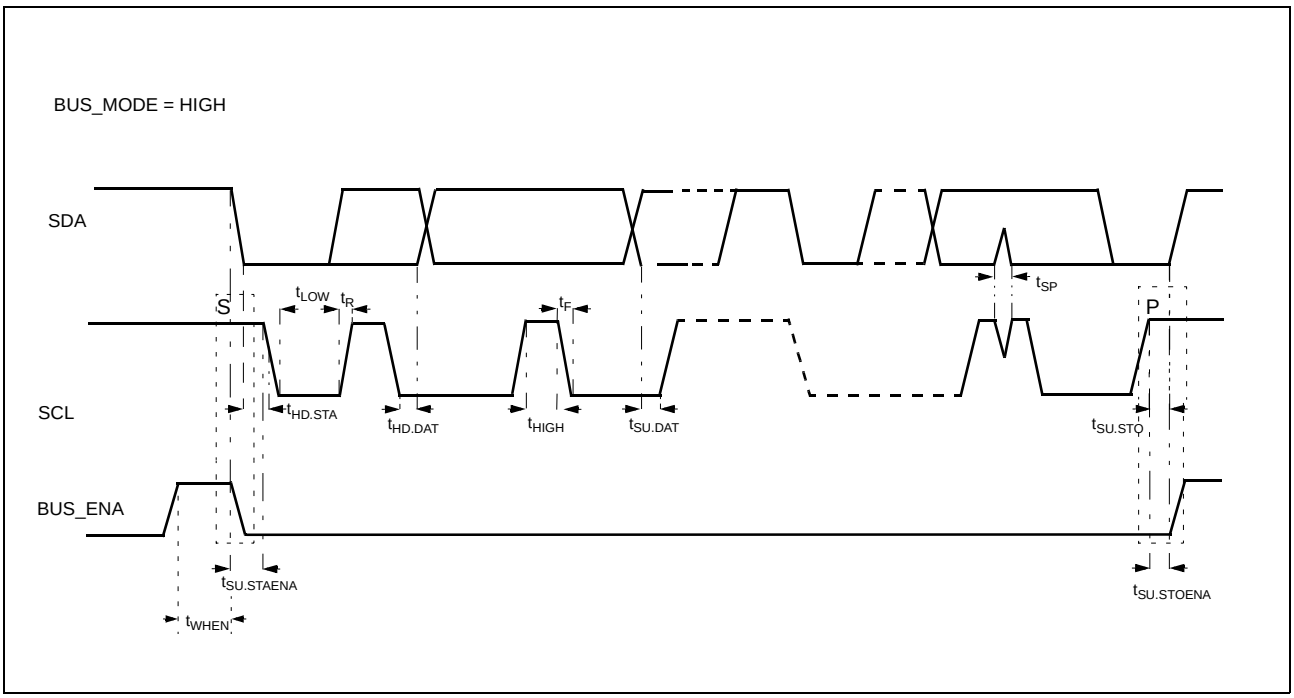
Subaddress 82H, Read Results from Fieldstrength, Multipath and IF counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1								1								IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.
0								1								IF_counter result: IF frequency is outside the desired window.IF frequency is higher as the desired IF frequency.
x								0								IF_counter result: IF frequency is inside the desired window
	$M2^6$	$M2^5$	$M2^4$	$M2^3$	$M2^2$	$M2^1$	$M2^0$									Result multipath byte M6...M0
									$F2^6$	$F2^5$	$F2^4$	$F2^3$	$F2^2$	$F2^1$	$F2^0$	Result Fieldstrength byte F6...F0

Subaddress 83H, Read results misc								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	1			Res	Res	Res	Res	IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.
0	1			Res	Res	Res	Res	IF_counter result: IF frequency is outside the desired window.IF frequency is higher as the desired IF frequency.
x	0			Res	Res	Res	Res	IF_counter result: IF frequency is inside the desired window
		1						Fieldstrengthsignal is higher as the preseted value in subaddres 0BH (D8...D14)
		0						Fieldstrengthsignal is lower as the preseted value in subaddres 0BH (D8...D14)
			1					Multipathsignal is higher as the preseted value in subaddres 0BH (D0...D6)
			0					Multipathsignal is lower as the preseted value in subaddres 0BH (D0...D6)

8.13.2 I²C Bus Timing



3W-Bus Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
LOW level input voltage (SDA, SCL, BUS_ENA, BUS_MODE)	V_{IL}	-0.5	0.90	V
HIGH level input voltage (SDA, SCL, BUS_ENA, BUS_MODE)	V_{IH}	2.10	5.50	V
Pulse widh of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
LOW level output voltage 3mA sink current (SDA)	V_{OL}	0	0.40	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capcitance from 10pF to 400pFwith up to 3mA	tf_{OF}	$20+0.1C_b$ [3]	250	ns
SCL clock frequency	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition [1]	t_{BUF}	1.3		us
Hold time (repeated) START condition. After this period, the first clock pulse is generated. [1]	$t_{HO.STA}$	0.6		us
LOW period of the SCL clock	t_{LOW}	1.3		us
HIGH period of the SCL clock	t_{HIGH}	0.6		us
Set-up time for a repeated START condition [1]	$t_{SU.STA}$	0.6		us
Data hold time	$t_{HD.DAT}$	0		ns
Data set -up time	$t_{SU.DAT}$	100		ns
Rise, fall time of both SDA and SCL signals	t_R, t_F	$20+0.1C_b$ [3]	300	ns
Set-up time for STOP condition [1]	$t_{SU.STO}$	0.6		us
Capacitive load for each bus line	C_b		400	pF
Setup time SCL to BUS_ENA [2]	$t_{SU.SCLEN}$	0.6		us
H-pulsewidth (BUS_ENA)	t_{WHEN}	0.6		us

[1] only in I^2C bus mode
[2] only in 3W bus mode
[3] C_b= capacitance of one bus line in pF.
Note that the maximum t_F for the SDA and SCL bus lines quoted at 300ns is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA / SCL pins and the SDA /SCL bus lines without exceeding the maximum specified t_F.

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Parameter	Symbol	Limit Values		Units
		min.	max.	
ESD-Protection all bipolar pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	- 2	2	kV
ESD-Protection all CMOS pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	t.b.d.	t.b.d.	kV
Total power dissipation	P_{tot}		900	mW
Ambient temperature	T_A	- 40	85	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	- 40	125	°C
Thermal resistance P-MQFP-64 (sys-air)	T_{thSA}		54	K/W

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

9.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_{VCC}	8	9	V	
Current consumption	I_{vcc}		100	mA	
Ambient temperature	T_A	- 40	85	°C	

9.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

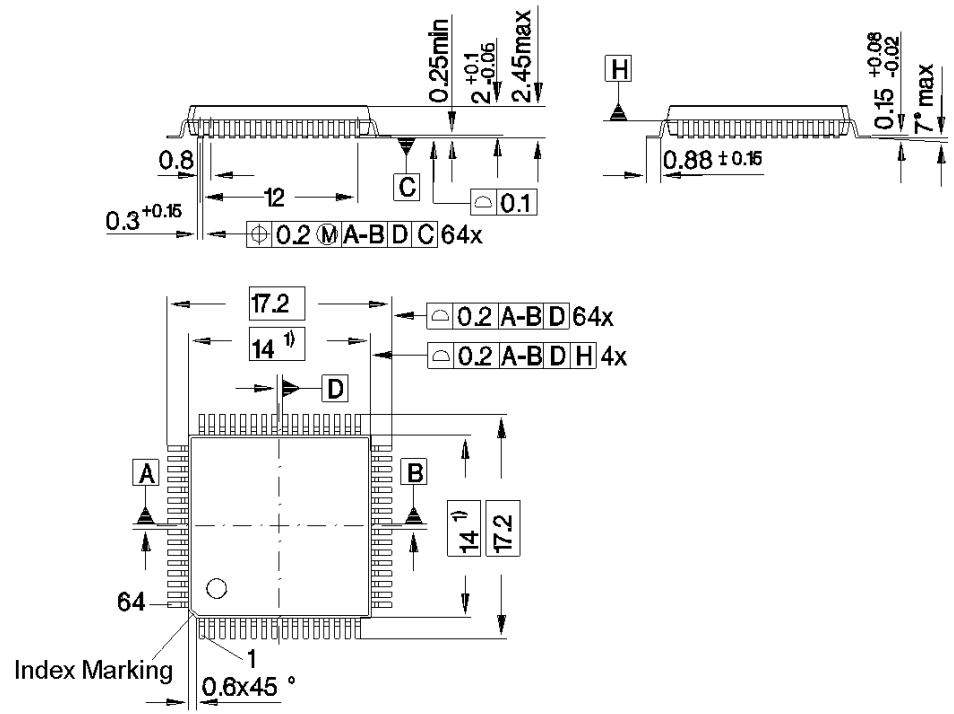
Parameter T_A = 25 °C,V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Power supply						
Total current consumption	I_{VCC}		85		mA	
1st local oscillator						
Frequency range	$f_{1st\ LO}$	50		250	MHz	
Frequency range	$f_{1st\ LO}$	80		150	MHz	Q factor of coil > tbf
Frequency range	$f_{1st\ LO}$	160		250	MHz	coil tbf; see SUB06h
Negative input impedance	Z_{27-28}		- tbf		Ω	f = 100 MHz
RF mixer						
Input frequency	f_{31-32}	60		140	MHz	
Max input RF level	V_{31-32}	120			dBµV	
Input impedance single ended	$R_{31/32}$		tbf		Ω	
	$C_{31/32}$		tbf		pF	
Mixer gain	A_{mix}		tbf		dB	
Input IP3			tbf		dBµV	
Noise Figure	F		tbf		dB	
Reference voltage RF section	V_{39}		4.8		V	
Prestage AGC outputs						
AGC threshold range	V_{31-32}	15		60	mV	see diagram SUB06h
AGC voltage for MOSFET Gate 2	V_{30}		6.4		V	V_{31-32} = 0 mV
AGC voltage for MOSFET Gate 2	V_{30}			0.1	V	V_{31-32} = 200 mV
AGC current normal polarity	I_{35}		12		mA	V_{31-32} = 0 mV
AGC current normal polarity	I_{35}			0.1	mA	V_{31-32} = 200 mV
AGC current inverse polarity	I_{34}		12		mA	V_{31-32} = 200 mV
AGC current inverse polarity	I_{34}			0.1	mA	V_{31-32} = 0 mV
Integrator current	I_{30}		-50		µA	V_{31-32} = 0 mV; Vm = 3V
Integrator current	I_{30}		50		µA	V_{31-32} = 200 mV; Vm = 3V

Parameter T_A = 25 °C, V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
IF amplifier						
DC input voltage	V_{41}		4		V	
Input resistance	R_{41}		330		Ω	
Output resistance	R_{45}		330		Ω	
Voltage gain	A_{45-41}		26		dB	V_{44} = 1.5 V; see also diagram SUB07h
Voltage gain	A_{45-41}		16		dB	V_{44} = 3.5 V; see also diagram SUB07h
Noise figure	F		7		dB	R_G = 330 Ω
IF limiter amplifier / fieldstrength generator						
Input voltage for limiter threshold	V_{49}		25		μV_{rms}	f_{in} = 10.7 MHz; V_{54} - 3 dB
AM suppression	A_{AM}		80		dB	m = 30 %
Fieldstrength voltage	V_{55}			0.5	V	V_{49} = 0 mV_{rms}
Fieldstrength voltage	V_{55}		tbf		V	V_{49} = 1 mV_{rms}
Fieldstrength voltage	V_{55}		tbf		V	V_{49} = 10 mV_{rms}
Fieldstrength voltage	V_{55}		4.5		V	V_{49} = 200 mV_{rms}
Fieldstrength dynamic range	V_{55dyn}		90		dB	
Fieldstrength linearity	V_{55lin}		±1		dB	
Fieldstrength temperature drift	V_{55temp}			±3	dB	
FM demodulator / soft mute						
AF output voltage	V_{54}		600		mV_{rms}	ΔF = 75 kHz; f_{IF}=10.7 MHz
AF output voltage	V_{54}		300		mV_{rms}	ΔF = 75 kHz; f_{IF}= 21.4 MHz
Total harmonic distortion	THD_{54}		0.5		%	ΔF = 75 kHz
Total harmonic distortion detuned	THD_{54}			0.8	%	f_{in} = 10.7 MHz ± 50 kHz; ΔF = 75 kHz
AF mute depth range	a_{54}	0		38	dB	V_{53} = 0 V; see diagram SUB03h
AF full mute	a_{54}	80			dB	V_{53} = 0 V; see diagram SUB03h
Multipath detector						
Attack current	I_{58}*)		800		µA	V_{56} = 1 V_{pp}; V_m = 5 V
Recovery current	I_{58}*)		-9		µA	V_{56} = 0 V_{pp}; V_m = 3.6 V
Start voltage	V_{59Def}		4.7		V	V_{56} = 0 V_{pp}
Detector characteristic	V_{59}		V_{59Def} - 0.1 V		V	f_{56} = 25 kHz V_{56} = 160 mV_{pp}
Detector characteristic	V_{59}		V_{59Def} - 1 V		V	f_{56} = 200 kHz V_{56} = 160 mV_{pp}
Reference voltage IF	V_{43}		4.8		V	

Parameter T_A = 25 °C, V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
*) Detector currents are measured between the output pin (-pole) and a voltage source V_m						
Crystal oscillator						
Operating frequency	f_{16-17}		61.5		MHz	3rd harmonic
Negative input impedance	Z_{16-17}		- 250		Ω	f = 61.5 MHz
Negative input impedance	Z_{16-17}		1.4		kΩ	f = 20.5 MHz
Input impedance crystal	R_{cr}			tbd	Ω	3rd harmonic
Spurious harmonics crystal	a_{sp}			- 20	dB	f < 200 MHz
Bus controlled adjust range	Δf_{adj}		± 40		ppm	see diagram SUB06h
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} on AC		500		mV_{pp}	f = 10.25 MHz, C_{load} = 10 pF
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} on DC		1.5		V_{DC}	f = 10.25 MHz, C_{load} = 10 pF
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} off DC			50	mV_{DC}	C_{load} = 10 pF
Chargepump output (Loopfilter input)						
DC voltage	$V_{PD\_0/1}$		2.5		V	locked
DC current	$\pm I_{PD\_0/1\_3}$	3.2	4	4.8	mA	see Status, Subaddress 00H, bit D1, D2 $V_{PD\_0/1}$ = 1.5V
DC current	$\pm I_{PD\_0/1\_2}$	1.6	2	2.4	mA	
DC current	$\pm I_{PD\_0/1\_1}$	0.8	1	1.2	mA	
DC current	$\pm I_{PD\_0/1\_0}$	400	500	600	uA	
Tristate output current	$\pm I_{PD\_0/1\_OFF}$		0.1	10	nA	$V_{PD\_0/1}$ = 1.5V , guaranteed by design
Loop amplifier tuningvoltage output (Loopfilter output)						
LOW output voltage	V_{PDA_L}	0	tbd.	400	mV	I_{TUNE} = 100 uA
HIGH output voltage	V_{PDA_H}	V_{VCC}-0.5V	tbd.	V_{CC}	mV	I_{TUNE} = -100 uA
HIGH output current source	I_{PDA_H}		2.4		mA	V_{TUNE} = 4V, $V_{PD\_0/1}$ = 0V (see Status, Subaddress 00H, bit D11)
LOW output current source	I_{PDA_L}		1.2		mA	V_{TUNE} = 4V, $V_{PD\_0/1}$ = 0V (see Status, Subaddress 00H, bit D11)
PLL for synthesizer (see PLL Synthesizer on page 17)						
PLL / VCO step size (programmable via R-counter)	f_{ref}	6.25		100	kHz	$f_{crystal}$ = 61.5 MHz
N-counter divide ratio	N	2		65535		16-Bit
R-counter divide ratio	R	2		65535		16-Bit

Parameter T_A = 25 °C,V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Port outputs, PORT_1, PORT_2, IF_CENT, IF_WINDOW (see Output ports on page 16)						
LOW output voltage	V_P	0	100	400	mV	I_P = 1 mA
HIGH Leackage current	I_{P_LEACK}	0		100	nA	V_P = 5 V
I2C / 3-Wire-bus (BUS_MODE, SCL, SDA, BUS_ENA) (see I2C Bus Timing on page 26 and Bus Data Format on page 20)						
H-input voltage	V_{IH}	2.10		5.50	V	
L-input voltage	V_{IL}	-0.5		0.90	V	
Hysteresis of Schmitt trigger inputs (BUS_MODE, SCL, SDA, BUS_ENA)	V_{hys}		0.30		V	
Input capacity	C_I			5	pF	

10 Package Outline



Does not include plastic or metal protrusion of 0.25 max. per side