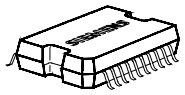
Smart Quad Low-Side Switch

Features

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 8 bit Serial Data Input and Diagnostic Output (SPI protocol)
- Direct Parallel Control of Four Channels for PWM Applications
- Cascadable with Other Quad Switches
- Low Quiescent Current
- µC Compatible Input
- **E**lecto**s**tatic **D**ischarge (ESD) Protection

Product Summary

Supply voltage	V_S	4.5 – 5.5	V
Drain source voltage	$V_{DS(AZ)max}$	60	V
On resistance (T_J = 25 °C)	$R_{ON(max)}$	0.4	Ω
Output current (all outp. ON equal)	$I_{D(NOM)}$	1	A
(individually)		3	A



P-DSO-20-10

Ordering Code:
Q67006-A9315

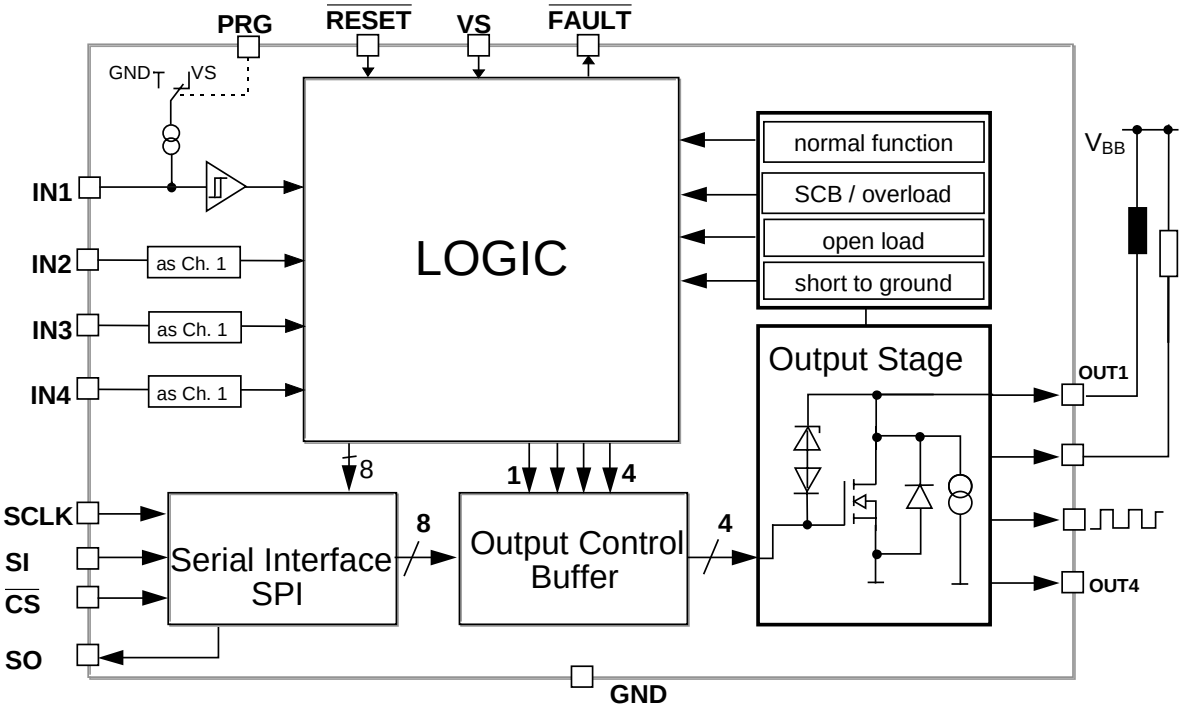
Application

- µC Compatible Power Switch for 12 V and 24 V Applications
- Switch for Automotive and Industrial System
- Solenoids, Relays and Resistive Loads
- Injectors
- Robotic controls

General Description

Quad Low-Side Switch in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and four open drain DMOS output stages. The TLE 6220 GP is protected by embedded protection functions and designed for automotive and industrial applications. The output stages can be controlled direct in parallel for PWM applications (injector coils), or through serial control via the SPI. Therefore the TLE 6220 GP is particularly suitable for engine management and powertrain systems.

Block Diagram

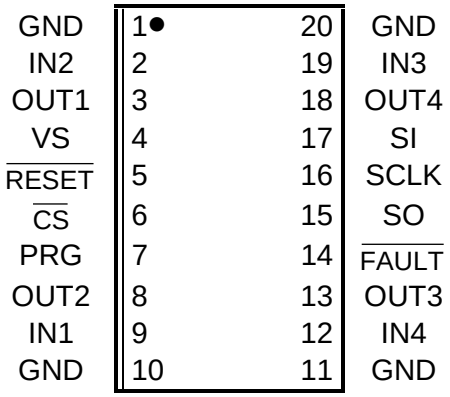


Pin Description

Pin	Symbol	Function
1	GND	Ground
2	IN2	Input Channel 2
3	OUT1	Power Output Channel 1
4	VS	Supply Voltage
5	$\overline{\text{RESET}}$	Reset
6	$\overline{\text{CS}}$	Chip Select
7	PRG	Program (inputs high or low active)
8	OUT2	Power Output Channel 2
9	IN1	Input Channel 1
10	GND	Ground
11	GND	Ground
12	IN4	Input Channel 4
13	OUT3	Power Output Channel 3
14	$\overline{\text{FAULT}}$	General Fault Flag
15	SO	Serial Data Output
16	SCLK	Serial Clock
17	SI	Serial Data Input
18	OUT4	Power Output Channel 4
19	IN3	Input Channel 3
20	GND	Ground

Heat slug internally connected to ground pins

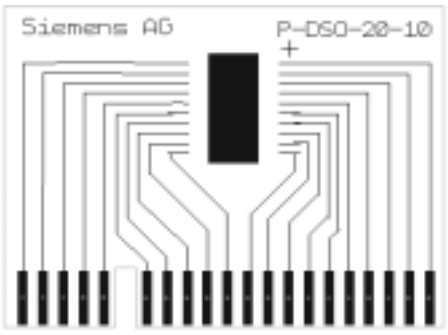
Pin Configuration (Top view)



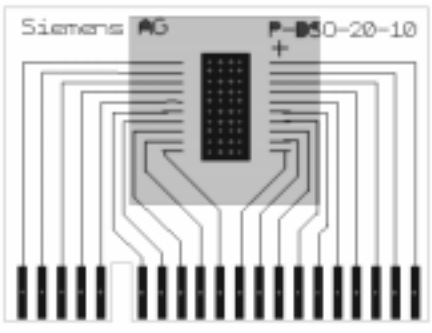
Power SO-20

Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply Voltage	V_S	-0.3 ... +7	V
Continuous Drain Source Voltage (OUT1...OUT4)	V_{DS}	45	V
Input Voltage, All Inputs and Data Lines	V_{IN}	- 0.3 ... + 7	V
Load Dump Protection $V_{Load\ Dump} = U_P + U_S$; U_P=13.5 V	$V_{Load\ Dump}$ [2]		V
With Automotive Injector Valve R_L = 14 Ω		62	
R_I [1]=2 Ω; t_d=400ms; IN = low or high			
With R_L= 6.8 Ω (I_D = 2A)		52	
R_I=2 Ω; t_d=400ms; IN = low or high			
Output Current per Channel (see el. characteristics)	$I_{D(lim)}$	self limited	A
Output Current per Channel @ T_A = 25°C (All 4 Channels ON; Mounted on PCB) [3]	I_D	1	A
Output Clamping Energy I_D = 1A	E_{AS}	50	mJ
Power Dissipation (DC, mounted on PCB) @ T_A = 25°C	P_{tot}	3	W
Electro**s**tatic **D**ischarge Voltage (human body model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2000	V
DIN Humidity Category, DIN 40 040		E	
IEC Climatic Category, DIN IEC 68-1		40/150/56	
Thermal resistance			K/W
junction - case	R_{thJC}	5	
junction - ambient @ min. footprint	R_{thJA}	50	
junction - ambient @ 6 cm^2 cooling area		38	



Minimum footprint



PCB with heat pipes,
backside 6 cm^2 cooling area

[1] R_I=internal resistance of the load dump test pulse generator LD200
[2] $V_{LoadDump}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839.
[3] Output current rating so long as maximum junction temperature is not exceeded. At T_A = 125 °C the output current has to be calculated using R_{thJA} according mounting conditions.

Electrical Characteristics

Parameter and Conditions V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)	Symbol	Values			Unit
		min	typ	max	
1. Power Supply, Reset					
Supply Voltage[4]	V_S	4.5	--	5.5	V
Supply Current	I_S	--	1	2	mA
Supply Current in Standby Mode (RESET = L)	$I_{S(stby)}$	--	--	50	µA
Minimum Reset Duration (After a reset all parallel inputs are ORed with the SPI data bits)	$t_{Reset,min}$	10			µs
2. Power Outputs					
ON Resistance V_S = 5 V; I_D = 1 A T_J = 25°C	$R_{DS(ON)}$	--	--	0.4	Ω
T_J = 150°C		--	--	0.75	
Output Clamping Voltage output OFF	$V_{DS(AZ)}$	45	53	60	V
Current Limit	$I_{D(lim)}$	3	4	6	A
Output Leakage Current V_{RESET} = L	$I_{D(lkg)}$	--	--	10	µA
Turn-On Time I_D = 1 A, resistive load	t_{ON}	--	5	10	µs
Turn-Off Time I_D = 1 A, resistive load	t_{OFF}	--	5	10	µs
3. Digital Inputs					
Input Low Voltage	V_{INL}	- 0.3	--	1.0	V
Input High Voltage	V_{INH}	2.0	--	--	V
Input Voltage Hysteresis	V_{INHys}	50	100	200	mV
Input Pull Down/Up Current (IN1 ... IN4)	$I_{IN(1..4)}$	20	50	100	µA
PRG, $\overline{\text{RESET}}$ Pull Up Current	$I_{IN(PRG,Res)}$	20	50	100	µA
Input Pull Down Current (SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA
Input Pull Up Current ($\overline{\text{CS}}$)	$I_{IN(CS)}$	10	20	50	µA
4. Digital Outputs (SO, $\overline{\text{FAULT}}$)					
SO High State Output Voltage I_{SOH} = 2 mA	V_{SOH}	V_S - 0.4	--	--	V
SO Low State Output Voltage I_{SOL} = 2.5 mA	V_{SOL}	--	--	0.4	V
Output Tri-state Leakage Current $\overline{\text{CS}}$ = H, 0 ≤ V_{SO} ≤ V_S	I_{SOlkg}	-10	0	10	µA
$\overline{\text{FAULT}}$ Output Low Voltage I_{FAULT} = 1.6 mA	V_{FAULTL}	--	--	0.4	V
Current Limitation; Overload Threshold Current	$I_{D(lim)\ 1...4}$	3	4	6	A
Overtemperature Shutdown Threshold	$T_{th(sd)}$	170	--	200	°C
Hysteresis	T_{hys}	--	10	--	K

[4] For V_S < 4.5V the power stages are switched according the input signals and data bits or are definitely switched off. This undervoltage reset gets active at V_S = 3V (typ. value) and is guaranteed by design.

Electrical Characteristics cont.

Parameter and Conditions V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)	Symbol	Values			Unit
		min	typ	max	
5. Diagnostic Functions					
Open Load Detection Voltage	$V_{DS(OL)}$	--	3	--	V
Output Pull Down Current	$I_{PD(OL)}$	50	90	150	µA
Fault Delay Time	$t_{d(fault)}$	50	110	200	µs
Short to Ground Detection Voltage	$V_{DS(SHG)}$	--	2	--	V
Short to Ground Detection Current	I_{SHG}	-50	-100	-150	µA
6. SPI-Timing					
Serial Clock Frequency (depending on SO load)	f_{SCK}	DC	--	5	MHz
Serial Clock Period (1/fclk)	$t_{p(SCK)}$	200	--	--	ns
Serial Clock High Time	t_{SCKH}	50	--	--	ns
Serial Clock Low Time	t_{SCKL}	50	--	--	ns
Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK)	t_{lead}	250	--	--	ns
Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$)	t_{lag}	250	---	--	ns
Data Setup Time (required time SI to falling of CLK)	t_{SU}	20	--	--	ns
Data Hold Time (falling edge of CLK to SI)	t_H	20	--	--	ns
SI, $\overline{CS}$, SCLK Rise Time (SPI inputs)	t_{rSI}	--	--	50	ns
SI, $\overline{CS}$, SCLK Fall Time (SPI inputs)	t_{fSI}	--	--	50	ns
Disable Time @ C_L = 50 pF	t_{DIS}	--	--	150	ns
Transfer Delay Time[5] ($\overline{CS}$ high time between two accesses)	t_{dt}	200	--	--	ns
Data Valid Time C_L = 50 pF	t_{valid}	--	--	110	ns
C_L = 100 pF[6]		--	--	120	
C_L = 220 pF[6]		--	--	150	

[5] This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200µs.
[6] This parameter will not be tested but guaranteed by design

Functional Description

The TLE 6220 GP is an quad-low-side power switch which provides a serial peripheral interface (SPI) to control the 4 power DMOS switches, as well as diagnostic feedback. The power transistors are protected against short to V_{BB}, overload, overtemperature and against overvoltage by an active zener clamp.
The diagnostic logic recognises a fault condition which can be read out via the serial diagnostic output (SO).

Circuit Description

Power Transistor Protection Functions

Each of the four output stages has its own zener clamp, which causes a voltage limitation at the power transistor when solenoid loads are switched off. The outputs are provided with a current limitation set to a minimum of 3 A. The continuous current for each channel is 1A (all channels ON; depending on cooling).
Each output is protected by embedded protection functions. In the event of an overload or short to supply, the current is internally limited and the corresponding bit combination is set (early warning). If this operation leads to an overtemperature condition, a second protection level (about 170 °C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

SPI Signal Description

$\overline{\text{CS}}$ - Chip Select. The system microcontroller selects the TLE 6220 GP by means of the $\overline{\text{CS}}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.

$\overline{\text{CS}}$ High to Low transition:
- Diagnostic status information is transferred from the power outputs into the shift register.
- Serial input data can be clocked in from then on.
- SO changes from high impedance state to logic high or low state corresponding to the SO bits.

$\overline{\text{CS}}$ Low to High transition:
- Transfer of SI bits from shift register into output buffers
- Reset of diagnosis register.

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

SCLK - Serial Clock. The system clock pin clocks the internal shift register of the TLE 6220 GP. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out of the shift register on the

rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.
The input data consists of one byte, made up of four control bits and four data bits. The control word is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see page 11). The four data bits contain the input information for the four channels, and are high active.

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

$\overline{\textbf{RESET}}$ - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.

Output Stage Control

The four outputs of the TLE 6220 GP can either be controlled in parallel (IN1...IN4), or via the Serial Peripheral Interface (SPI).

Parallel Control

A Boolean operation (either AND or OR) is performed on each of the parallel inputs and respective SPI data bits, in order to determine the states of the respective outputs. The type of Boolean operation performed is programmed via the serial interface.
The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 are switched OFF. PRG pin itself is internally pulled up when it is not connected.

PRG - Program pin. PRG = High (V_S): Parallel inputs Channel 1 to 4 are high active
PRG = Low (GND): Parallel inputs Channel 1 to 4 are low active.

Serial Control of the Outputs: SPI protocol

Each output is independently controlled by an output latch and a common reset line, which disables all four outputs. The Serial Input (SI) is read on the falling edge of the serial clock. A logic high input 'data bit' turns the respective output channel ON, a logic low 'data bit' turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output control buffer.

As mentioned above, the serial input byte consists of a 4 bit control word and a 4 bit data word. Via the control word, the specific mode of the device is programmable.

MSB LSB
CCCC DDDD : Serial input byte
Control Bits Data Bits

Five specific control words are recognised, having the following functions:

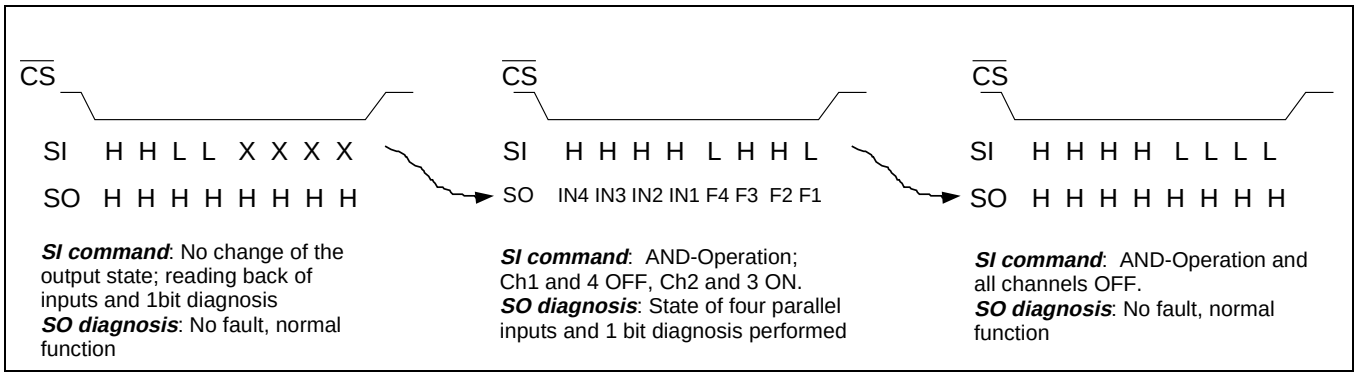
No.	Serial Input Byte	Function
1	LLLL XXXX	Only 'Full Diagnosis' performed. No change to output states.
2	HHLL XXXX	State of four parallel inputs and '1-bit Diagnosis' outputted.
3	HLHL XXXX	Echo-function of SPI; SI direct connected to SO
4	LLHH DDDD	IN1...4 and serial data bits 'OR'ed. 'Full Diagnosis' performed.
5	HHHH DDDD	IN1...4 and serial data bits 'AND'ed. 'Full Diagnosis' performed.

Note: 'X' means 'don't care', because this bit will be ignored
'D' represents the data bit, either being H (=ON) or L (=OFF)

1. **LLLL XXXX** - Diagnosis only
By clocking in this control byte, it is possible to get pure diagnostic information (two bits per channel) in accordance with Figure 1 (page 11). The data bits are ignored, so that the state of the outputs are not influenced. This command is only active once unless the next control command is again "Diagnosis only".

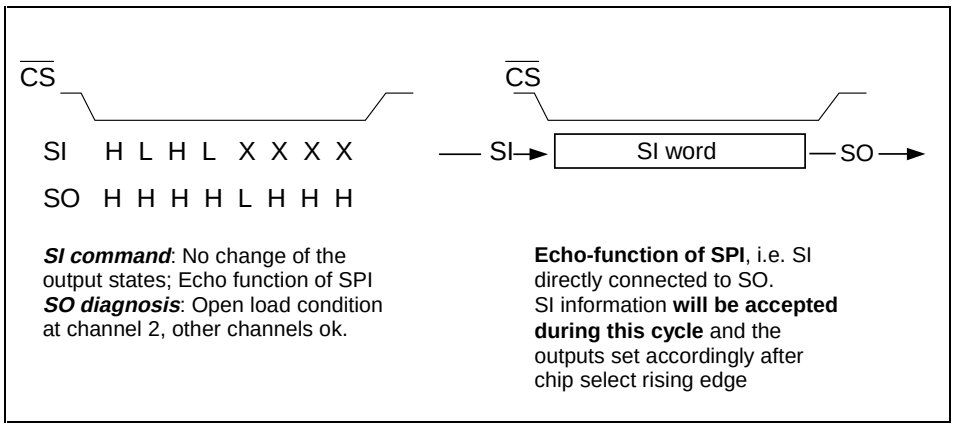
2. **HHLL XXXX** - Reading back of input, and '1-bit Diagnosis'
If the TLE 6220 GP is used as bare die in a hybrid application, it is necessary to know if proper connections exist between the µC-port and parallel inputs. By entering 'HHLL' as the control word, the first four bits of the SO give the state of the parallel inputs, depending on the µC signals. By comparing the four IN-bits with the corresponding µC-port signal, the necessary connection between the µC and the TLE 6220 can be verified - i.e. 'read back of the inputs'.
The second 4-bit word fed out at the serial output contains '1-bit' fault information of the outputs (H = no fault, L = fault). In the expression given below for the output byte, 'FX' is the fault bit for channel X.

MSB LSB
IN4 IN3 IN2 IN1 F4 F3 F2 F1 : Serial Output byte



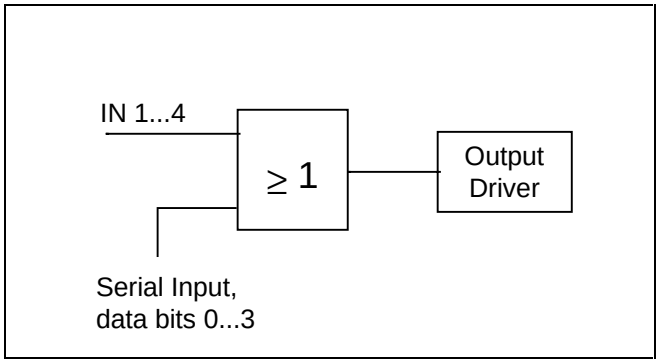
3. **HLHL XXXX** - Echo-function of SPI

To check the proper function of the serial interface the TLE 6220 GP provides a "SPI Echo Function". By entering HLHL as control word, SI and SO are connected during the next $\overline{CS}$ period. By comparing the bits clocked in with the serial output bits, the proper function of the SPI interface can be verified. This internal loop is only closed once (for one $\overline{CS}$ period).



4. **LLHH DDDD** - OR operation, and 'full diagnosis'

With LLHH as the control word, each of the input signals IN1...IN4 are 'OR'ed with the corresponding data bits (DDDD).



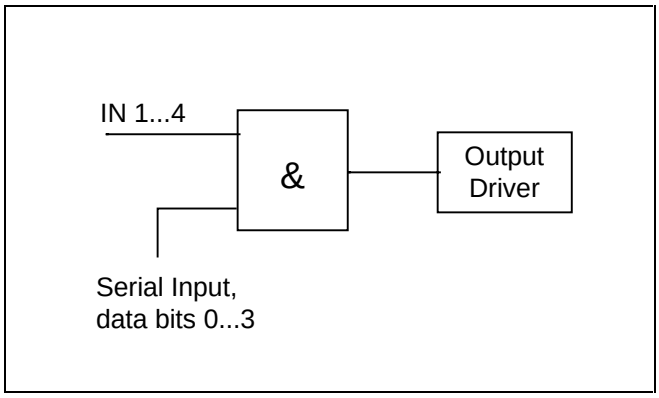
This OR operation enables the serial interface to switch the channel ON, even though the corresponding parallel input might be in the off state.

⇒ **SPI Priority for ON-State**

Also parallel control of the outputs is possible without an SPI input.

The OR-function is the default Boolean operation if the device restarts after a Reset, or when the supply voltage is switched on for the first time.
If the OR operation is programmed it is latched until it is overwritten by the AND operation.

5. **HHHH DDDD -** AND operation, and 'full diagnosis'
With HHHH as the control word, each of the input signals IN1...IN4 are 'AND'ed with the corresponding data bits (DDDD).



The AND operation implies that the output can be switched off by the SPI data bit input, even if the corresponding parallel input is in the ON state.

⇒ **SPI Priority for OFF-state**

This also implies that the serial input data bit can only switch the output channel ON if the corresponding parallel input is in the ON state.
If the AND operation is programmed it is latched until it is overwritten by the OR operation.

Control words beside No. 1- 5

All control words except those for Diag Only, Read Back of Inputs, SPI echo, will be accepted as an OR or an AND command with valid data bits depending on the boolean operation which was programmed before.

Example 1:
LLHH HLLH: OR operation between parallel inputs and data bits, i.e channel 1 and 4 will be switched on.
The next command is now: **LHHH HHLH**
LHHH as command word has no special meaning but it will be accepted as an OR operation and the data bits will be ORed with the inputs and the outputs 1,3 and 4 will be switched on.
See above: 'If the OR operation is programmed it is latched until it is overwritten by the AND operation.'

Example 2:
HHHH LLHL means: Data bits will be ANDed with the parallel inputs and the outputs switch accordingly. Then **HLLH HHLH** is clocked in: AND was latched by the command before and is now valid again by using the HLLH command word. So the data bits will be accepted and again ANDed with the parallel input signals.
See above: 'If the AND operation is programmed it is latched until it is overwritten by the OR operation.'

Diagnostics

$\overline{\text{FAULT}}$ - Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the four channels. This fault indication can be used to generate a µC interrupt. Therefore a 'diagnosis' interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.

As soon as a fault occurs, the fault information is latched into the diagnosis register. A new error will over-write the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{\text{CS}}$ is high. If $\overline{\text{CS}}$ receives a LOW signal, all diagnosis bits can be shifted out serially. The rising edge of $\overline{\text{CS}}$ will reset all error registers.

Full Diagnosis

For full diagnosis there are two diagnostic bits per channel configured as shown in Figure 1.

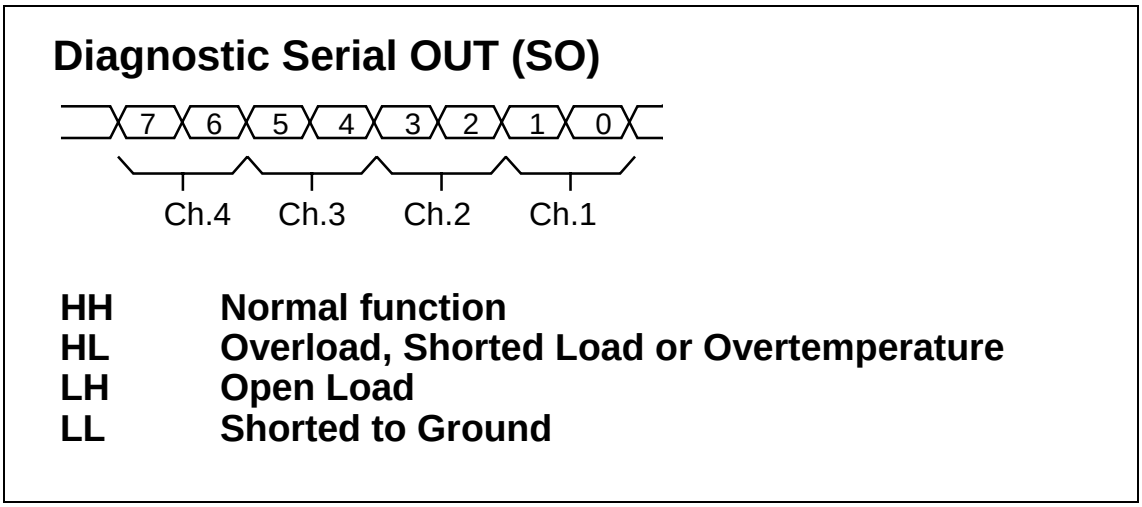


Figure 1: Two bits per channel diagnostic feedback

Normal function: The bit combination **HH** indicates that there is no fault condition, i.e. normal function.
Overload, Short Circuit to Battery (SCB) or Overtemperature: HL is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition.
Open load: An open load condition is detected when the drain voltage decreases below 3 V (typ.). **LH** bit combination is set.
Short Circuit to GND: If a drain to ground short circuit exists and the drain to ground current exceeds 100 µA, short to ground is detected and the **LL** bit combination is set.

A definite distinction between open load and short to ground is guaranteed by design.

The standard way of obtaining diagnostic information is as follows:
Clock in serial information into SI pin and wait approximately 150 µs to allow the outputs to settle. Clock in the identical serial information once again - during this process the data coming out at SO contains the bit combinations representing the diagnosis conditions as described in Figure 1.

Timing Diagrams

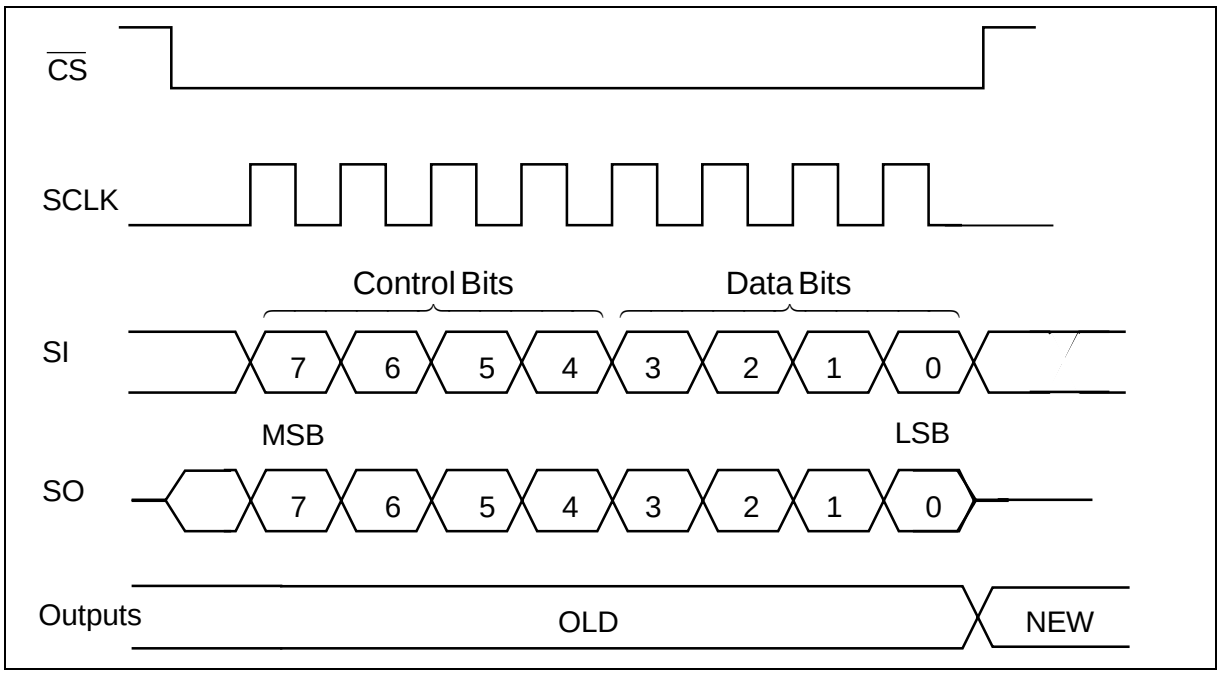


Figure 2: Serial Interface

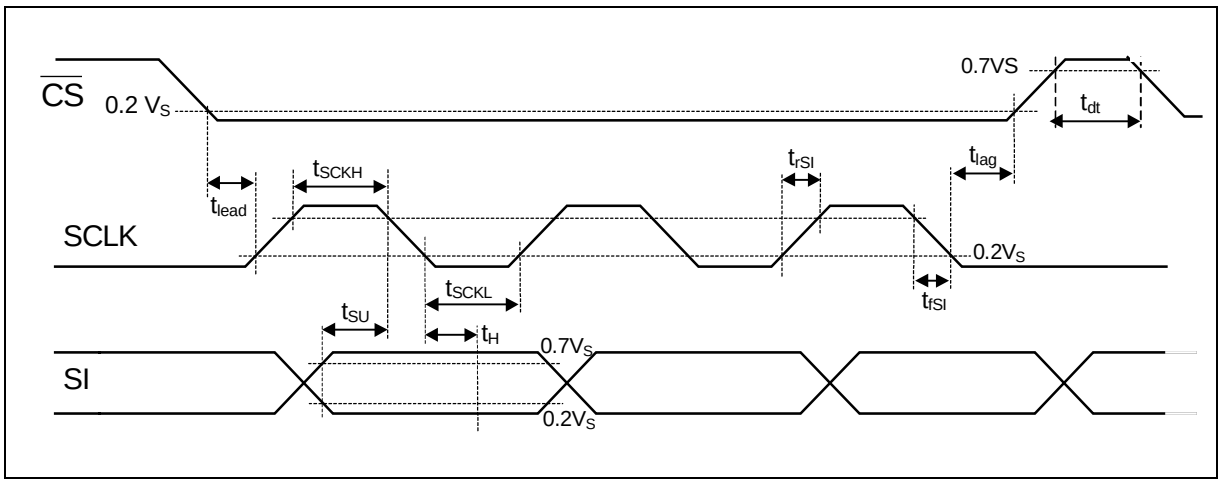


Figure 3: Input Timing Diagram

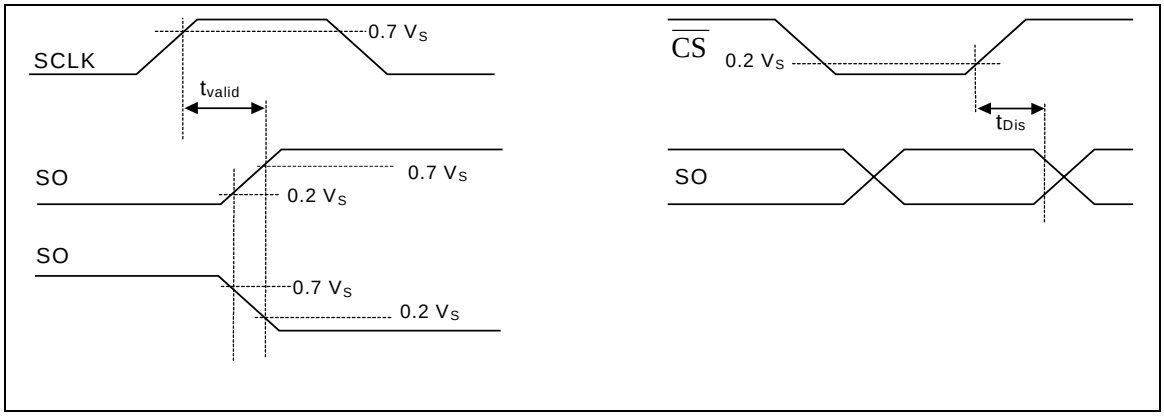


Figure 4:
SO Valid Time Waveforms **Enable and Disable Time Waveforms**

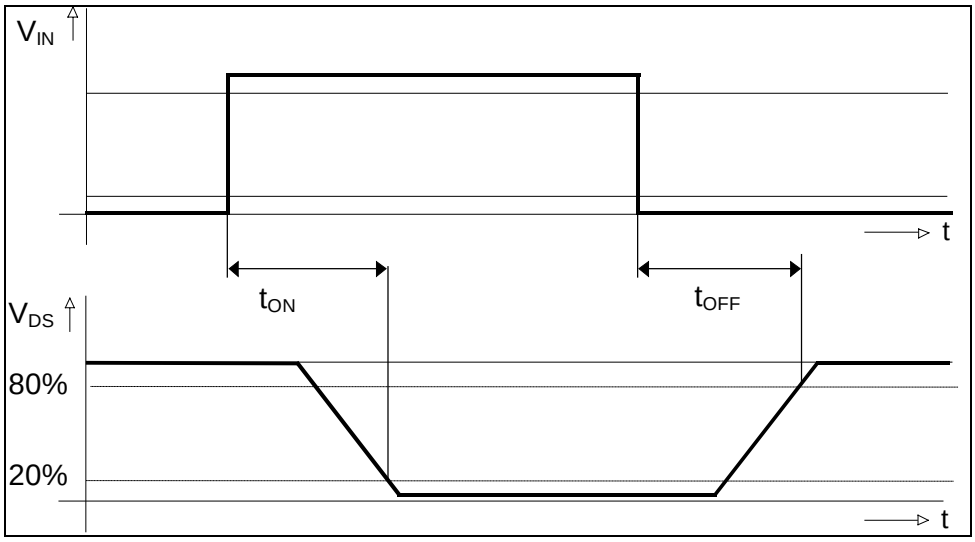
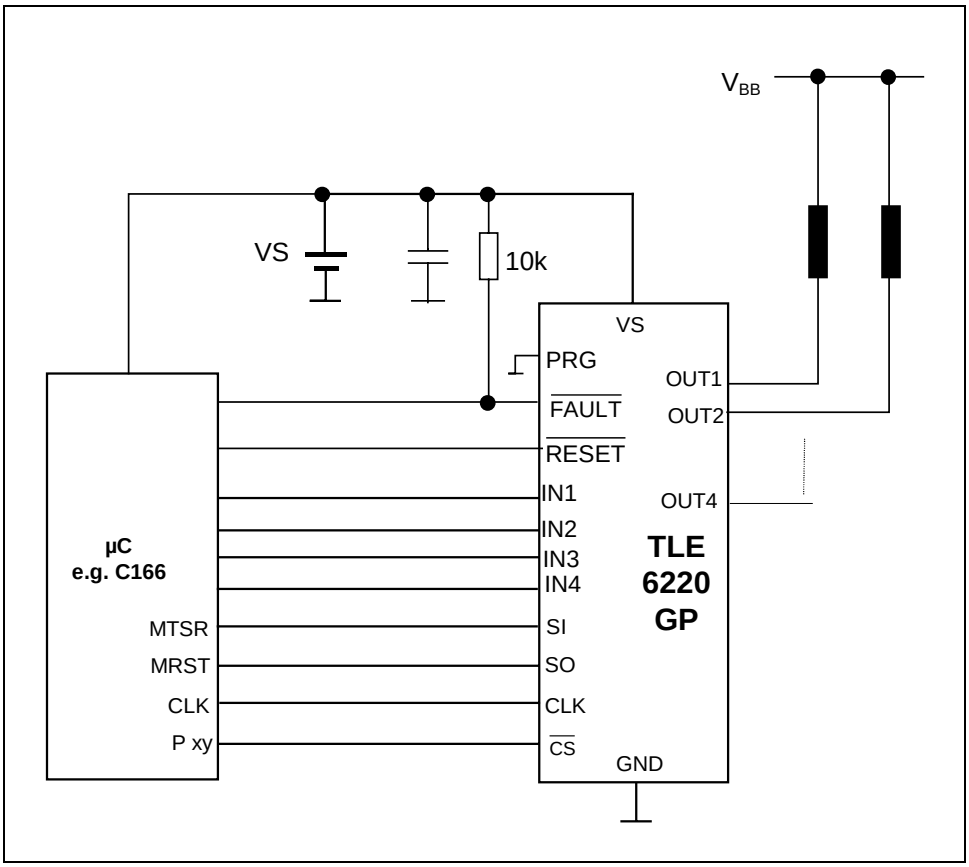


Figure 5: Power Outputs

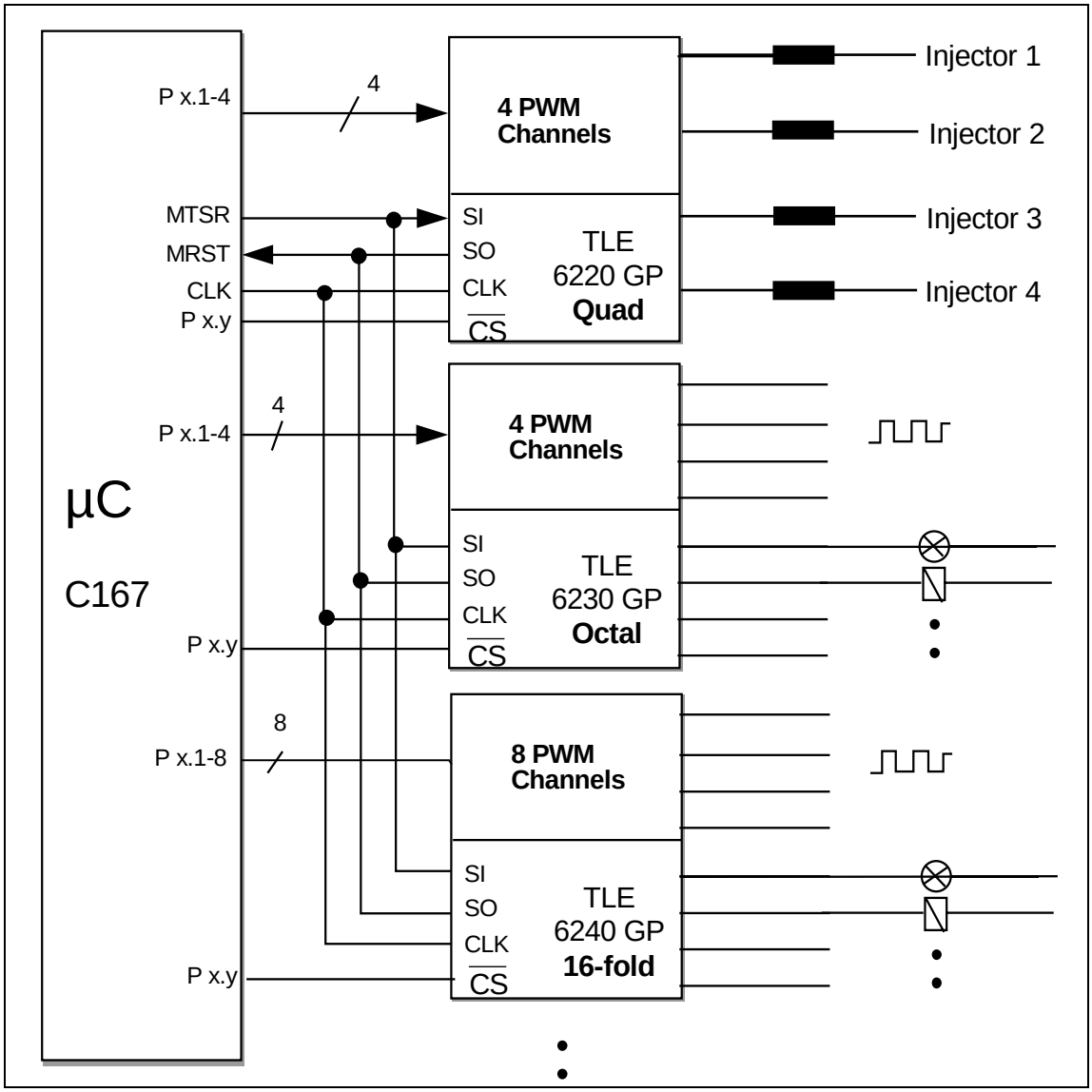
Application Circuit



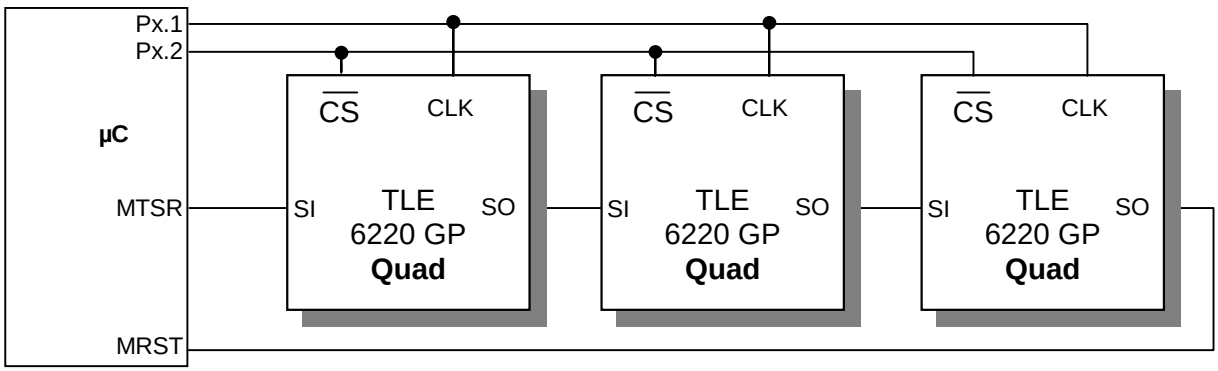
Parallel SPI Configuration

Engine Management Application

TLE 6230 GP in combination with TLE 6240 GP (16-fold switch) for relays and general purpose loads and TLE 6220 GP (quad switch) to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled direct in parallel for PWM applications.



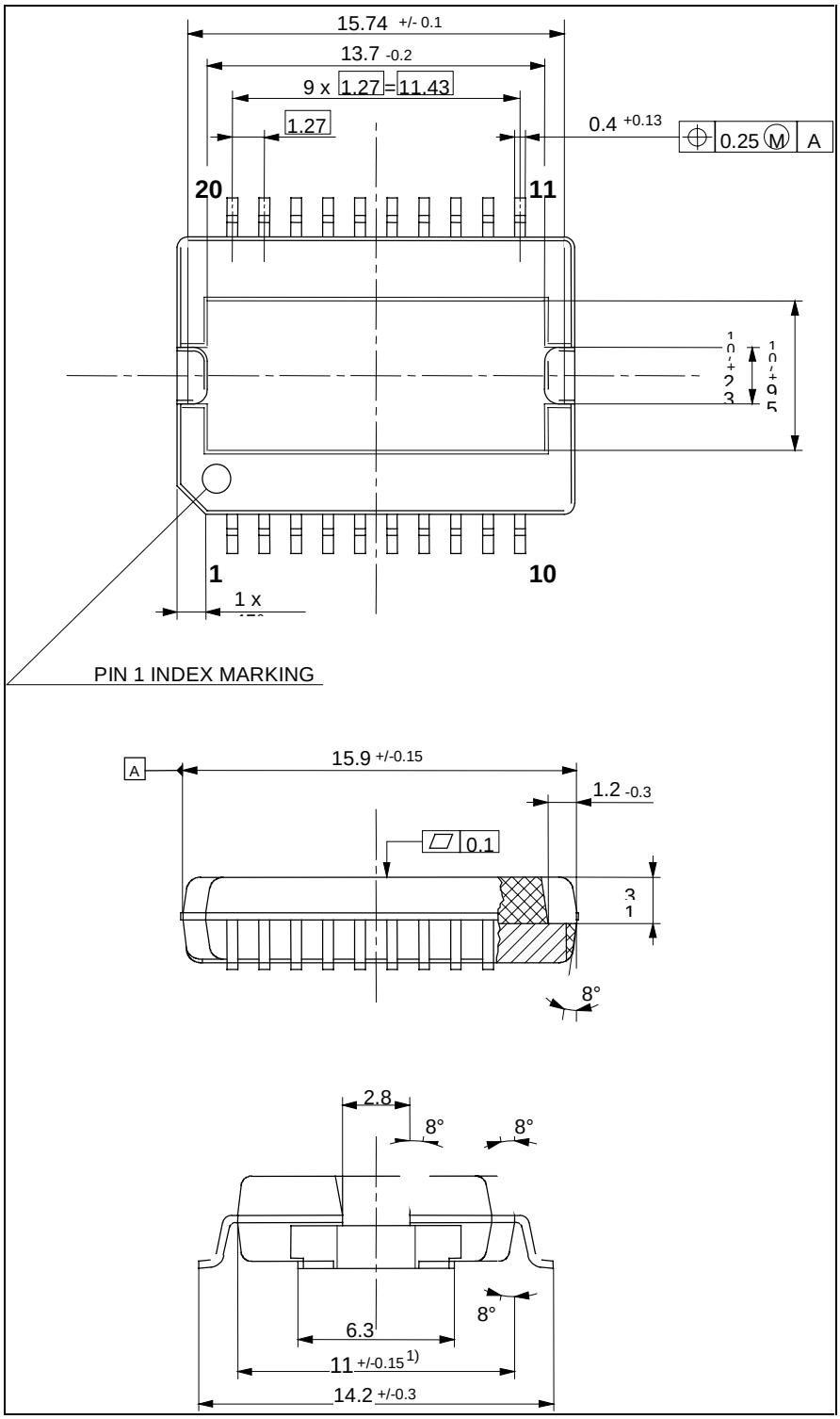
Daisy Chain Application TLE 6220 GP



Package and Ordering Code

(all dimensions in mm)

P - DSO - 20 - 10	Ordering Code
TLE 6220 GP	Q67006-A9315



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