Wireless Components

ASK Super Heterodyne Receiver

TDA 5200 V1.0

Specification June 1999

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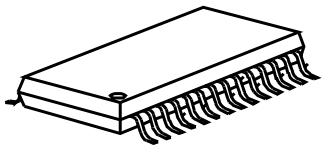
Productinfo

General Description

The IC is a very low power consumption single chip ASK Superheterodyne Receiver (SHR) for the frequency bands 868-870 MHz and 433-435 MHz. The SHR offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (I_S=4.8mA typ)
- Supply voltage range 5V±10%
- Power down mode with very low supply current (80nA typ)
- Fully integrated VCO and PLL Synthesizer
- RF input sensitivity < -105 dBm
- Selectable frequency ranges 868-870 MHz and 433-435 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7 MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Applications

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5200		P-TSSOP-28-1

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

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2.2 Application

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- Remote Control Systems
- Alarm Systems
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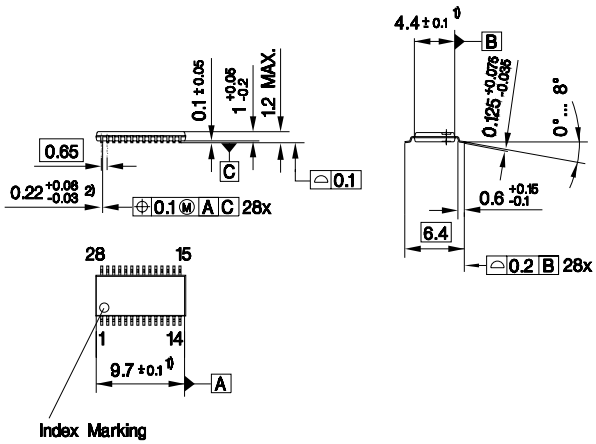
2.4 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

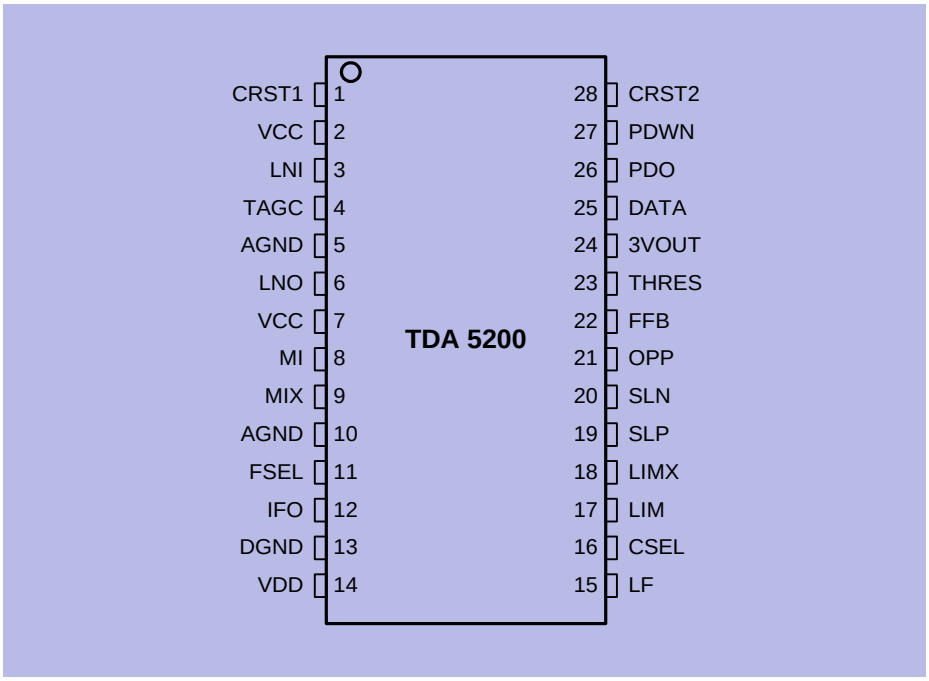
Figure 2-1 P-TSSOP-28-1

(Plastic Package)

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

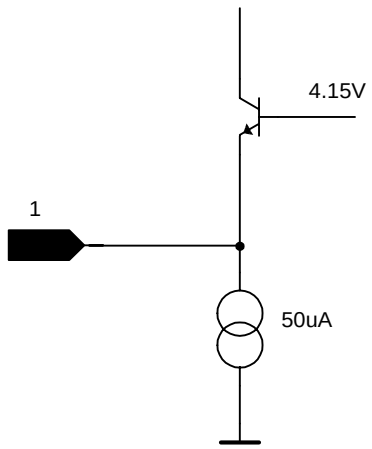
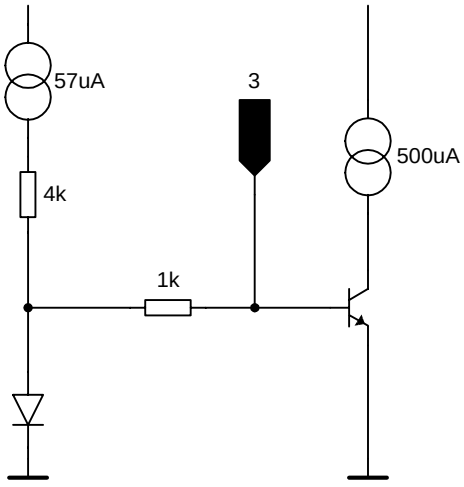


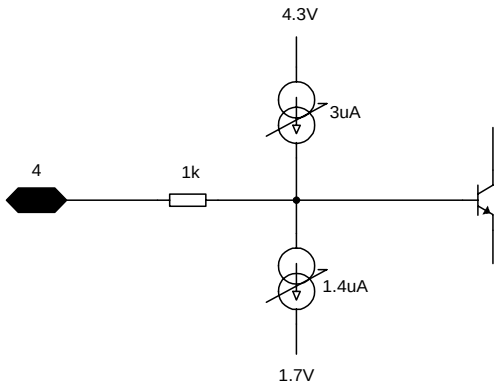
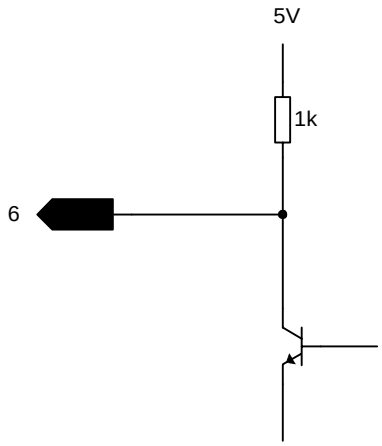
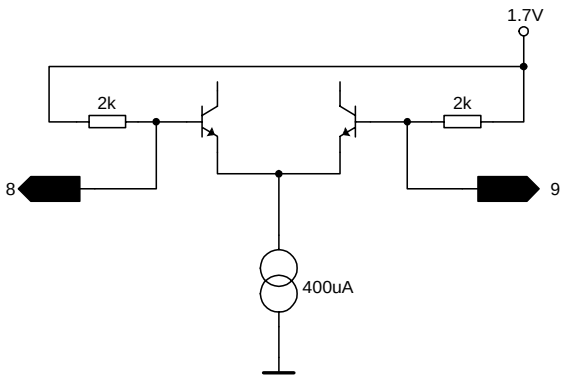
Pin_Configuration.wmf

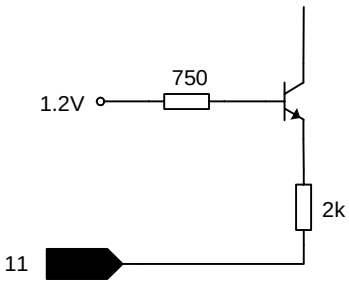
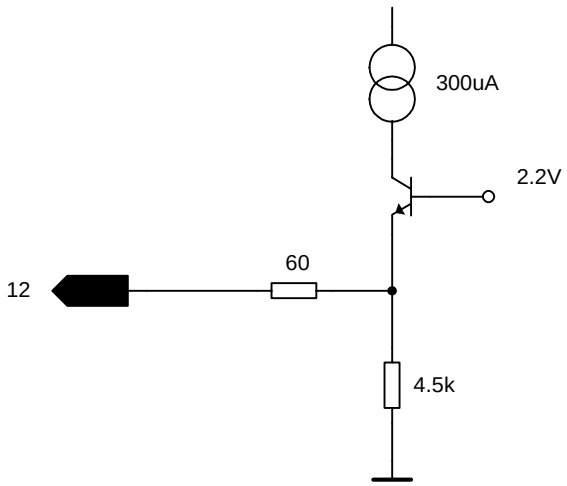
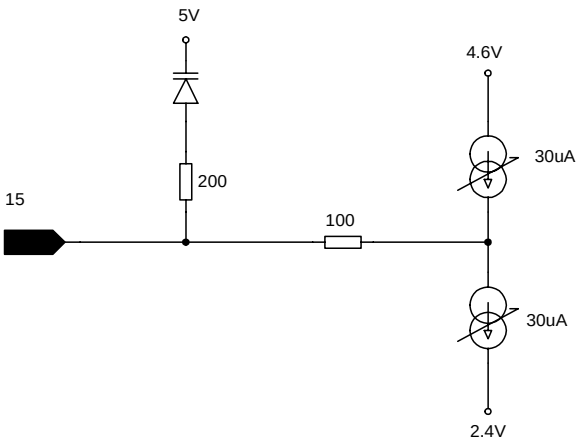
Figure 3-1 IC Pin Configuration

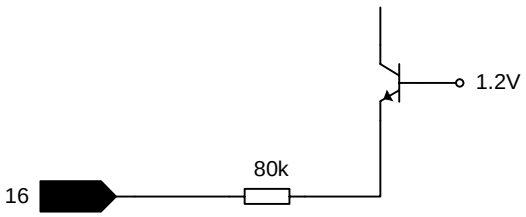
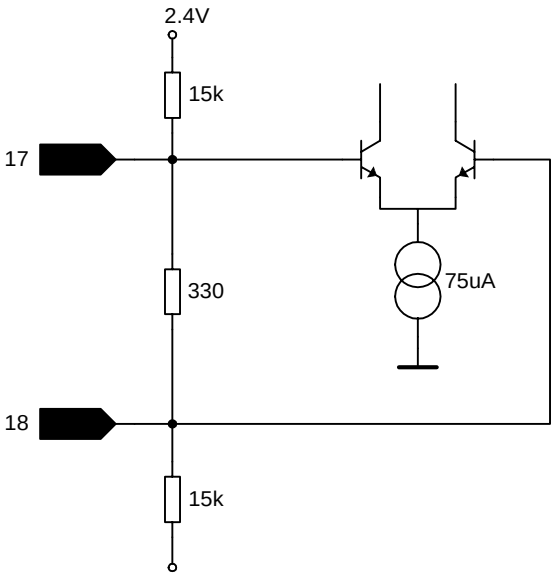
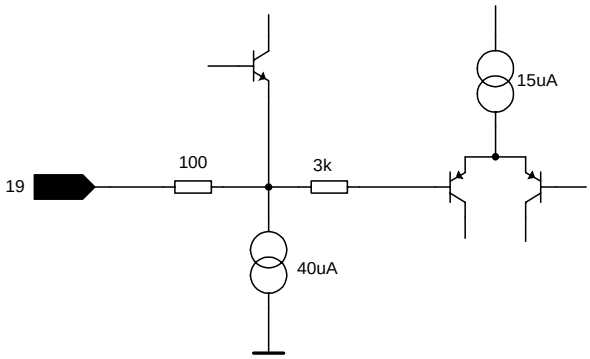
3.2 Pin Definition and Function

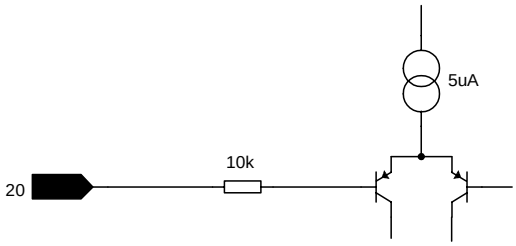
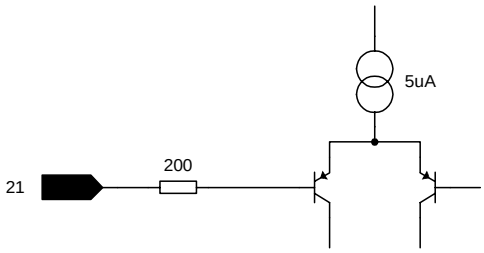
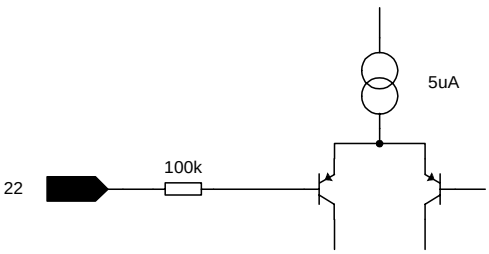
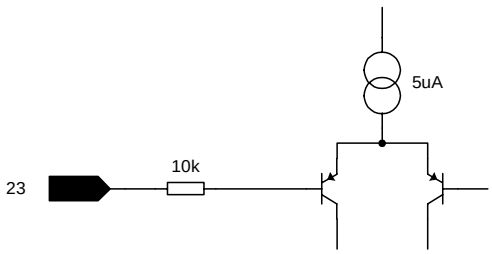
Table 3-1 Pin Definition and Function

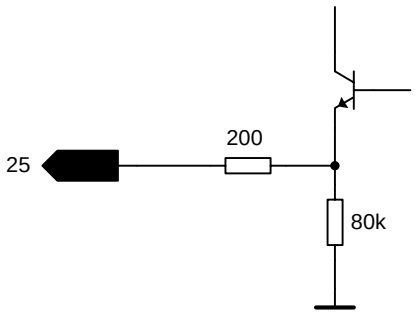
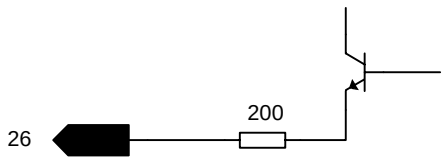
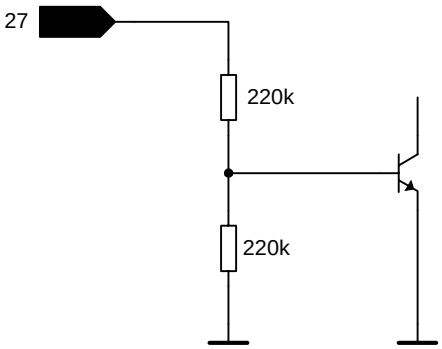
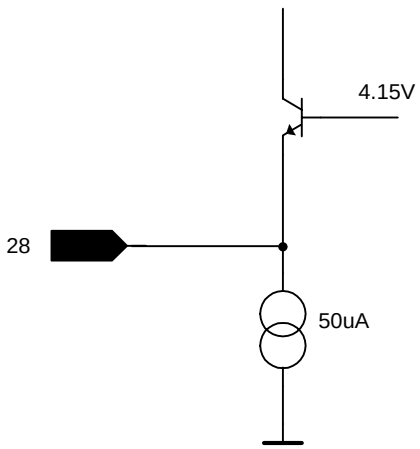
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return

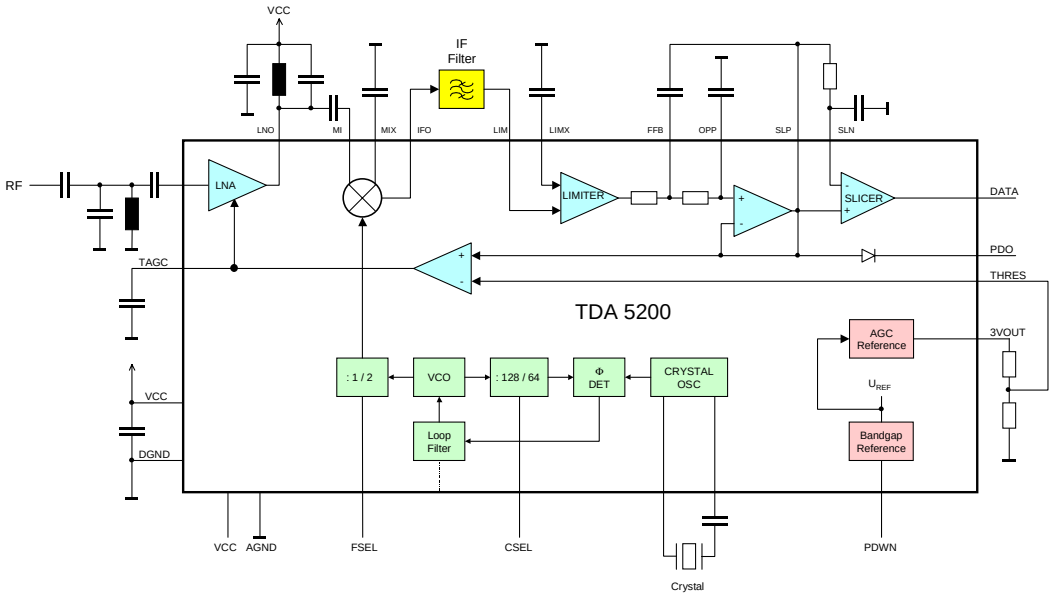
11	FSEL		869/434 MHz Operating Frequency Selector
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	LF		PLL Filter Access Point

16	CSEL		6.xx or 13.xx MHz Quartz Selector
17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input

20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output

25	DATA		Data Output
26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram



Functional_diagram.wmf

Figure 3-2 Main Block Diagram

3.4 Functional Blocks

1. Low noise amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 - 20dB. The gain figure is determined by the external matching network situated between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3.2dB, the current consumption is 500µA. The gain can be reduced by 17dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in chapter 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appro-

priate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and threshold voltage is described in chapter 4.1.

2. Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 433-435MHz/868-870MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB. A low pass filter with a corner frequency of 20MHz is built on chip in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3. PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 852MHz. No additional components are necessary. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. In case of operation in the 433 - 435 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin **FSEL** (Pin 11) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below). The loop filter is also realised fully on-chip.

Table 3-2

FSEL	RF Frequency
Open	433 - 435 MHz
Shorted to ground	868 - 870 MHz

4. Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 6 and 13MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-3

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

5. Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80dB that has a bandpass-characteristic centred around 10.7MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in figure 5.4.2. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 17dB in case the input signal strength is too strong as described in chapters 3.4.1 and 4.1.

6. Data Filter

The data filter comprises an OP-Amp with a bandwidth greater than 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in chapter 4.2.

7. Data Slicer

The data slicer is a fast comparator for a maximum data rate of >10kbaud. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in chapter 4.5.

8. Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is 500µA.

9. Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA .

Table 3-4

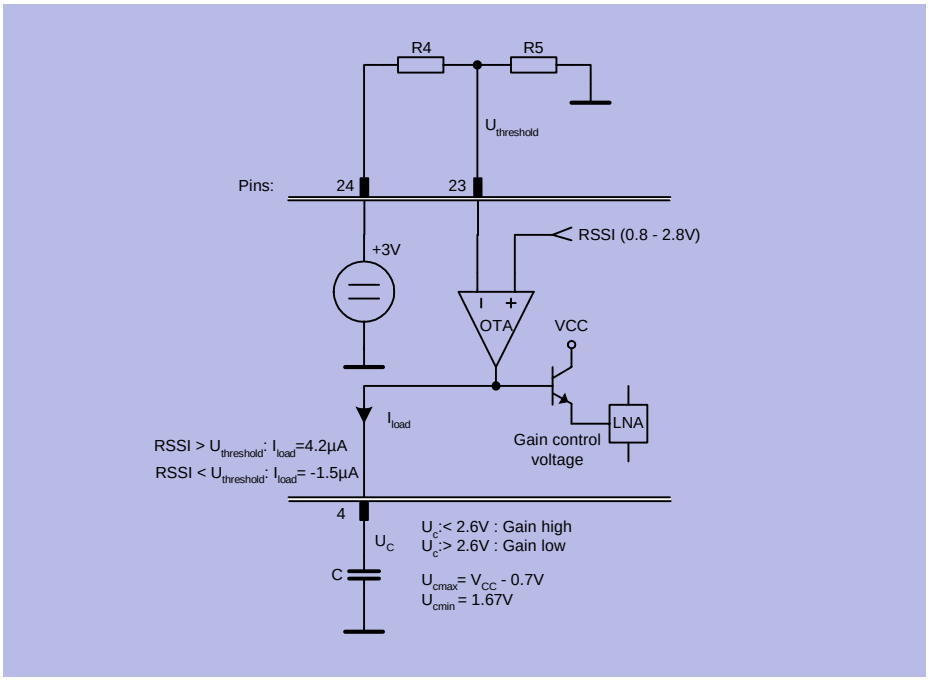
PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

Contents of this Chapter

4.1 Choice of LNA threshold voltage and time constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA_autom.wmf

Figure 4-1 LNA automatic gain control circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

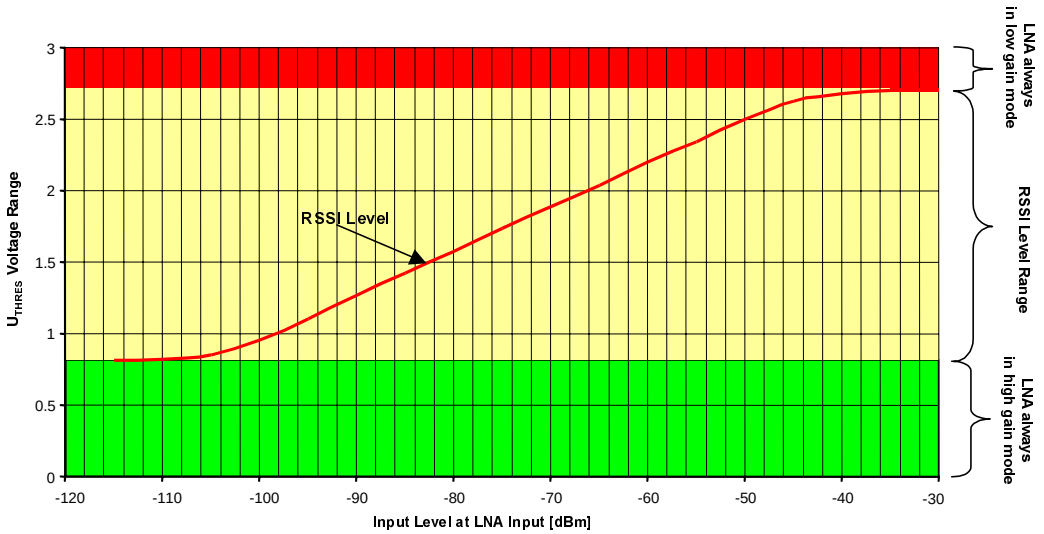


Figure 4-2 RSSI Level and permissive AGC threshold levels

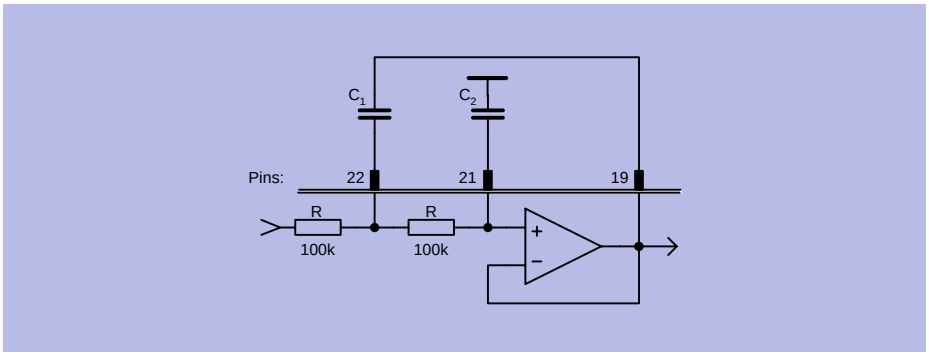
This voltage U_{thres} is applied to the **THRES** pin (Pin 23). The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in an upcoming Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50µA, but that the THRES pin input current is only in the region of 40nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. R4 can be chosen as 120kΩ, R5 as 180kΩ to yield an overall 3VOUT output current of 10µA.

As stated above the capacitor connected to the TAGC pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Siemens the capacitor value should be greater than 47nF. The optimum choice shall be described in the above mentioned upcoming Application Note.

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas.



Filter_Design.wmf

Figure 4-3 Data Filter Design

(1) (2)

$$C1 = \frac{2Q}{R\omega_{3dB}} \qquad C2 = \frac{1}{2QR\omega_{3dB}}$$

with

$\omega_{3dB} = 2\pi\int 3dB\zeta$ (3) the 3dB cut-off frequency

where

in case of a Bessel filter Q = 0.577 and ζ = 1.732

and

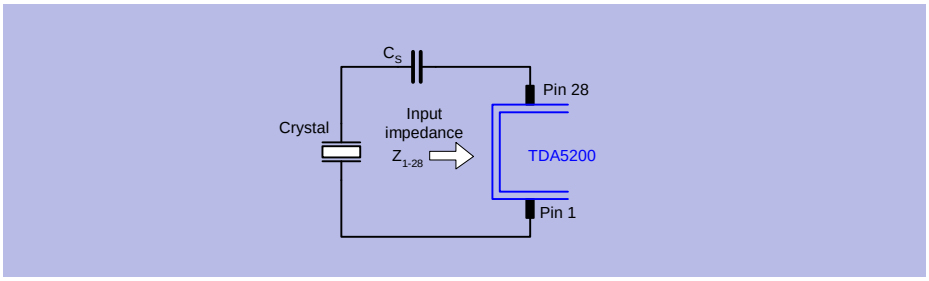
in case of a Butterworth filter Q = 0.71 and ζ = 1.0

Example: Butterworth filter with f_{3dB} = 6kHz : C_1 = 377pF

C_2 = 187pF

4.3 Quartz load capacitance calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in chapter 5.3 and by the quartz specifications given by the quartz manufacturer.



Quartz_load.wmf

Figure 4-4 Determination of series capacitance value for the quartz oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with C_l the load capacitance (refer to the quartz crystal specification).

Examples:

6.78 MHz:	C_L = 16 pF	X_L=750 Ω	C_S = 10.6 pF
13.56 MHz:	C_L = 16 pF	X_L=1250 Ω	C_S = 5.9 pF

4.4 Quartz frequency calculation

The quartz frequency is calculated by using the following formula:

$f_{QU} = (f_{RF} \pm 10.7) / r$ (1),

with
- f_{RF} .... receive frequency
- f_{LO} .... local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)
- f_{QU} .... quartz oscillator frequency
- r .... ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table.

Table 4-1

FSEL	CSEL	Ratio r = (f_{LO}/f_{QU})
open	open	64
open	GND	32
GND	open	128
GND	GND	64

Subtraction of 10.7 occurs in case the receive frequency is higher than the intended local oscillator frequency, addition in case the receive frequency lies below the local oscillator frequency.

Examples:

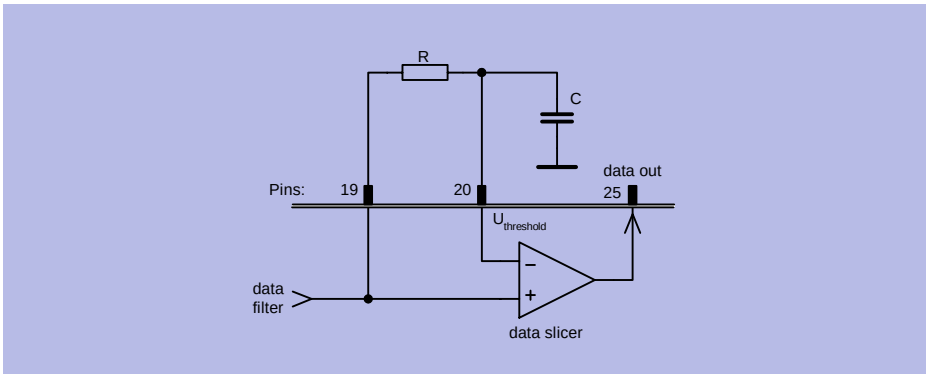
$$f_{QU} = (868.28\,MHz - 10.7\,MHz)/64 = 13.3997\,MHz$$

$$f_{QU} = (868.28\,MHz - 10.7\,MHz)/128 = 6.6998\,MHz$$

$$f_{QU} = (433.92\,MHz - 10.7\,MHz)/32 = 13.2256\,MHz$$

4.5 Data slicer threshold generation

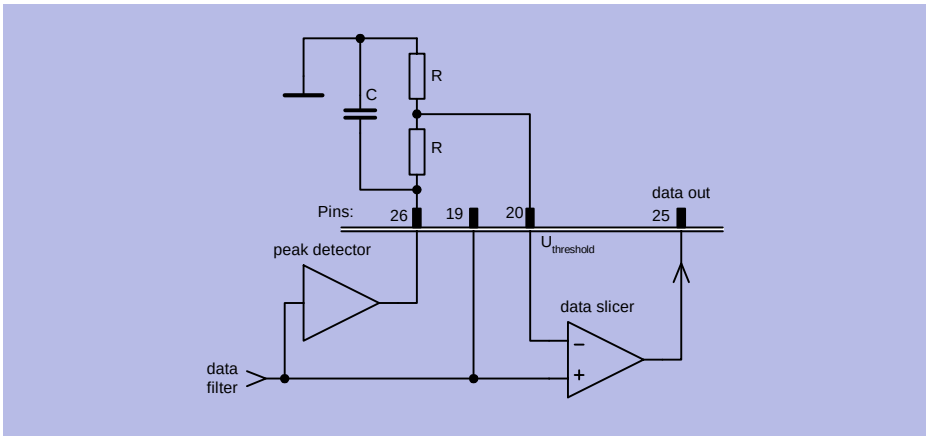
The threshold of the data slicer can be generated in two ways, depending on the signal coding scheme used. In case of a signal coding scheme without DC content such as Manchester coding the threshold can be generated using an external R-C integrator as shown in the following . The cut-off frequency of the R-C integrator has to be lower than the lowest frequency appearing in the data signal. In order to keep distortion low, the minimum value for R is 20kΩ.



Data_slice1.wmf

Figure 4-5 Data slicer threshold generation with external R-C integrator

Another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.



Data_slice2.wmf

Figure 4-6 Data slicer threshold generation utilising the peak detector

5 Reference

Contents of this Chapter

5.1 Absolute Maximum Ratings

The maximum ratings may not be exeeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Ambient temperature T_{amb} = -40°C .. +85°C

Table 5-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Supply Voltage	V_S	-0.3	5.5	V	
Junction Temperature	T_j	-40	+150	°C	
Storage Temperature	T_s	-40	+125	°C	
Thermal Resistance	R_{thJA}		114	K/W	
ESD integrity, all pins	V_{ESD}	-2	+2	kV	HBM according to MIL STD 883D, method 3015.7

5.2 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC limits are not guaranteed.

Supply voltage V_S = 4.5 V .. 5.5 V

Ambient temperature T_{amb} = -40°C .. +85°C

Table 5-2

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Receiver Input Level	RF_{in}	-107	-13	dBm	@Source Impedance 50Ω, BER 2E-3
LNI Input Frequency	f_{RF}	433/868	435/870	MHz	
MI/X Input Frequency	f_{MI}	433/868	435/870	MHz	
3dB IF Frequency Range	$f_{IF\ -3dB}$	5	23	MHz	IF centred around 10.7 MHz
Powerdown Mode On	$PWDN_{ON}$	0	0.8	V	
Powerdown Mode Off	$PWDN_{OFF}$	2	V_S	V	
Gain Control Voltage, LNA high gain state	V_{TAGC_H}	1.5	2.5	V	
Gain Control Voltage, LNA low gain state	V_{TAGC_L}	2.6	VS-0.7V	V	

5.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. All specifications measured with Infineon Evaluation Board as shown in chapter 5.5.
Supply voltage V_S = 4.5V ... 5.5V, Ambient temperature T_{amb} = +25°C

Table 5-3

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Supply Current						
Supply current, standby mode	$I_{S\ PDWN}$		50		nA	Pin 27 (PDWN) open or tied to 0 V
Supply current, device operating in 869 MHz range	$I_{S\ REC}$		4.8		mA	Pin 11 (FSEL) tied to GND
Supply current, device operating in 434 MHz	$I_{S\ REC}$		4.6		mA	Pin 11 (FSEL) open
LNA, Signal Input LNI (PIN 3), V_{TAGC} < 2.6V, high gain mode						
Input impedance, f_{RF} = 434 MHz	$S_{11\ LNA}$		0.762/-34.7 deg			
Input impedance, f_{RF} = 869 MHz	$S_{11\ LNA}$		0.544/-73.5 deg			
Input level @ 1dB compression	$P1dB_{LNA}$		t.b.d.		dBm	
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{LNA}$		-10		dBm	matched input
Input 3rd order intercept point f_{RF} = 869 MHz	$IIP3_{LNA}$		-15		dBm	matched input
LO signal feedthrough	LO_{LNI}		-84		dBm	
LNA, Signal Output LNO (PIN 6), V_{TAGC} < 2.6V, high gain mode						
Output impedance, f_{RF} = 434 MHz	$S_{22\ LNA}$		0.785/-12.9 deg			
Output impedance, f_{RF} = 869 MHz	$S_{22\ LNA}$		0.750/-24.2 deg			
Gain f_{RF} = 434 MHz	$S_{21\ LNA}$		2.28/138.2 deg			
Gain f_{RF} = 869 MHz	$S_{21\ LNA}$		2.02/101.7 deg			
Voltage Gain Antenna to MI f_{RF} = 434 MHz	G_{AntMI}		t.b.d.		dB	
Voltage Gain Antenna to MI f_{RF} = 869 MHz	G_{AntMI}		t.b.d.		dB	
Noise Figure	NF_{LNA}		t.b.d.		dB	

LNA, Signal Input LNI, V_{TAGC} > 2.6V, low gain mode						
Input impedance, f_{RF}=434 MHz	S_{11LNA}		0.809/-35.4 deg			
Input impedance, f_{RF}=869 MHz	S_{11LNA}		0.595/-80.2 deg			
Input level @ 1dB compression	$P1dB_{LNA}$		t.b.d.		dBm	
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{LNA}$		-13		dBm	
Input 3rd order intercept point f_{RF} = 869 MHz	$IIP3_{LNA}$		-7		dBm	
LNA, Signal Output LNO, V_{TAGC} > 2.6V, low gain mode						
Output impedance, f_{RF}=434 MHz	S_{22LNA}		0.804/-13.6 deg			
Output impedance, f_{RF}=869 MHz	S_{22LNA}		0.753/-26.3 deg			
Gain f_{RF} = 434 MHz	$S_{21\ LNA}$		0.034 / 140.6 deg			
Gain f_{RF} = 869 MHz	$S_{21\ LNA}$		0.032 / 109.1deg			
Voltage Gain Antenna to MI f_{RF} = 434 MHz	G_{AntMI}		t.b.d.		dB	
Voltage Gain Antenna to MI f_{RF} = 869 MHz	G_{AntMI}		t.b.d.		dB	
Noise Figure	NF_{LNA}		t.b.d.		dB	
LNA, Signal 3VOUT (PIN 24)						
Output voltage	V_{3VOUT}		3		V	
Current out	I_{3VOUT}			50	µA	
LNA, Signal THRES (PIN 23)						
Input Voltage range	V_{THRES}	0		V_S-1V	V	see chapter 4.1
LNA low gain mode	V_{THRES}			V_S-1V	V	or shorted to Pin 24
LNA high gain mode	V_{THRES}	0			V	or open
Current in	I_{THRES_in}		50		nA	
LNA, Signal TAGC (PIN 4)						
TAGC output voltage, LNA low gain state	V_{TAGC_L}	2.6		V_S-0.7V	V	RSSI > V_{THRES}
TAGC output voltage, LNA high gain state	V_{TAGC_H}	1.67		2.6	V	RSSI < V_{THRES}
Current out, LNA low gain state	I_{TAGC_out}		4.2		uA	RSSI > V_{THRES}
Current in, LNA high gain state	I_{TAGC_in}		1.5		uA	RSSI < V_{THRES}

Mixer, Signal Input MI/MIX (PINS 8/9)						
Input impedance f_{RF} = 434 MHz	$S_{11\ MIX}$		0.888 / -14.4 deg			
Input impedance f_{RF} = 869 MHz	$S_{11\ MIX}$		0.842 / -28.1 deg			
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{MIX}$		-28		dBm	
Input 3rd order intercept point f_{RF} = 869 MHz	$IIP3_{MIX}$		-26		dBm	
LO signal feedthrough f_{RF} = 434 MHz	LO_{MI}		-74		dBm	MI open input voltage
LO signal feedthrough f_{RF} = 869 MHz	LO_{MI}		-60		dBm	MI open input voltage
MIXER, Signal Output IFO (PIN 12)						
Output impedance	Z_{IFO}		330		Ω	
Conversion Voltage Gain f_{RF} = 434 MHz	G_{MIX}		+19		dB	
Conversion Voltage Gain f_{RF} = 869 MHz	G_{MIX}		+18		dB	
Noise Figure, SSB (~ DSB NF+3dB)	NF_{MIX}		t.b.d.		dB	
RF to IF isolation	A_{RF-IF}		t.b.d.		dB	
LIMITER, Signal Input LIM/X (PIS 17/18)						
Input Impedance	Z_{LIM}		330		Ω	
RSSI dynamic range	DR_{RSSI}	60		80	dB	
RSSI linearity	LIN_{RSSI}		±1		dB	
Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz	
DATA FILTER						
Useable bandwidth	$BW_{BB\ FILT}$	10			kHz	
RSSI Level at Data Filter Output SLP, RF_{IN} = -103dBm	$RSSI_{low}$	0.9			V	LNA in high gain mode
RSSI Level at Data Filter Output SLP, RF_{IN} > -30dBm	$RSSI_{high}$			2.8	V	LNA in low gain mode
DATA SLICER, Signal Output DATA (PIN 25)						
Useable bandwidth	$BW_{BB\ SLIC}$		10		kHz	
Capacitive loading of output	$C_{max\ SLIC}$			20	pF	
LOW output voltage	V_{SLIC_L}		0		V	

HIGH output voltage	V_{SLIC_H}			Vs-1 V	V	
Output current	I_{SLIC_out}			200	µA	
PEAK DETECTOR, Signal Output PDO (PIN 26)						
LOW output voltage	V_{SLIC_L}		0		V	
HIGH output voltage	V_{SLIC_H}			V_S-1	V	
Load current	I_{load}			500	uA	
Leakage current	$I_{leakage}$		50		nA	
Crystal Oscillator, Signals CRSTL1, CRSTL2 (PINS 1/28)						
Operating frequency	f_{CRSTL}	6		14	MHz	fundamental mode, series resonance
Input Impedance @ ~6MHz	$Z_{1\text{-}28}$		-900 +j750		Ω	
Input impedance @ ~13MHz	$Z_{1\text{-}28}$		-450 +j1250		Ω	
Serial Capacity @ ~ 6MHz	$C_{S\,6}$ = C1		10.6		pF	
Serial Capacity @ ~ 13MHz	C_{S13}= C1		5.6		pF	
PLL, Signal LF (PIN 15)						
Tuning Voltage relative to V_S	V_{TUNE}	0.4	1.6	2.4	V	
POWER DOWN MODE, Signal PDWN (PIN 27)						
Powerdown Mode On	PWD-N_{ON}	0		0.8	V	
Powerdown Mode Off	PWD-N_{OFF}	2.8		V_S	V	
Input bias current PDWN	I_{PDWN}		20		uA	
Start-up Time until valid IF signal is detected	T_{su}		1		mS	
VCO MULTIPLEXER, Signal FSEL (PIN 11)						
f_{RF} range 434MHz	V_{FSEL}	1.4		4	V	or open
f_{RF} range 869MHz	V_{FSEL}	0		0.2	V	
Input bias current FSEL	I_{FSEL}		200		uA	FSEL tied to GND
PLL DIVIDER, Signal CSEL (PIN 16)						
f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4		4	V	or open
f_{CRSTL} range 13.xxMHz	V_{CSEL}	0		0.2	V	
Input bias current CSEL	I_{CSEL}		5		uA	CSEL tied to GND

5.4 Test Circuit

The device performance parameters were measured on a Infineon test PCB.

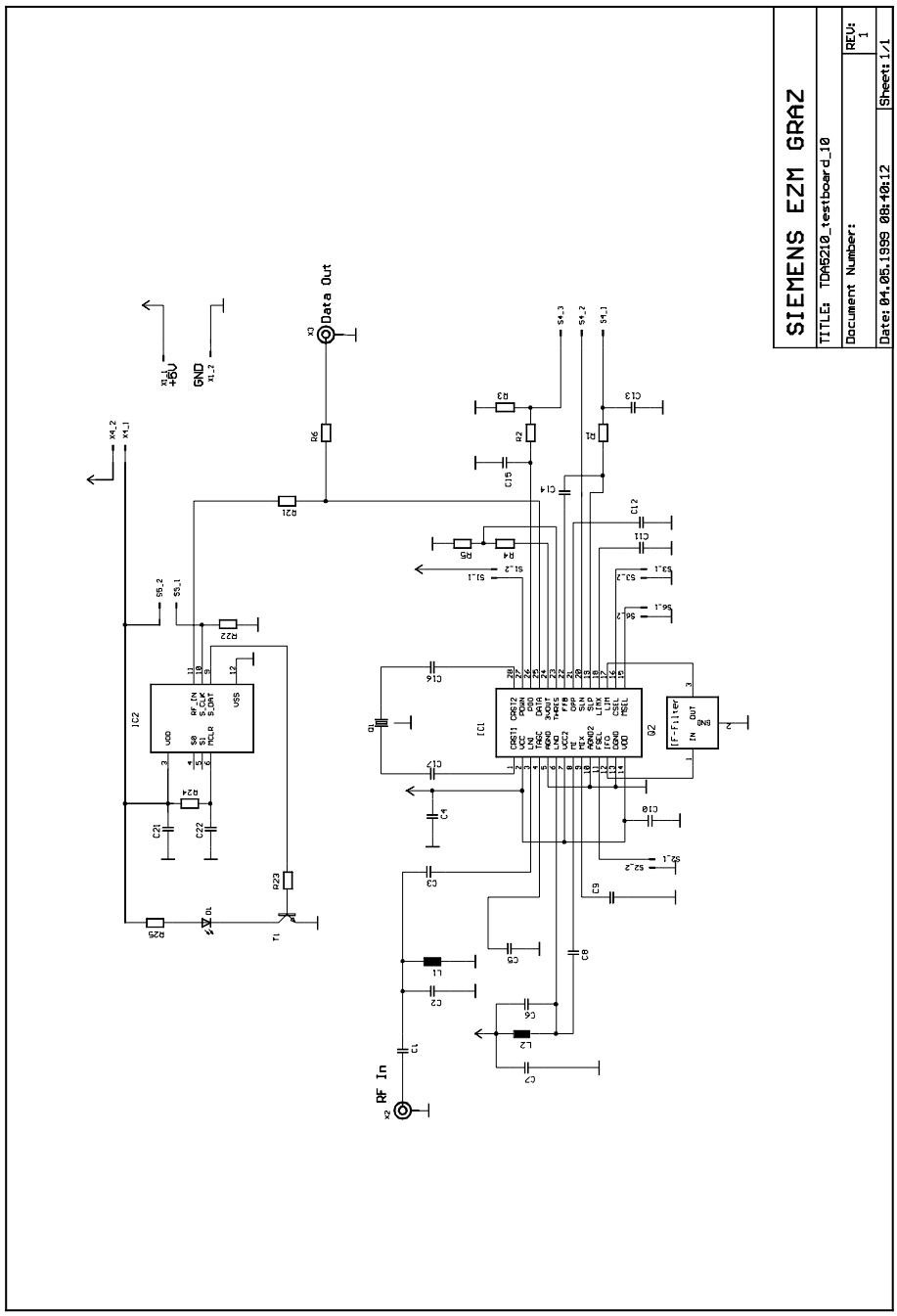


Figure 5-1 Schematic

Note: The reference designator have changed with respect to the previous version of the specification.

5.5 Test Board Layouts

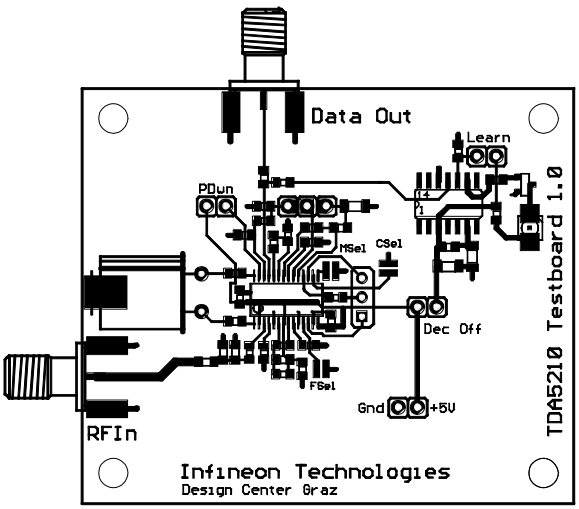


Figure 5-2 Top Side

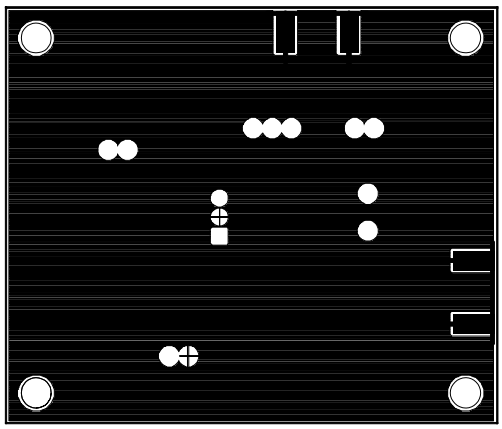


Figure 5-3 Bottom Side

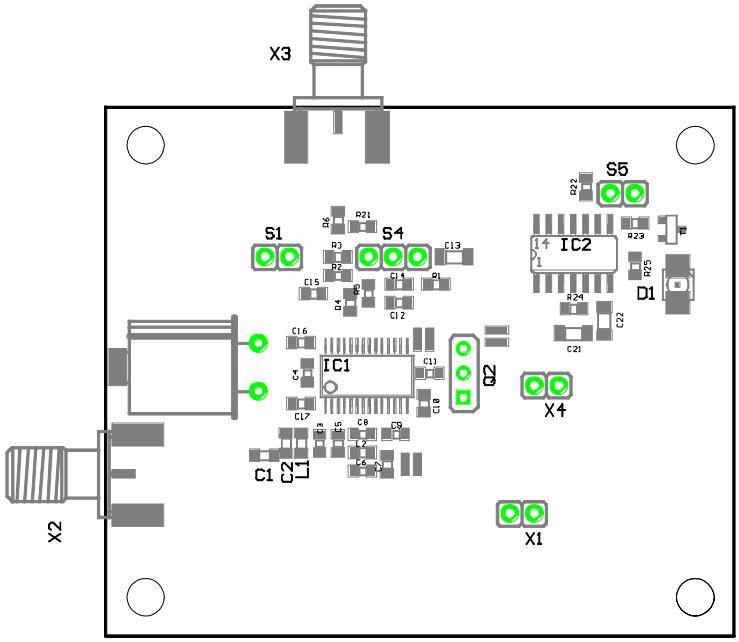


Figure 5-4 Component Placement

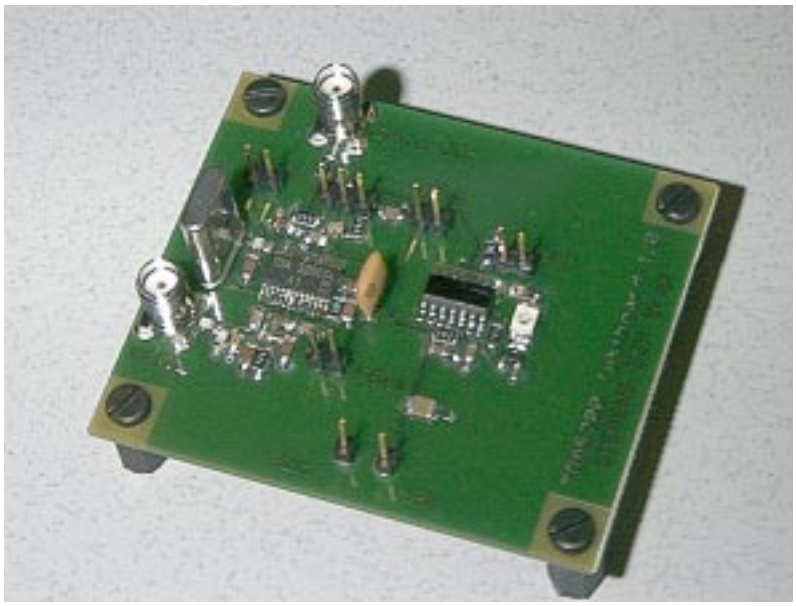


Figure 5-5 Photograph of Evaluation Board

5.6 Bill of Materials

The following components are necessary for evaluation of the TDA5200 without use of a Microchip HCS515 decoder.

Table 5-4

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R4	120kΩ	0805, ± 5%
R5	180kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	434 MHz: 10nH 869 MHz:3.9nH	Toko, PTL2012-F Toko, PTL2012-F
L2	434 MHz: 15nH 869 MHz:3.3nH	Toko, PTL2012-F Toko, PTL2012-F
C1	1pF	0805, COG, ± 0.1pF, Philips, Samsung
C2	434 MHz: 4.7pF 869 MHz:3.9pF	0805, COG, ± 0.1pF, Philips, Samsung 0805, COG, ± 0.1pF, Philips, Samsung
C3	434 MHz: 6.8pF 869 MHz:5.6pF	0805, COG, ± 0.1pF, Philips, Samsung 0805, COG, ± 0.1pF, Philips, Samsung
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	434 MHz: 8.2pF 869 MHz:3.9pF	0805, COG, ± 0.1pF, Philips, Samsung 0805, COG, ± 0.1pF, Philips, Samsung
C7	100pF	0805, COG, ± 5%
C8	434 MHz: 33pF 869 MHz:22pF	0805, COG, ± 5% 0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	470pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	220pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 5%
C16	8.2pF	0805, COG, ± 0.1pF, Philips, Samsung
C17	434 MHz: 12pF 869 MHz:18pF	0805, COG, ± 5% 0805, COG, ± 5%
Q2	(f_{RF} – 10.7MHz)/32 or (f_{RF} – 10.7MHz)/64	HC49/U, fundamental mode, CL = 12pF, e.g. 434.2MHz: Jauch Q 13,23437-S11-1323-12-10/20 e.g. 868.4MHz: Jauch Q 13,40155-S11-1323-12-10/20
F1	SFE10.7MA5-A or SKM107M1-A20-10	Murata Toko

X2, X3	142-0701-801	Johnson
X1, X4, S1, S5		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5200	Infineon

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA5200 in conjunction with a Microchip HCS515 decoder.

Table 5-5

Ref	Value	Specification
R21	22kΩ	0805, ± 5%
R22	100kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560kΩ	0805, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS515	Microchip
T1	BC 847B	Siemens
D1	LS T670-JL	Siemens