



Features

- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier (P_{out} Typically 23 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF Typically 2.1 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components
- PSSO20 Plastic Package with Down-set Paddle Heat Slug or HP-VFQFP-N20 with Extended Performance and Flipchip Version

Electrostatic sensitive device.
Observe precautions for handling.

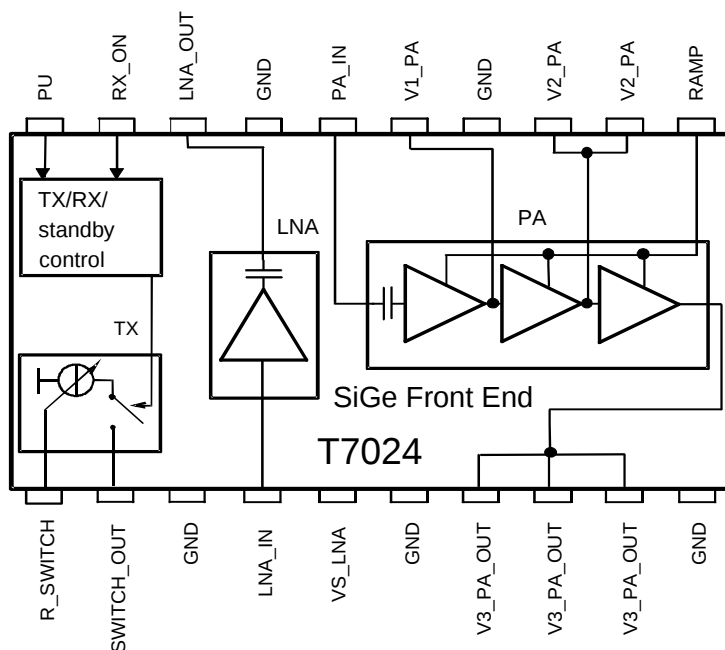


Description

The T7024 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth™, DECT, and many other ISM applications according to FCC part 15.

Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



Bluetooth™ /ISM 2.4-GHz Front- End IC

T7024

Preliminary



Pin Configuration

Figure 2. Pinning PSSO20

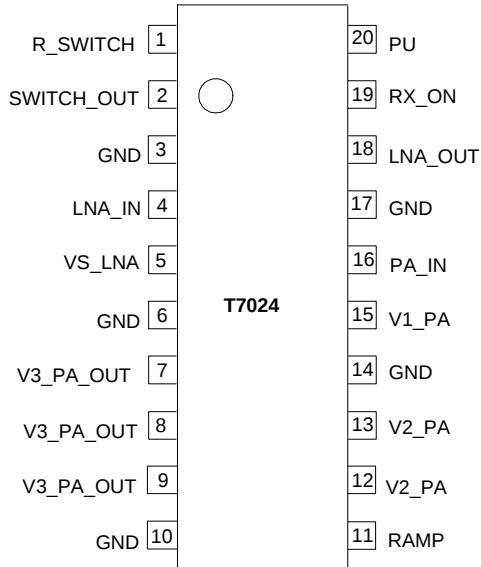
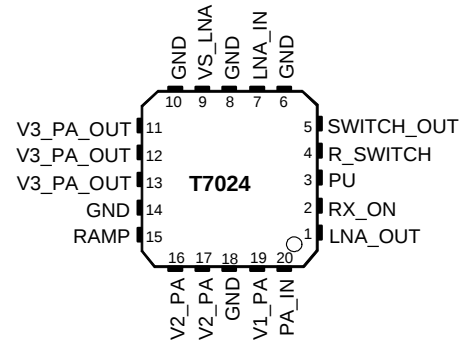
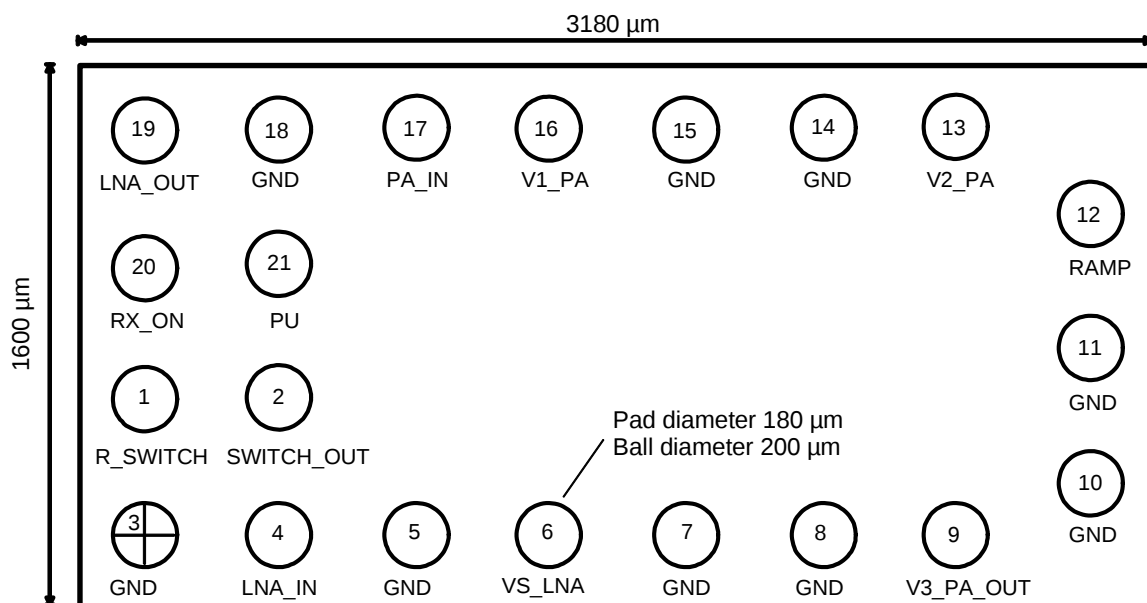


Figure 3. Pinning HP-VFQFP-N20



Pin Description

Pins PSSO20	Pins N20	Symbol	Function
1	4	R_SWITCH	Resistor to GND sets the PIN diode current
2	5	SWITCH_OUT	Switched current output for PIN diode
3	6	GND	Ground
4	7	LNA_IN	Low-noise amplifier input
5	9	VS_LNA	Supply voltage input for low-noise amplifier
6	8	GND	Ground
7	11	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
8	12	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
9	13	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
10	10	GND	Ground
11	15	RAMP	Power ramping control input
12	16	V2_PA	Inductor to power supply for power amplifier
13	17	V2_PA	Inductor to power supply for power amplifier
14	14	GND	Ground
15	19	V1_PA	Supply voltage for power amplifier
16	20	PA_IN	Power amplifier input
17	18	gnd	Ground
18	1	LNA_OUT	Low-noise amplifier output
19	2	RX_ON	RX active high
20	3	PU	Power-up active high
Slug	Slug	GND	Ground

Figure 4. Pad Location, Thickness: 450 μm 

Pad Description

Pad	Symbol	Function	X-Coordinate of Pad ⁽¹⁾ (μm)	Y-Coordinate of Pad ⁽¹⁾ (μm)
1	R_SWITCH	Resistor to GND sets the PIN diode current	0	400
2	SWITCH_OUT	Switched current output for PIN diode	400	400
3	GND	Ground	0	0
4	LNA_IN	Low-noise amplifier input	400	0
5	GND	Ground	800	0
6	VS_LNA	Supply voltage input for low-noise amplifier	1200	0
7	GND	Ground	1600	0
8	GND	Ground	2000	0
9	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output	2400	0
10	GND	Ground	2780	150
11	GND	Ground	2780	550
12	RAMP	Power ramping control input	2780	950
13	V2_PA	Inductor to power supply for power amplifier	2450	1200
14	GND	Ground	2050	1200
15	GND	Ground	1650	1200
16	V1_PA	Supply voltage for power amplifier	1250	1200
17	PA_IN	Power amplifier input	850	1200
18	GND	Ground	400	1200
19	LNA_OUT	Low-noise amplifier output	0	1200
20	RX_ON	RX active high	0	800
21	PU	Power-up active high	400	800

Note: 1. Relative to center of Pad 3.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage Pins VS_LNA, V1_PA, V2_PA, V3_PA_OUT	V_S	6	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
RF input power LNA	P_{inLNA}	5	dBm
RF input power PA	P_{inPA}	10	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient PSSOP20, slug soldered on PCB	R_{thJA}	19	K/W
Junction ambient HP-VFQFP-N20, slug soldered on PCB	R_{thJA}	27	K/W

Operating Range

All voltages are referred to ground (Pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The table represents the sum of all supply currents depending on the TX/RX mode.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply voltage Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current TX PSSO20	I_S		190		mA
N20	I_S		165		mA
RX	I_S		8		mA
Standby current PU = 0	$I_{S_standby}$		10		μA
Ambient temperature	T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3.0\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier ⁽¹⁾						
Supply voltage	Pins V1_PA, V2_PA, V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current	TX PSSO20 N20	I_{S_TX}		190		mA
	RX (PA off), $V_{\text{RAMP}} \leq 0.1\text{ V}$	I_{S_RX}			10	μA
Standby current	Standby	$I_{S_standby}$			10	μA
Frequency range	TX	f	2.4		2.5	GHz
Gain-control range	TX	ΔGp	60	42		dB
Power gain maximum	TX, Pin PA_IN to V3_PA_OUT	Gp	28	30	33	dB
Power gain minimum	TX, Pin PA_IN to V3_PA_OUT	Gp	-40		-17	dB
Ramping voltage maximum	TX, power gain (maximum) Pin RAMP	$V_{\text{RAMP max}}$	1.7	1.75	1.83	V
Ramping voltage minimum	TX, power gain (minimum) Pin RAMP	$V_{\text{RAMP min}}$		0.1		V
Ramping current maximum	TX, $V_{\text{RAMP}} = 1.75\text{ V}$, Pin RAMP	$I_{\text{RAMP max}}$			0.5	mA
Power-added efficiency	TX PSSO20 N20	PAE	30	35		%
		PAE	35	40		%
Saturated output power	TX, input power = 0 dBm referred to Pins V3_PA_OUT	P_{sat}	22.0	23	24.0	dBm
Input matching ⁽²⁾	TX, Pin PA_IN	Load VSWR		<1.5:1		
Output matching ⁽²⁾	TX, Pins V3_PA_OUT	Load VSWR		<1.5:1		
Harmonics at P 1dBCP	TX, Pins V3_PA_OUT	2 fo			-30	dBc
	TX, Pins V3_PA_OUT	3 fo			-30	dBc
T/R Switch Driver (Current Programming by External Resistor from R_SWITCH to GND)						
Switch-out current output	Standby, Pin SWITCH_OUT	$I_{S_O_standby}$			1	μA
	RX	$I_{S_O_RX}$			1	μA
	TX at 100 Ω	$I_{S_O_100}$		1.7		mA
	TX at 1.2 k Ω	$I_{S_O_1k2}$		7		mA
	TX at 33 k Ω	$I_{S_O_33k}$		17		mA
	TX at ∞	$I_{S_O_R}$		19		mA
Low-noise Amplifier ⁽³⁾						
Supply voltage	All, Pin VS_LNA	V_S	2.7	3.0	5.5	V
Supply current	RX	I_S		8	9	mA
Supply current (LNA and control logic)	TX (control logic active) Pin VS_LNA	I_S			0.5	mA

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, $Z_C = 50\ \Omega$.
 2. With external matching network, load impedance 50 Ω .
 3. Low-noise amplifier shall be unconditionally stable.
 4. With external matching components.

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_S = 3.0\text{ V}$, $T_{amb} = 25^\circ\text{C}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Standby current	Standby, Pin VS_LNA	$I_{S_standby}$		1	10	μA
Frequency range	RX	f	2.4		2.5	GHz
Power gain	RX, Pin LNA_IN to LNA_OUT	Gp	15	16	19	dB
Noise figure	RX, PSSO20 N20	NF NF		2.5 2.1	2.8 2.3	dB
Gain compression	RX, referred to Pin LNA_OUT	O1dB	-9	-7	-6	dBm
3 rd -order input interception point	RX	IIP3	-16	-14	-13	dBm
Input matching ⁽⁴⁾	RX, Pin LNA_IN	VSWRin			2:1	
Output matching ⁽⁴⁾	RX Pin LNA_OUT	VSWRout			2:1	
Logic input levels (RX_ON, PU)						
High input level	= '1' Pins RX_ON and PU	V_{iH}	2.4		$V_{S, LNA}$	V
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1' $V_{iH} = 2.4\text{ V}$	I_{iH}		40	60	μA
Low input current	= '0'	I_{iL}			0.2	μA

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, $Z_C = 50\ \Omega$.
 2. With external matching network, load impedance $50\ \Omega$.
 3. Low-noise amplifier shall be unconditionally stable.
 4. With external matching components.

Control Logic for LNA and T/R Switch Driver

Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

Typical Operating Characteristics

Figure 5. LNA (PSSO20): Gain and Noise Figure versus Frequency

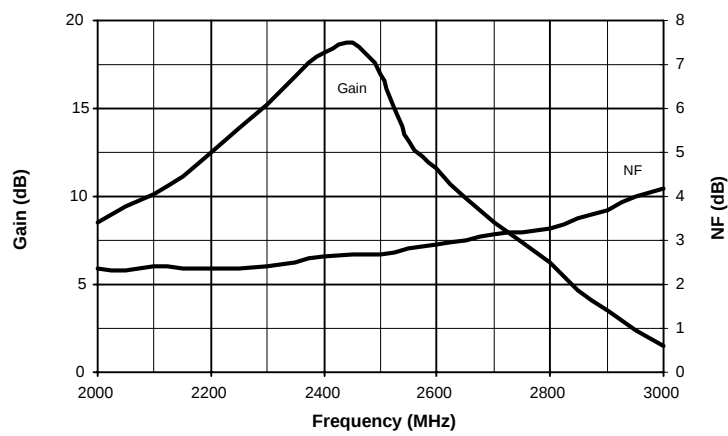


Figure 6. LNA (N20): Gain and Noise Figure versus Frequency

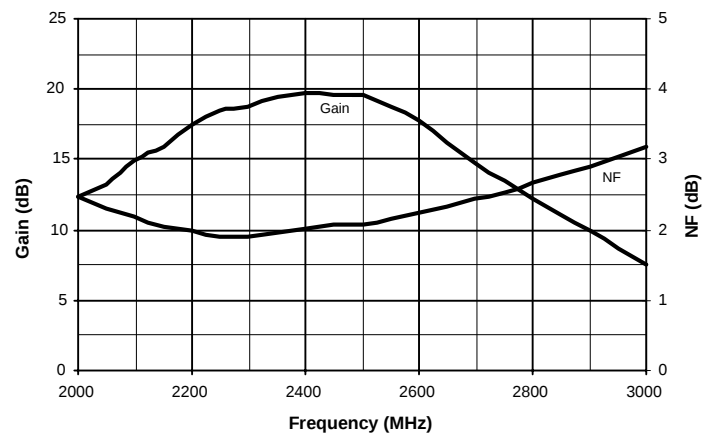


Figure 7. LNA: NF and Gain versus Temperature

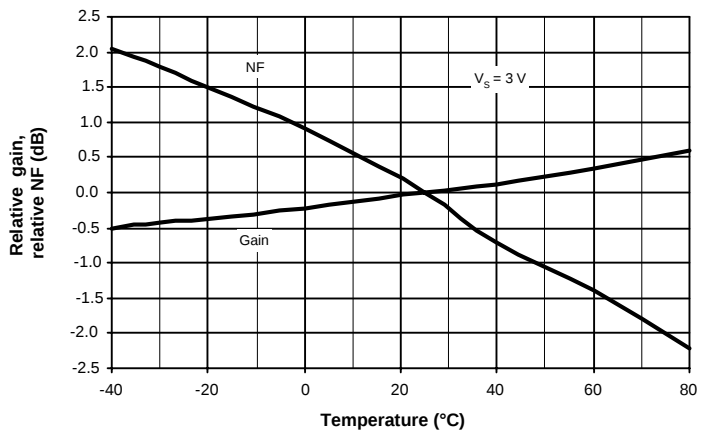


Figure 8. LNA: Typical Switch-out Current versus R_{switch}

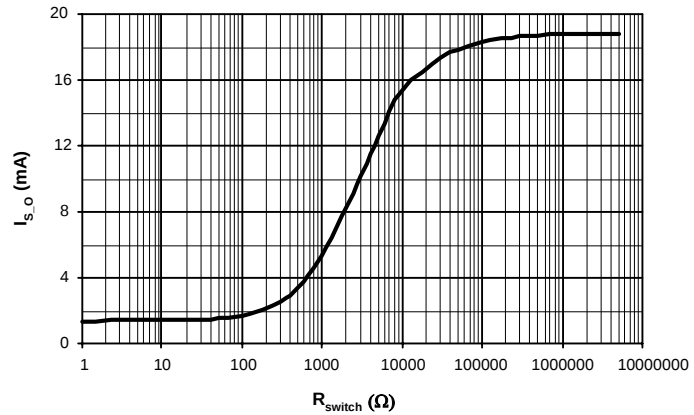


Figure 9. PA (PSSO20): Output Power and PAE versus Supply

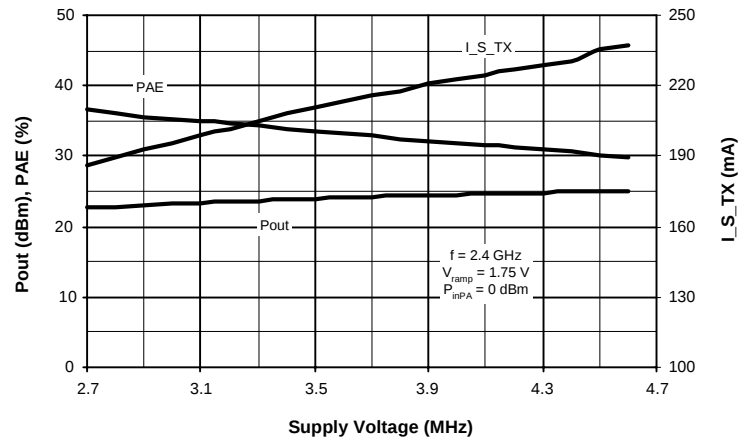


Figure 10. PA (PSSO20): Output Power and PAE versus Ramp Voltage

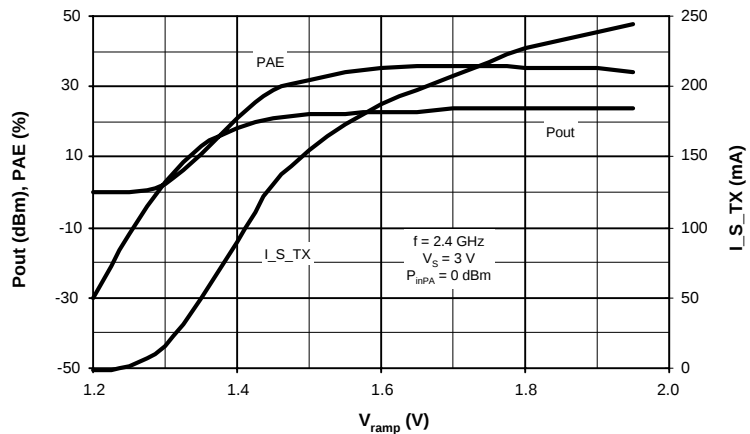


Figure 11. PA (PSSO20): Output Power and PAE versus Input Power

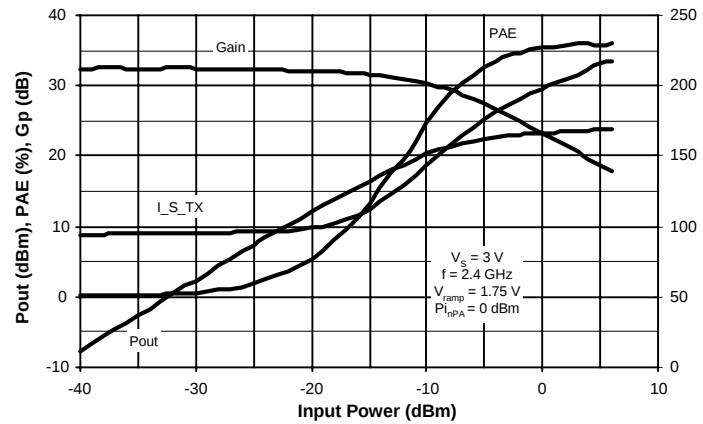


Figure 12. PA (PSSO20): Output Power and PAE versus Frequency

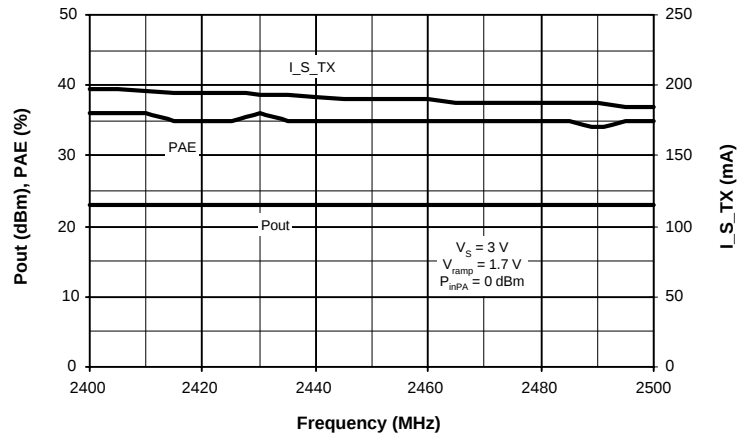


Figure 13. PA (N20): Output Power and PAE versus Supply Voltage

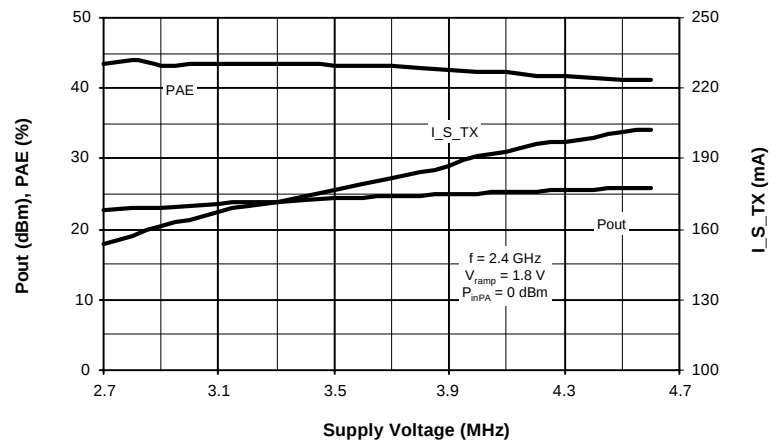


Figure 14. PA (N20) Output Power and PAE versus Ramp Voltage

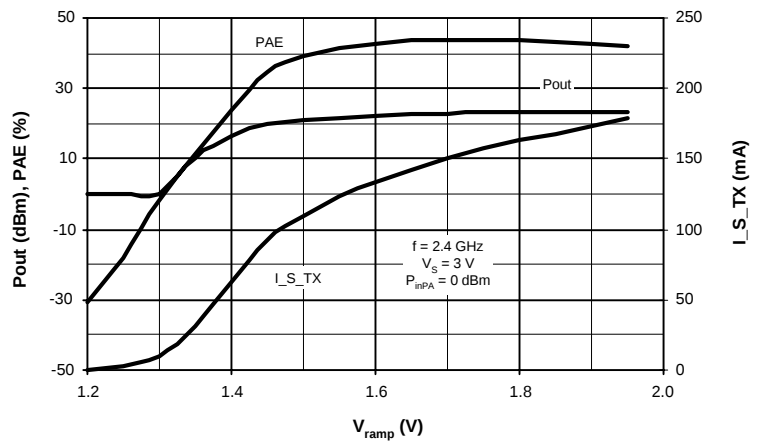


Figure 15. PA (N20): Output Power and PAE versus Input Power

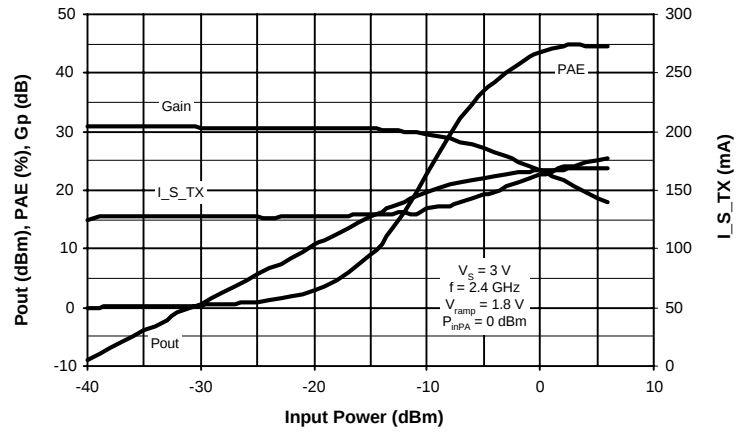


Figure 16. PA (N20): Output Power and PAE versus Frequency

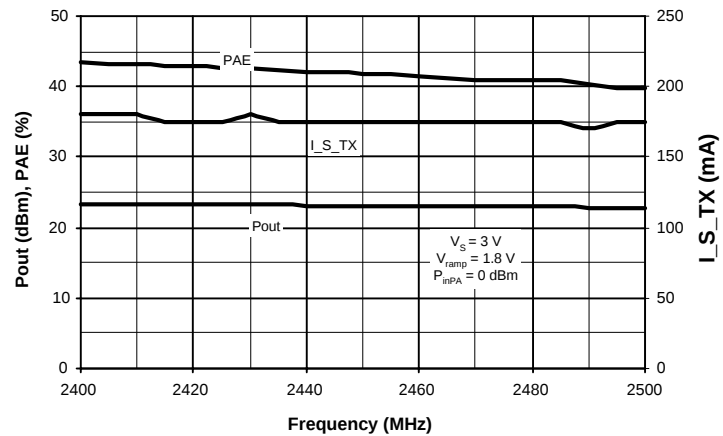
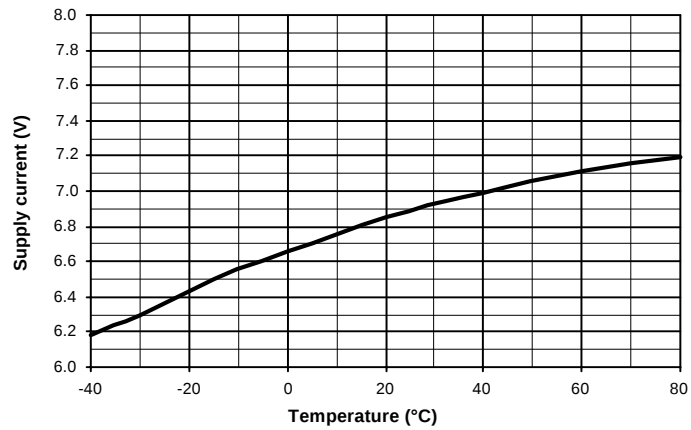
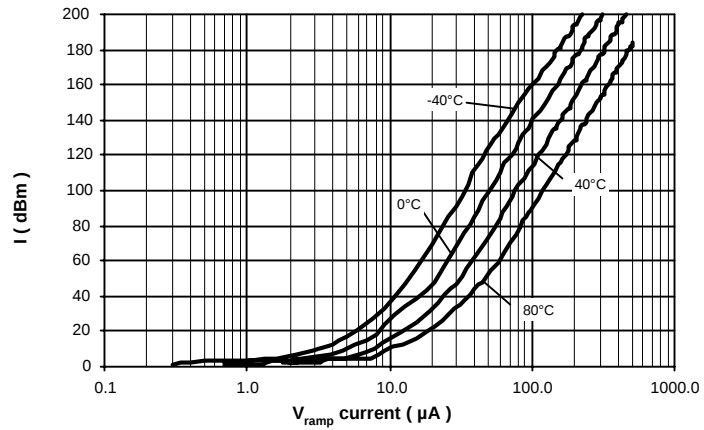
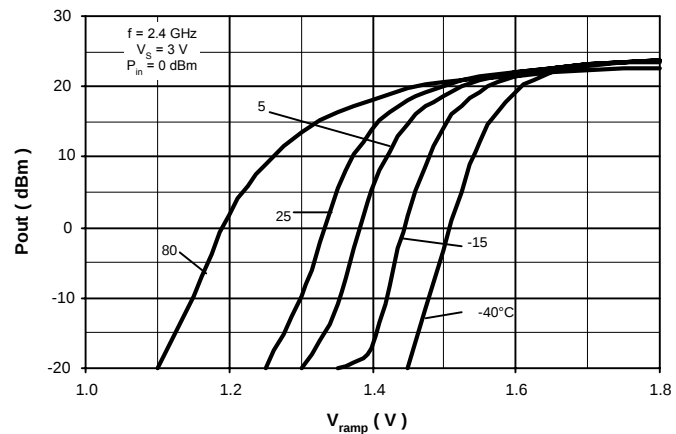


Figure 17. LNA: Supply Current versus Temperature

Figure 18. PA (PSSO20): Current versus V_{ramp} and TemperatureFigure 19. PA (PSSO20, N20): P_{out} versus V_{ramp} and Temperature

Input/Output Circuits

Figure 20. Input Circuit PA_IN/V1_PA

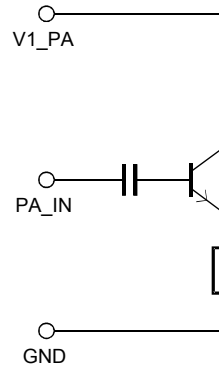


Figure 21. Input Circuit RAMP/V1_PA

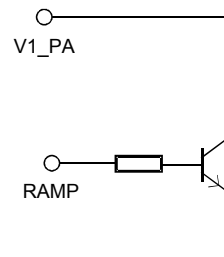


Figure 22. Input Circuit V2_PA

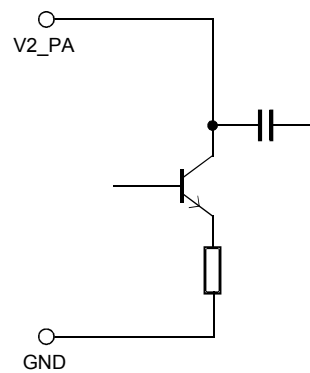


Figure 23. Input/Output Circuit V3_PA_OUT

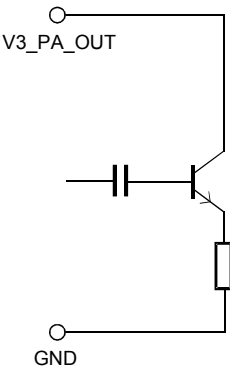


Figure 24. Input Circuit SWITCH_OUT/R_SWITCH

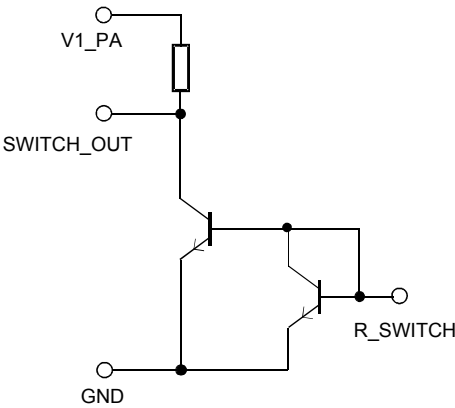


Figure 25. Input Circuit LNA_IN/VS_LNA

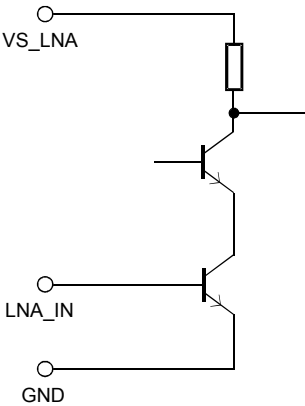


Figure 26. Input Circuit PU/RX_ON

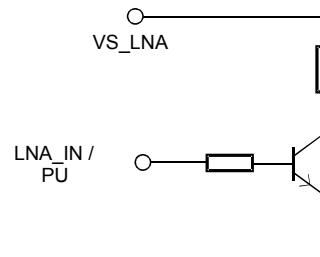
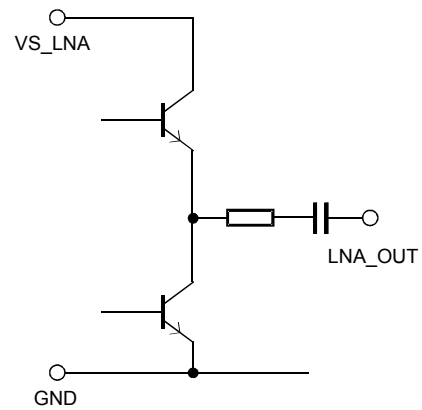


Figure 27. Output Circuit LNA_OUT



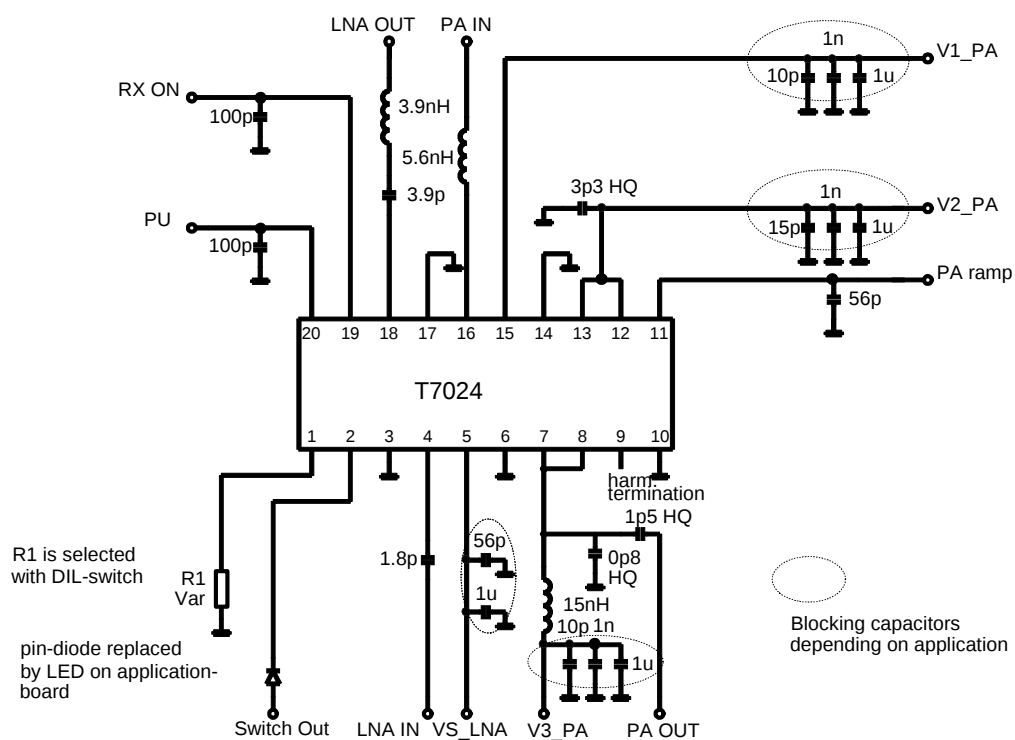
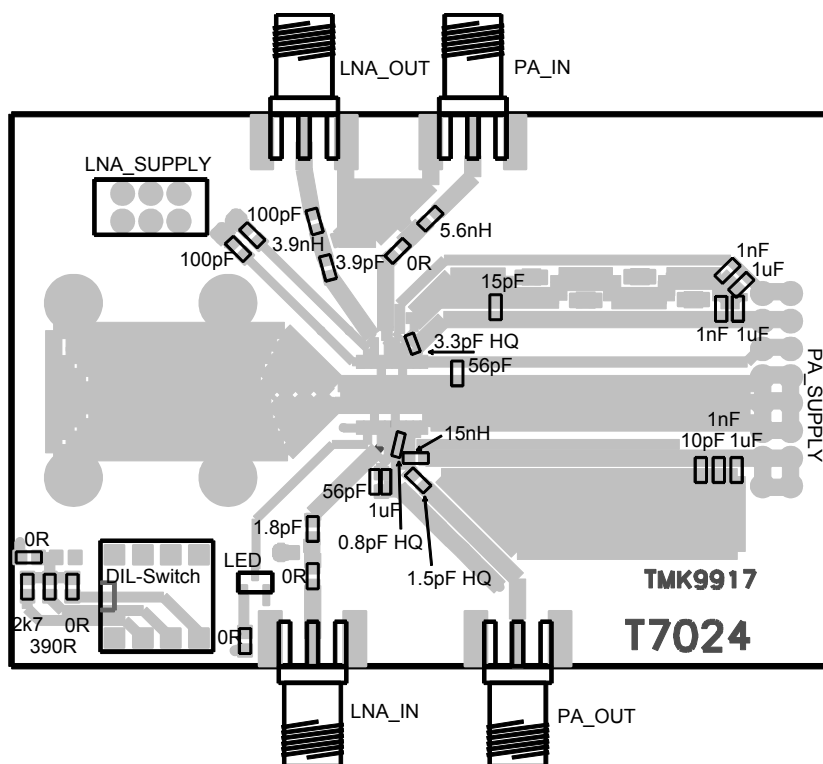


Figure 29. Layout for PSSO20



Gerberfiles are available on request.

The application board consists of 4 layers:

1. top layer: RF-signals, 35 μm Cu
2. spacing: 490 μm FR4
3. second layer: GND, 35 μm Cu
4. spacing: 550 μm FR4
5. third layer: GND (optional), 35 μm Cu
6. spacing: 490 μm FR4
7. bottom layer: DC connection, 35 μm Cu

Figure 30. Application Board N20

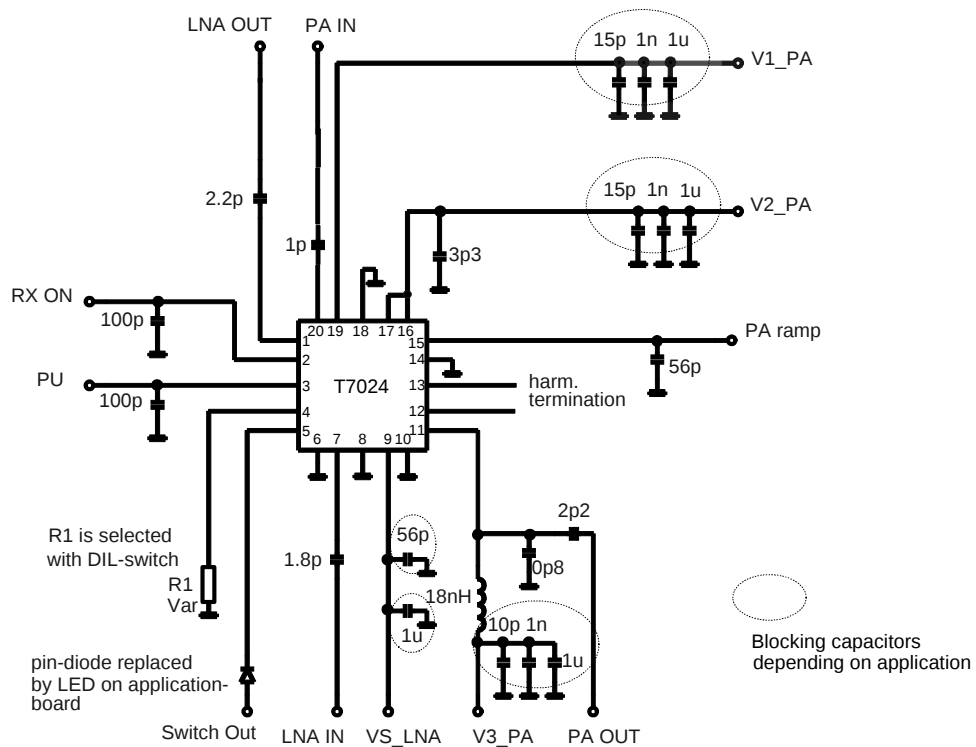
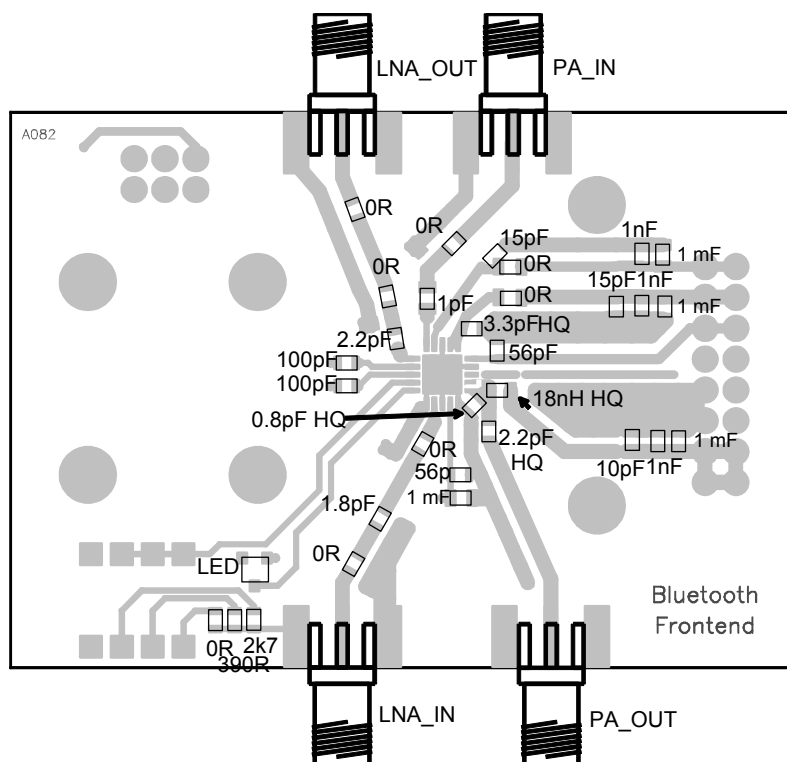


Figure 31. Layout for N20



Gerberfiles are available on request.

The application board consists of 4 layers:

1. top layer: RF-signals, 35 μm Cu
2. spacing: 490 μm FR4
3. second layer: GND, 35 μm Cu
4. spacing: 550 μm FR4
5. third layer: GND (optional), 35 μm Cu
6. spacing: 490 μm FR4
7. bottom layer: DC connection, 35 μm Cu

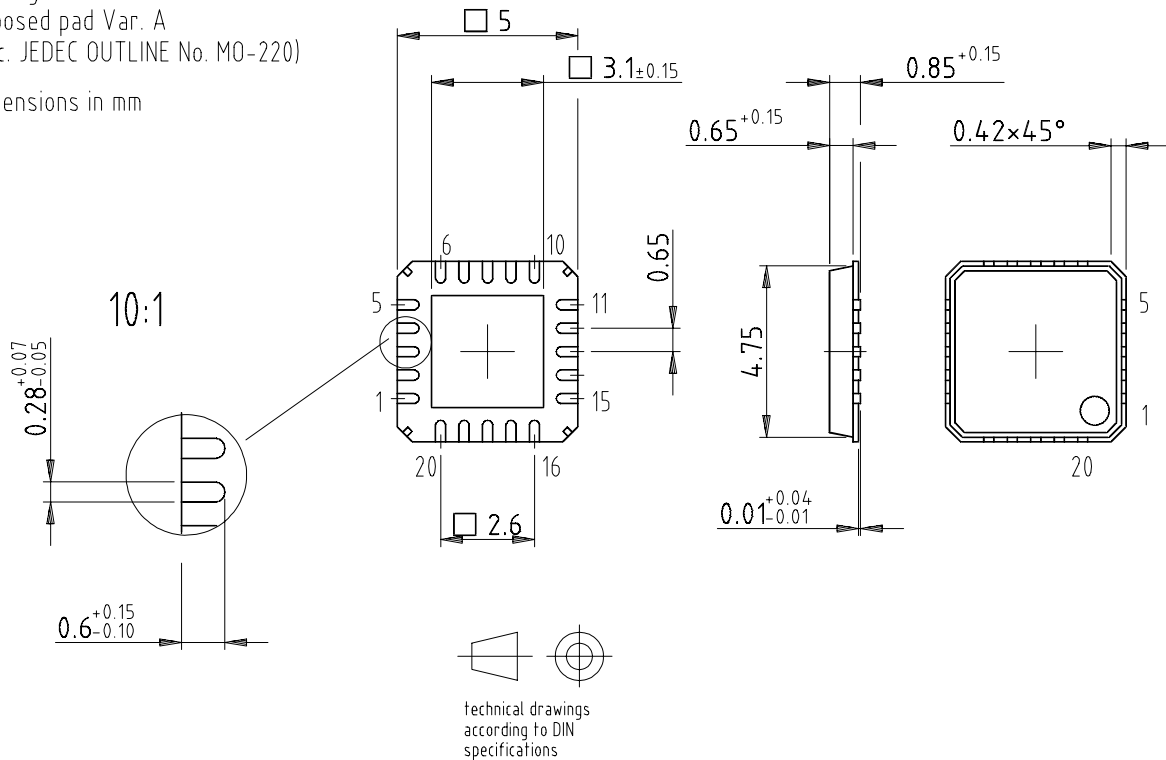
Ordering Information

Extended Type Number	Package	Remarks
T7024-TRS	PSSO20	Tube
T7024-TRQ	PSSO20	Taped and reeled
T7024-PGS	HP-VFQFP-N20	Tube
T7024-PGQ	HP-VFQFP-N20	Taped and reeled
T7024-DB	Flipchip	—

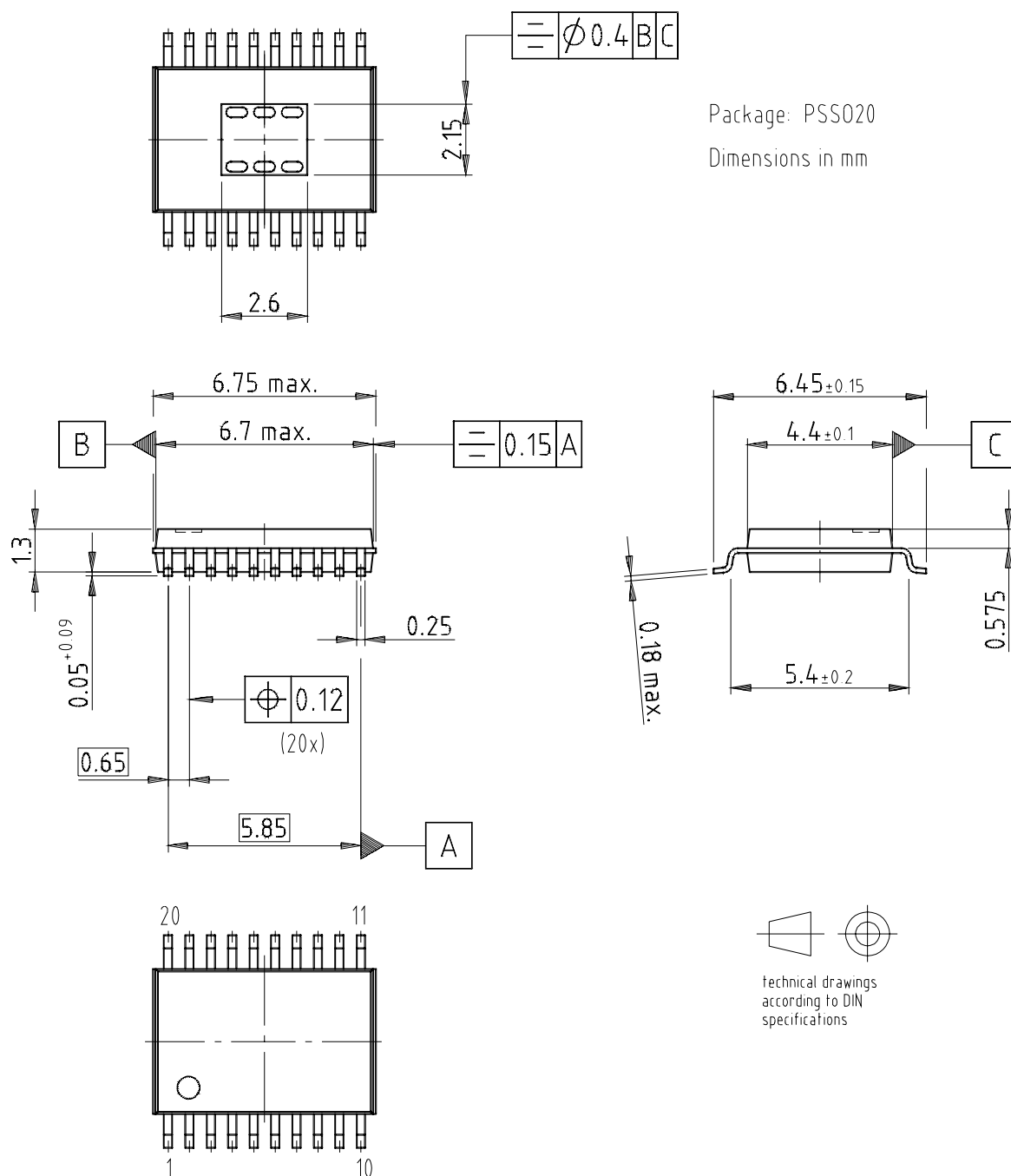
Package Information

Package: HP-VFQFP-N20
Exposed pad Var. A
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Drawing-No.: 6.543-5069.02-4
Issue: 1; 25.09.00



Drawing-No.: 6.543-5078.01-4
Issue: 1; 05.06.01



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