2.5V, 2GHz ANY DIFF. IN-TO-LVDS 1:4 FANOUT BUFFER/TRANSLATOR W/ INTERNAL TERMINATION

FEATURES

- Accepts any differential input signal and provides four LVDS outputs
- Guaranteed AC performance over temperature and voltage:
  - > 2.0GHz f_{MAX}
  - < 20ps within-device skew
  - < 200ps rise/fall times
- Low jitter design:
  - < 1ps (rms) cycle-to-cycle jitter
  - < 10ps (pk-pk) total jitter
- 2.5V voltage supply operation
- Unique input termination and V_T pin accepts DC–coupled and AC–coupled inputs (CML, PECL, LVDS, and HSTL)
- TTL/CMOS compatible enable input
- High-speed LVDS outputs
- Wide operating temperature range: –40°C to +85°C
- Available in 16-pin (3mm × 3mm) MLF™ package

APPLICATIONS

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

Precision Edge™

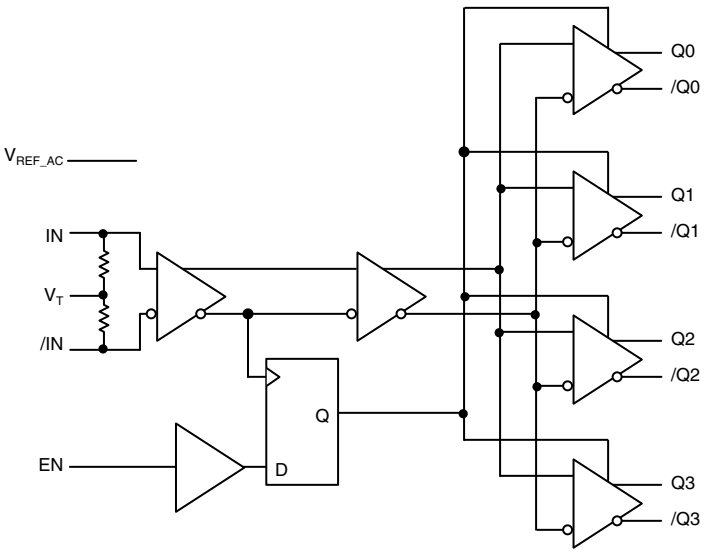
DESCRIPTION

The SY89832U is a 2.5V, high-speed, 2GHz differential LVDS (Low Voltage Differential Swing) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

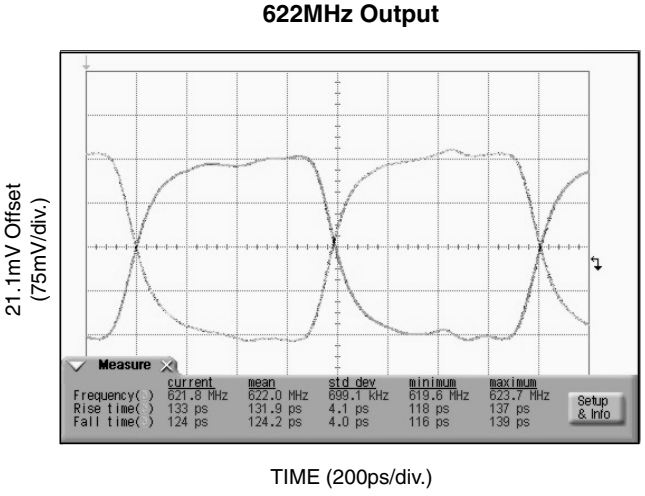
The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference output is included for AC-coupled applications.

The SY89832U is a part of Micrel's high-speed clock synchronization family. For 3.3V applications, see SY89833L. For applications that require a different I/O combination, consult Micrel's website at *www.micrel.com*, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE



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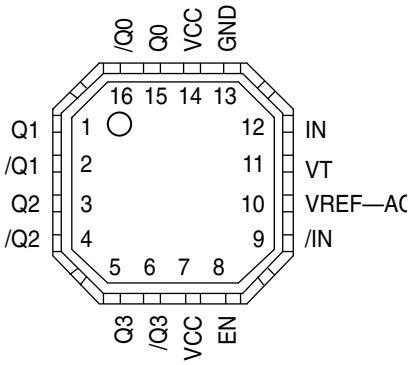
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

Rev.: C Amendment: /0
Issue Date: February 2003

PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89832UMI	MLF-16	Industrial	832U
SY89832UMITR*	MLF-16	Industrial	832U

*Tape and Reel

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2, 3, 4, 5, 6	(Q0, /Q0) to (Q3, /Q3)	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See "*LVDS Outputs"* section, Figure 2. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	TTL/CMOS Compatible Synchronous Enable: When EN goes LOW, Q outputs will go LOW and /Q outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{CC}/2V. A 25kΩ pull-up resistor is included. The default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal (IN, /IN).
9, 12	/IN, IN	Differential Clock Inputs: Internal 50Ω termination resistors to the V_T pin. See *"Input Interface Applications"* section.
10	VREF–AC	Reference Voltage equals V_{CC}–1.4V, and is used for AC-coupled applications. The maximum sink/source current is 0.5mA. See *"Input Interface Applications"* section. When using $V_{REF–AC}$, bypass with 0.01µF capacitor to V_{CC}.
11	VT	Termination Center-Tap. See *"Input Interface Applications"* section, and Figure 1a.
13, Exposed Pad	GND	Ground. Exposed pad internally connected to GND and must be connected to a ground plane for proper thermal operation.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0(1)	1(1)

Note 1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
Output Current (I_{OUT}) ..... ±10mA
Input Current (IN, /IN) ..... ±50mA
V_T Current (I_{VT}) ..... ±100mA
Input Sink/Source Current ($V_{REF–AC}$), **Note 3** ..... ±2mA
Lead Temperature (Soldering, 10sec.), ... 220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage Range ..... +2.375V to 2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
MLF™ (θ_{JA})
Still-Air ..... 60°C/W
500lfpm ..... 54°C/W
MLF™ (ψ_{JB}) , **Note 4** ..... 32°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No Load, Maximum Supply Voltage		75	100	mA
R_{IN}	Differential Input Resistance (IN, /IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	**Note 3**	0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage (IN, /IN)	**Note 3**	–0.3		V_{CC}+0.2	V
V_{IN}	Input Voltage Swing	**Note 3,** see Figure 2c, and 2d V_{IN} (max.), f_T = floating.	0.1		3.6	V
V_{DIFF_IN}	Differential Input Voltage Swing	**Note 3,** see Figure 2c, and 2d	0.2			V
$\|I_{IN}\|$	Input Current (IN, /IN)	**Note 3**			45	mA
V_{REF_AC}	Reference Voltage	**Note 3**	V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with airflow greater than 500lfpm.

Note 2. Specification for packaged product only.

Note 3. Due to the internal termination (see *"Differential Input"*) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	see Figures 2c, and 2d.	250	350	400	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	see Figures 2c, and 2d.	500	700	800	mV
V_{OH}	Output HIGH Voltage	see Figures 2a–2b.			1.475	V
V_{OL}	Output LOW Voltage	see Figures 2a–2b.	0.925			V
V_{OCM}	Output Common Mode Voltage	see Figures 2a–2b.	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage	see Figures 2a–2b.	–50		50	mV

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current				–300	µA

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS[Notes 1, 2]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	≥200mVpp Output Swing	2.0			GHz
t_{PLH} t_{PHL}	Differential Propagation Delay (IN-to-Q)	Input Swing: <400mV	370	470	570	ps
		Input Swing: ≥400mV	300	410	500	ps
t_{SKEW}	Within-Device Skew (Differential)	**Note 3**		5	20	ps
	Part-to-Part Skew (Differential)				200	ps
t_S	Set-Up Time (EN to IN, /IN)	**Note 4 and Note 5**	300			ps
t_H	Hold Time (EN to IN, /IN)	**Note 4 and Note 5**	500			ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	**Note 6**			1	ps(rms)
	Total Jitter	**Note 7**			10	ps(pk-pk)
t_r, t_f	Output Rise/Fall Times (20% to 80%)		70	120	200	ps

Note 1. Measured with a 400mV input signal, 50% duty cycle. All outputs are loaded with 100Ω between Q and /Q. 50Ω to V_{CC}–2V. Output swing is ≥ 200mV.

Note 2. Specification for packaged product only.

Note 3. Skew is measured between outputs under identical transitions.

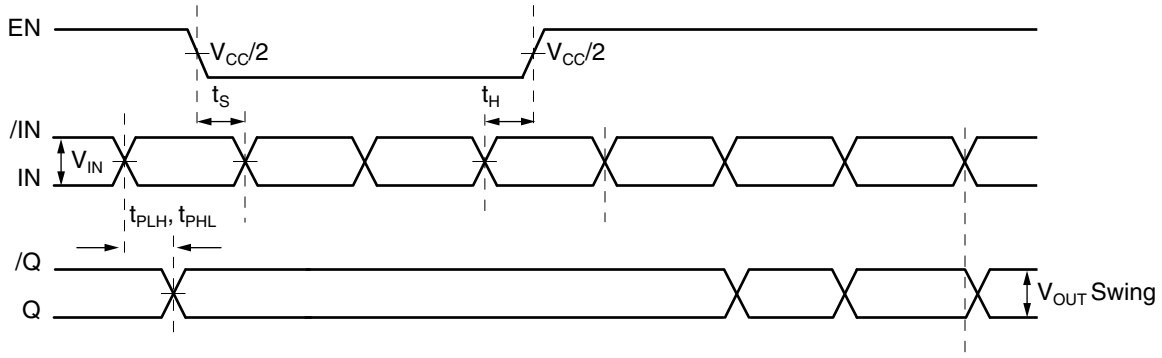
Note 4. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications set-up and hold times do not apply.

Note 5. See *"Timing Diagram."*

Note 6. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.

Note 7. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

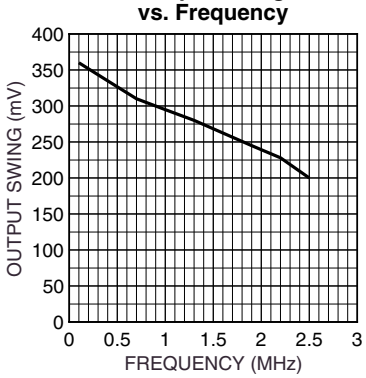
TIMING DIAGRAM



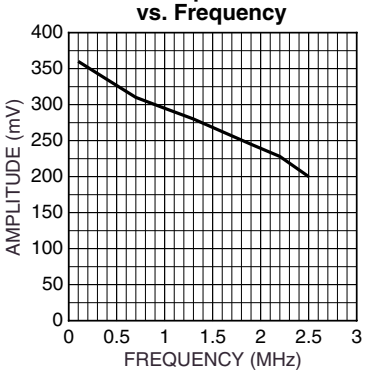
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V, T_A = 25°C, V_{IN} = 400mV, unless otherwise stated.

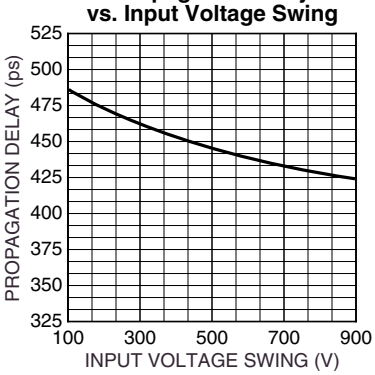
Output Swing vs. Frequency



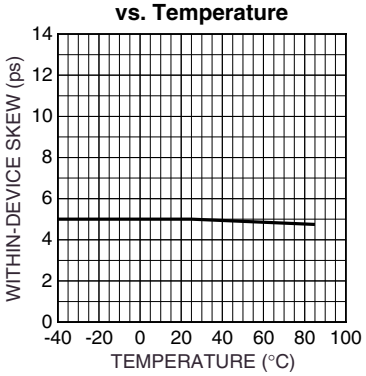
Amplitude vs. Frequency



Propagation Delay vs. Input Voltage Swing



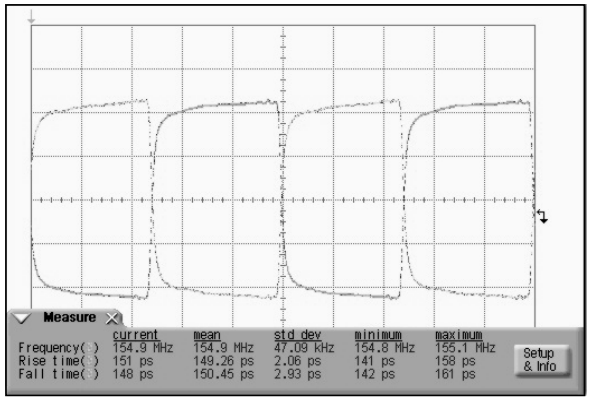
Within-Device Skew vs. Temperature



FUNCTIONAL CHARACTERISTICS

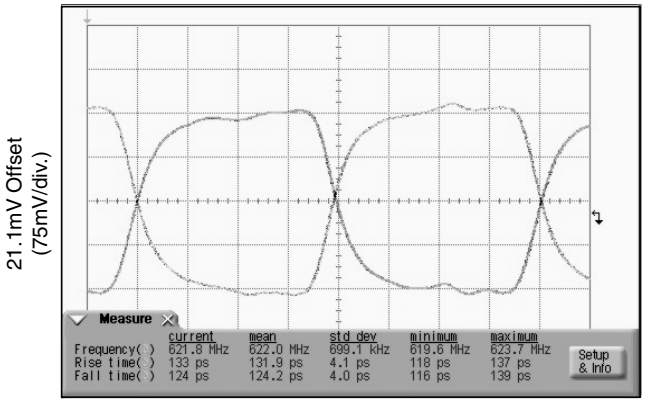
V_{CC} = 2.5V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.

155MHz Output



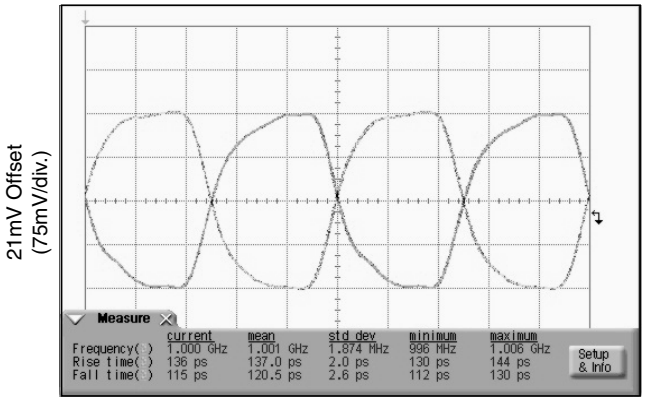
TIME (1.291ns/div.)

622MHz Output



TIME (200ps/div.)

1GHz Output



TIME (200ps/div.)

INPUT STAGE

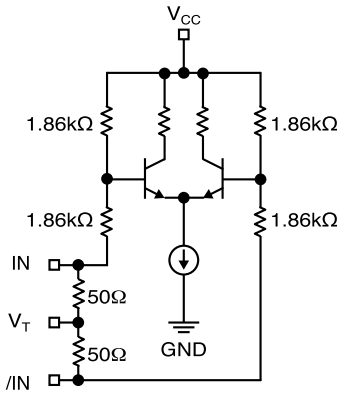


Figure 1a. Simplified Differential Input Buffer

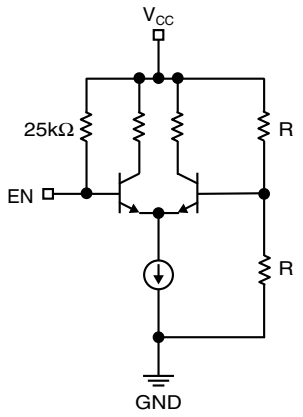


Figure 1b. Simplified TTL/CMOS Input Buffer

LVDS OUTPUTS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receive

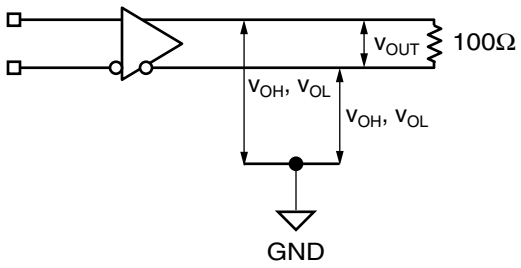


Figure 2a. LVDS Differential Measurement

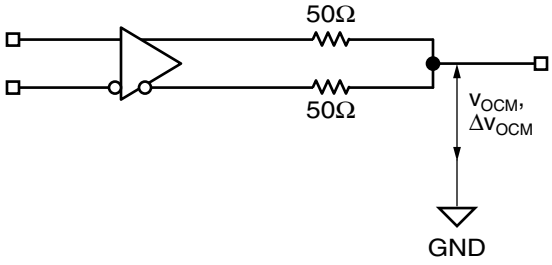


Figure 2b. LVDS Common Mode Measurement

DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

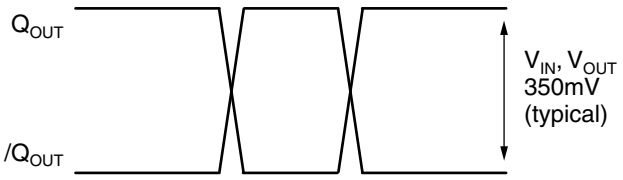


Figure 2c. Single-Ended Swing

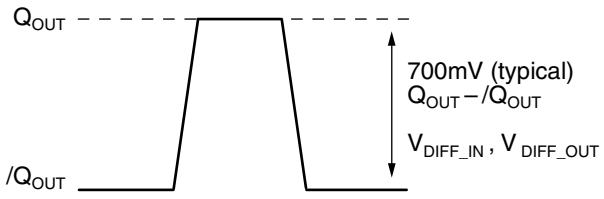


Figure 2d. Differential Swing (Q_{OUT}–$/Q_{OUT}$)

INPUT INTERFACE APPLICATIONS

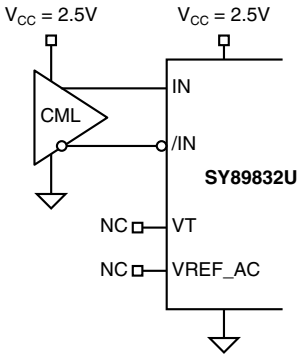


Figure 3a. DC-Coupled CML Input Interface

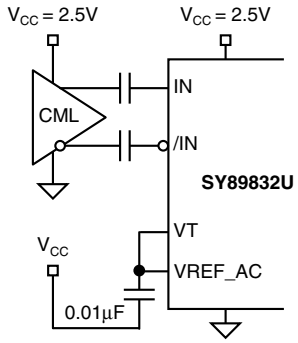


Figure 3b. AC-Coupled CML Input Interface

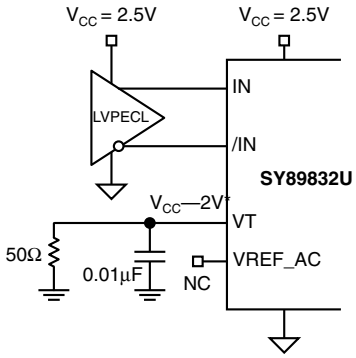


Figure 3c. DC-Coupled PECL Input Interface
(*Bypass with 0.01µF to GND)

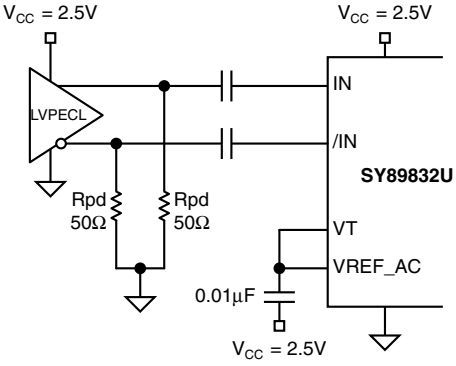


Figure 3d. AC-Coupled PECL Input Interface

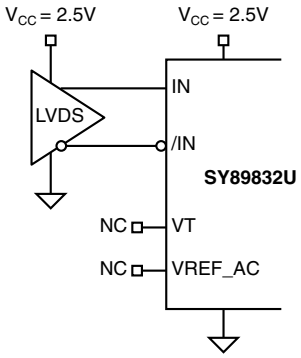


Figure 3e. LVDS Input Interface

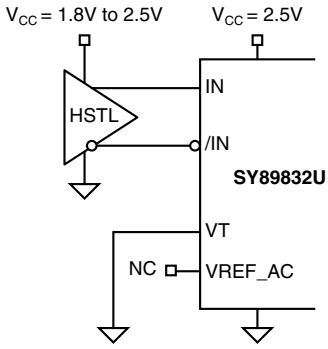
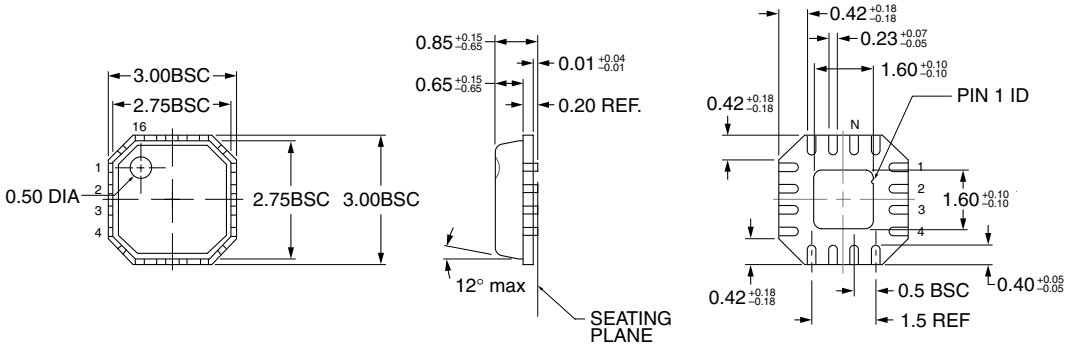


Figure 3f. HSTL Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTATION

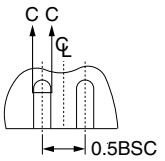
Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input Mux	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/ Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89833L	2GHz ANY DIFFERENTIAL INPUT-to-LVDS Out 1:4 Fanout Buffer Translator w/Internal Termination	http://www.micrel.com/product-info/products/sy89833l.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	http://www.amkor.com/products/notes_papers/MLF_appnote_0301.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/as/solutions.shtml

16 LEAD EPAD *Micro*LeadFrame™ (MLF-16)

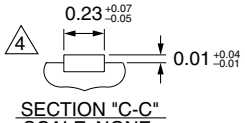


TOP VIEW

BOTTOM VIEW



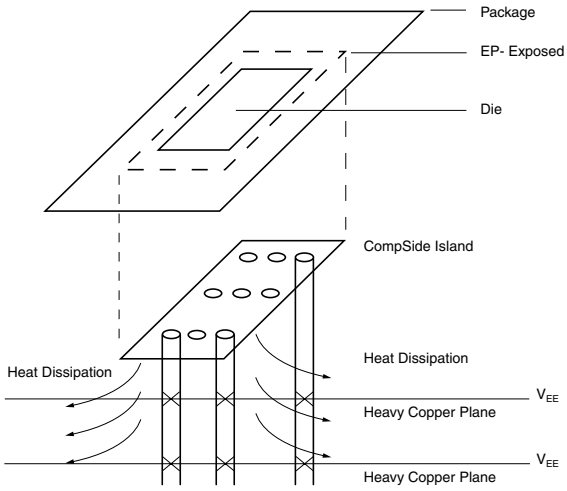
FOR EVEN TERMINAL/SIDE



SECTION "C-C"
SCALE: NONE

1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
Note 2. Exposed pads must be soldered to a ground for proper thermal management.

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