2GHz ANY DIFF. IN-TO-LVPECL ULTRA LOW-JITTER AND SKEW 1:4 FANOUT BUFFER/TRANSLATOR W/ INTERNAL TERMINATION

FEATURES

- Guaranteed AC performance over temperature and voltage
  - > 2.0GHz f_{MAX}
  - < 20ps within-device skew
  - < 225ps rise/fall times
- Low jitter design
  - < 1ps(rms) cycle-to-cycle
  - < 10ps(pk-pk) total jitter
- Unique input termination and V_T pin for DC-coupled and AC-coupled inputs (CML, HSTL, and LVPECL)
- Fully differential I/O design
- Low power 2.5V and 3.3V power supply
- TTL/CMOS compatible enable input
- Wide operating temperature range: –40°C to +85°C
- Available in 16-pin (3mm × 3mm) MLF™ package

APPLICATIONS

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

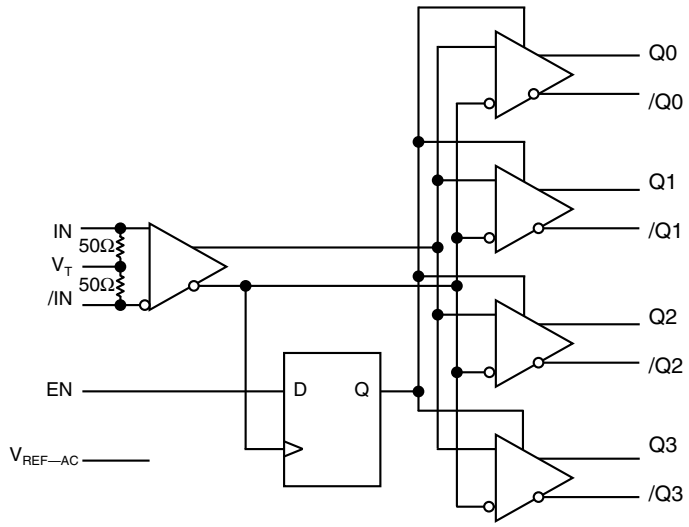
Precision Edge™

DESCRIPTION

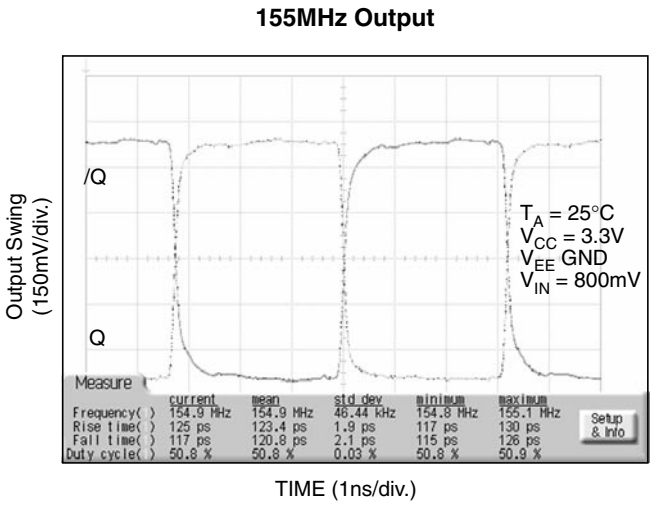
The SY89831U is a high-speed, 2GHz differential LVPECL 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps (5ps typ.) over supply voltage and temperature. The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference output is included for AC-coupled applications.

The SY89831U is a part of Micrel's high-speed clock synchronization family. For applications that require a different I/O combination, consult Micrel's website at *www.micrel.com*, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE



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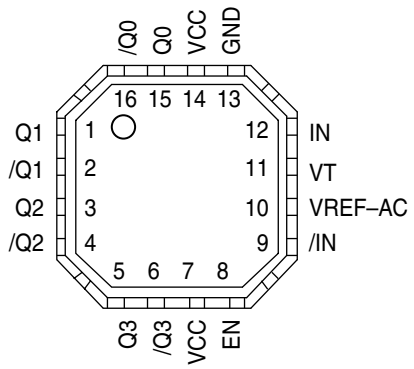
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

Rev.: C Amendment: /0
Issue Date: February 2003

PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89831UMI	MLF-16	Industrial	831U
SY89831UMITR*	MLF-16	Industrial	831U

*Tape and Reel

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2, 3, 4, 5, 6	(Q0, /Q0) to (Q3, /Q3)	LVPECL Differential (Outputs): Terminate to V_{CC}–2V. See *"Termination Recommendations"* section. Unused output pairs may be left floating with no impact on jitter.
8	EN	TTL/CMOS Compatible Synchronous Enable: When EN goes LOW, Q outputs will go LOW and /Q outputs will go HIGH on the next LOW transition at D inputs. Input threshold is V_{CC}/2V. Includes a 25kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal (IN, /IN).
9, 12	/IN, IN	Differential Clock (Inputs): Internal 50Ω termination resistors to V_T pin. See *"Input Interface Applications"* section.
10	VREF–AC	Reference Voltage: Equal to V_{CC}–1.4V (approx.), and used for AC–coupled applications. Maximum sink/source current is 0.5mA. See *"Input Interface Applications"* section. When using $V_{REF–AC}$, bypass with a 0.01µF capacitor to V_{CC}.
11	VT	Termination Center-Tap: For CML inputs, leave this pin floating. Otherwise, see Figures 2a to 2e in *"Input Interface Applications"* section.
13, Exposed Pad	GND	Ground. Exposed pad is internally connected to GND and must be connected to a ground plane for proper thermal operation.
14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0(1)	1(1)

Note 1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.5V
Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current (IN, /IN) ..... ±50mA
V_T Current (I_{VT}) ..... ±100µA
Input Sink/Source Current (V_{REF-AC}), **Note 3** ..... ±0.5mA
Lead Temperature (soldering, 10sec.) ..... 220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage Range ..... +2.375V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
  MLF™ (θ_{JA})
    Still-Air ..... 60°C/W
    500lfpm ..... 54°C/W
  MLF™ (Ψ_{JB}), **Note 4**
    Junction-to-Board ..... 32°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.375		3.63	V
I_{CC}	Power Supply Current	No load, maximum supply voltage		47	70	mA
R_{IN}	Differential Input Resistance (IN, /IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	**Note 3**	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	**Note 3**	0		V_{CC}–0.1	V
V_{IN}	Input Voltage Swing	**Note 3**, see Figure 1a, and 1b. V_T floating for V_{IN} (max.)	0.1		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing,	see Figure 1a, and 1b. **Note 3**	0.2			V
$\|I_{IN}\|$	Input Current (IN, /IN)	**Note 3**			35	mA

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product ony.

Note 3. Due to the internal termination (see *"Differential Input"*) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVTTL/LVCMOS INPUT DC ELECTRICAL CHARACTERISTICS(Note 1)

V_{CC} = 2.375V to 3.63V; V_{EE} = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		20		–125	µA
I_{IL}	Input LOW Current				–300	µA

Note 1. Specification for packaged product ony.

2.5V (100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 2.5V ±5%; V_{EE} = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CC}–2V	1355	1480	1605	mV
V_{OL}	Output LOW Voltage	R_L = 50Ω to V_{CC}–2V	555	680	805	mV
V_{OUT}	Output Voltage Swing	see Figure 1a, and 1b	550	800	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	see Figure 1a, and 1b	1100	1600	2100	mV

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Parameters are for V_{CC} = 2.5V. They vary 1:1 with V_{CC}.

Note 2. Specification for packaged product only.

3.3V (100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CC}–2V	2155	2280	2405	mV
V_{OL}	Output LOW Voltage	R_L = 50Ω to V_{CC}–2V	1355	1480	1605	mV
$V_{REF–AC}$	Reference Voltage, **Note 2**		1755	1875	1975	mV

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

Note 3. Single-ended input operation is limited to $V_{CC} \geq 3.0V$.

AC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 2.375 to 3.63V; V_{EE} = 0V; T_A = –40°C to +85°C, output loading is 50Ω to V_{CC}–2V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	Output Swing ≥ 450mV	2.0	2.5		GHz
t_{PLH} t_{PHL}	Propagation Delay-to-Output (Differential)	Input Swing: 100mV		390	0	ps
		Input Swing: 800mV	250	350	450	ps
t_{SKEW}	Within-Device Skew (Differential)	**Note 3**		5	20	ps
	Part-to-Part Skew (Differential)				150	ps
t_S	Set-Up Time (EN to IN, /IN)	**Note 4**	300			ps
t_H	Hold Time (EN to IN, /IN)	**Note 4**	300			ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	**Note 5**			1	ps(rms)
	Total Jitter	**Note 6**			10	ps(pk-pk)
t_r, t_f	Output Rise/Fall Times (20% to 80%)		70	150	225	ps

Note 1. Measured with 400mV input signal, 50% duty cycle, all loading with 50Ω to V_{CC}–2V. Output swing is ≥ 450mV.

Note 2. Specification for packaged product only.

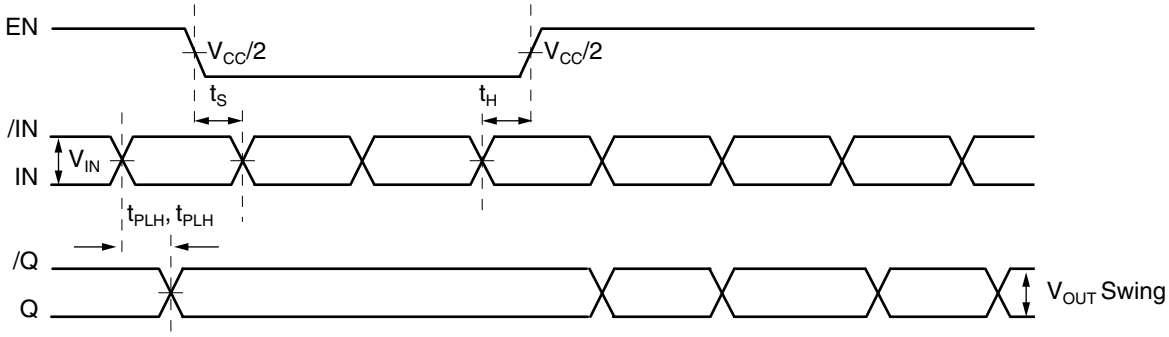
Note 3. Skew is measured between outputs under identical transitions.

Note 4. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

Note 5. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.

Note 6. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

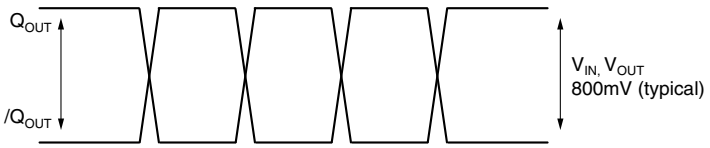


Figure 1a. Single-Ended Swing

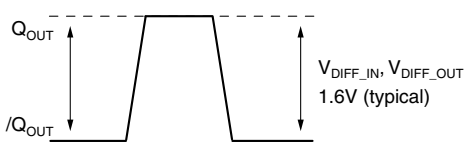
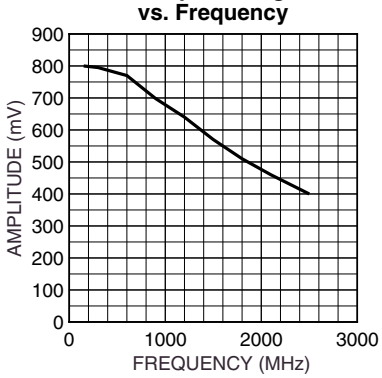


Figure 1b. Differential Swing

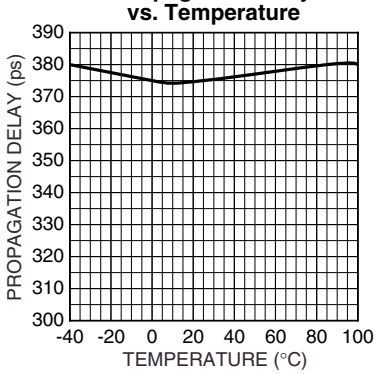
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = GND, T_A = 25°C, unless otherwise stated.

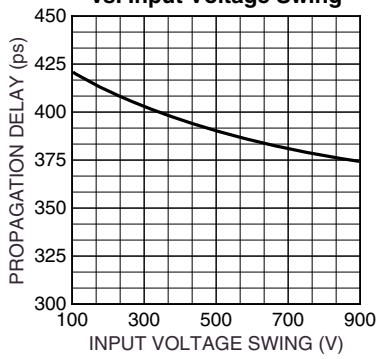
Output Swing vs. Frequency



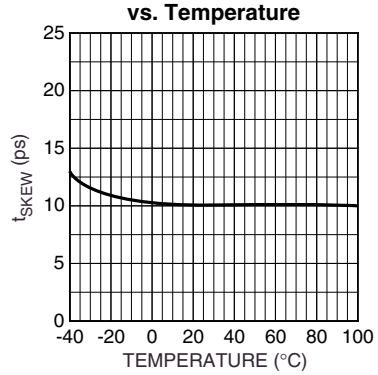
Propagation Delay vs. Temperature



Propagation Delay vs. Input Voltage Swing



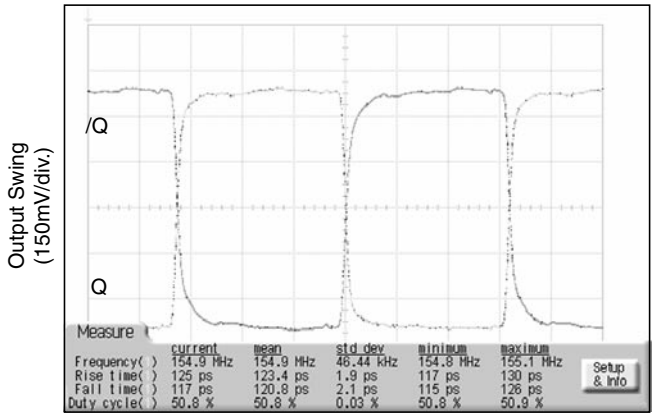
t_{SKEW} vs. Temperature



FUNCTIONAL CHARACTERISTICS

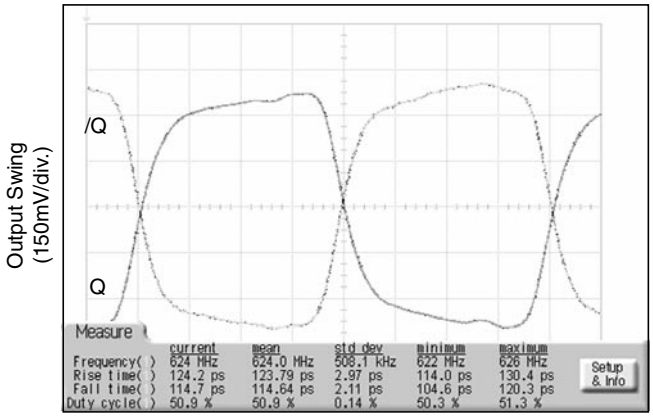
V_{CC} = 3.3V, V_{EE} = 0V, V_{IN} = 800mV, T_A = 25°C, unless otherwise stated.

155MHz Output



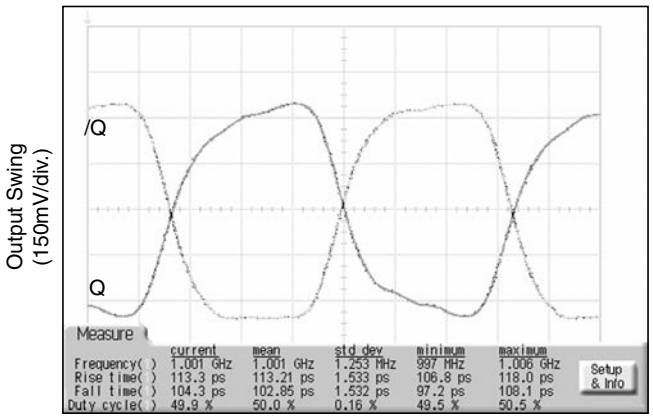
TIME (1ns/div.)

622MHz Output



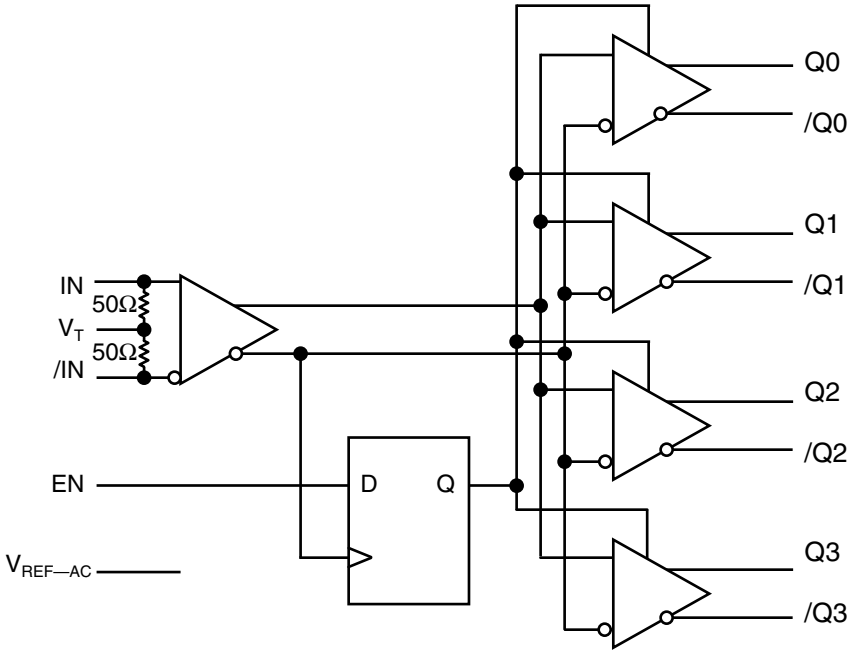
TIME (200ps/div.)

1GHz Output



TIME (150ps/div.)

FUNCTIONAL BLOCK DIAGRAM



DIFFERENTIAL INPUT

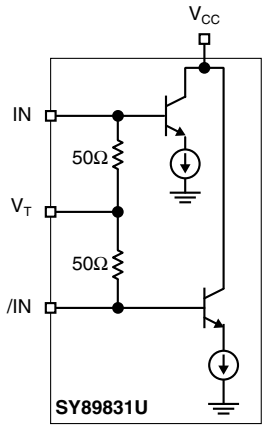


Figure 2. Input Stage

INPUT INTERFACE APPLICATIONS

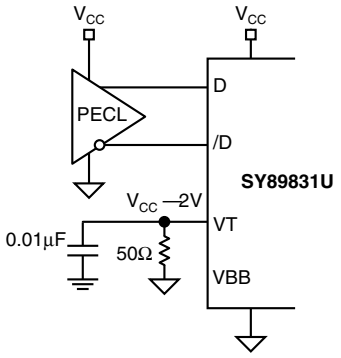


Figure 3a. DC-Coupled PECL Input Interface

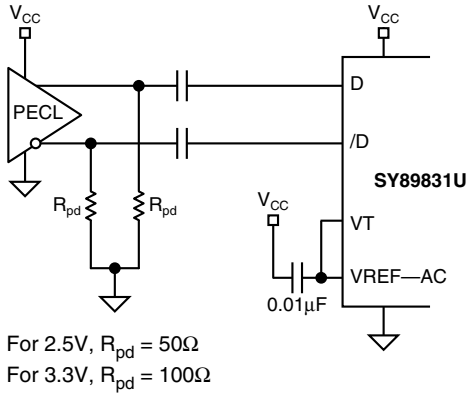


Figure 3b. AC-Coupled PECL Input Interface

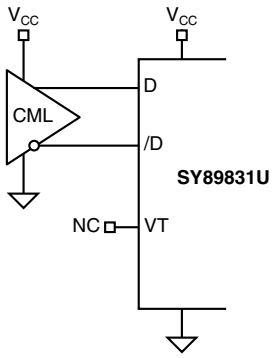


Figure 3c. DC-Coupled CML Input Interface

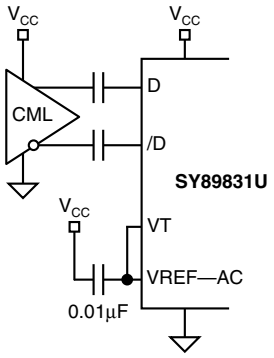


Figure 3d. AC-Coupled CML Input Interface

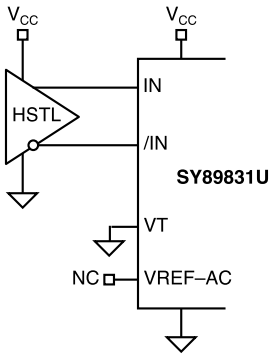


Figure 3e. HSTL Input Interface

OUTPUT TERMINATION RECOMMENDATIONS

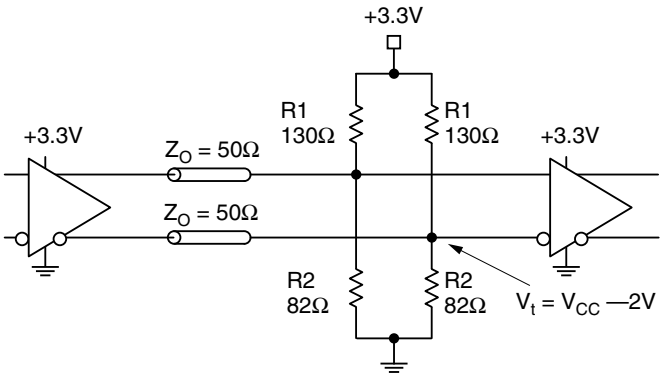


Figure 4. Parallel Termination—Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

Note 2. For +3.3V systems: R1 = 130Ω, R2 = 82Ω

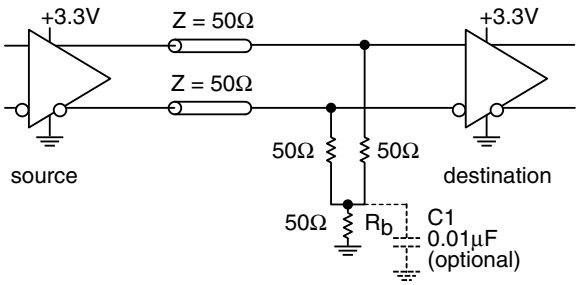


Figure 5. Three-Resistor "Y-Termination"

Note 1. Power-saving alternative to Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t.
For +2.5V systems R_b = 39Ω.
For +3.3V systems R_b = 46Ω to 50Ω.

Note 4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

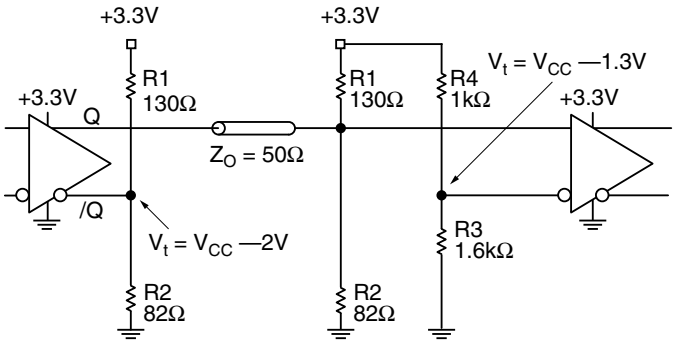


Figure 6. Terminating Unused I/O

Note 1. Unused output (/Q) must be terminated to balance the output.

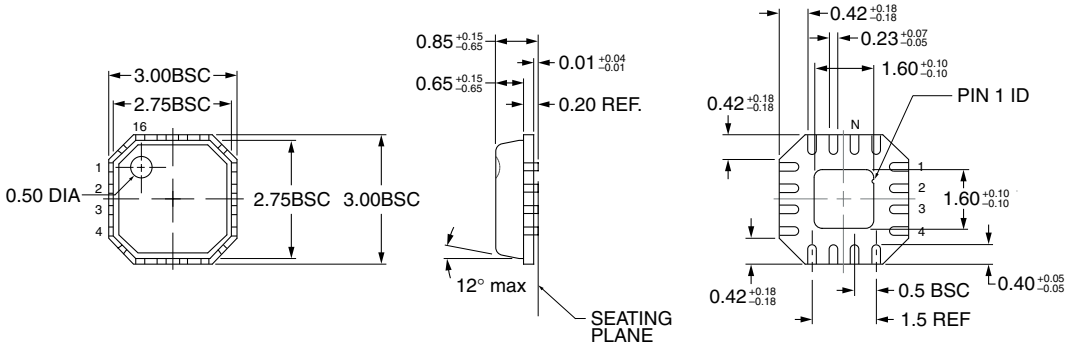
Note 2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.
For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1.6kΩ, R4 = 1k.

Note 3. Unused output pairs (Q and /Q) may be left floating.

RELATED PRODUCT AND SUPPORT DOCUMENTATION

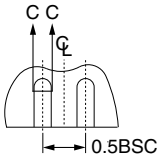
Part Number	Function	Data Sheet Link
SY89830U	1:4 LVPECL Fanout Buffer w/2:1 Mux Input	www.micrel.com/product-info/products/sy89830u.shtml
SY89832U	2GHz Ultra Low-Jitter and Skew 1:4 LVPECL Fanout Buffer/Translator w/Internal Termination	www.micrel.com/product-info/products/sy89832u.shtml
SY89833U	2GHz Any Diff. In-to-LVDS Out 1:4 Fanout Buffer/Translator w/Internal Termination	www.micrel.com/product-info/products/sy89833u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0301.pdf

16 LEAD EPAD *Micro*LeadFrame™ (MLF-16)

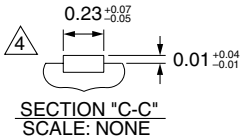


TOP VIEW

BOTTOM VIEW

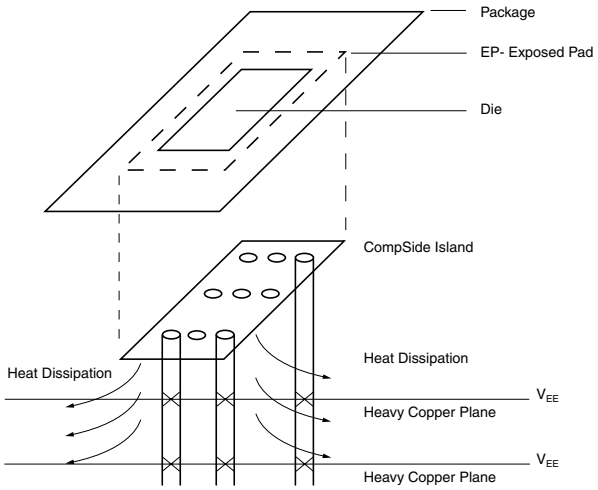


FOR EVEN TERMINAL/SIDE



1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
Note 2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

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