3.3V 1:22 HIGH-PERFORMANCE, LOW VOLTAGE BUS CLOCK DRIVER

FEATURES

- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- 22 differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω to ground with no offset voltage
- Low part-to-part skew (200ps max.)
- Low pin-to-pin skew (50ps max.)
- Available in a 64-Pin EPAD-TQFP

APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

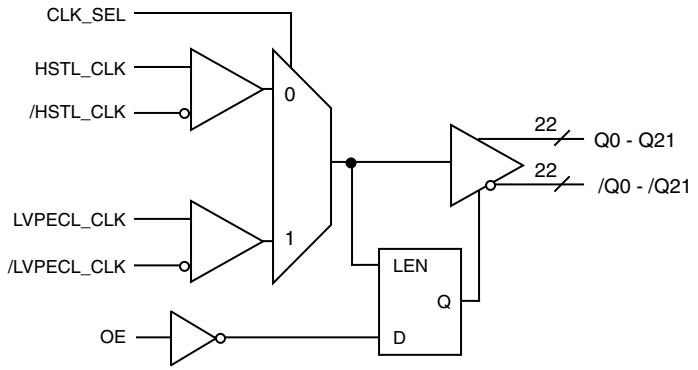
Precision Edge™

DESCRIPTION

The SY89824L is a High Performance Bus Clock Driver with 22 differential HSTL (High Speed Transceiver Logic) output pairs. The part is designed for use in low voltage (3.3V/1.8V) applications which require a large number of outputs to drive precisely aligned, ultra low skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low Voltage Positive Emitter Coupled Logic) by the CLK_SEL pin. The Output Enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89824L features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89824L is available in a single space saving package, enabling a lower overall cost solution.

LOGIC SYMBOL



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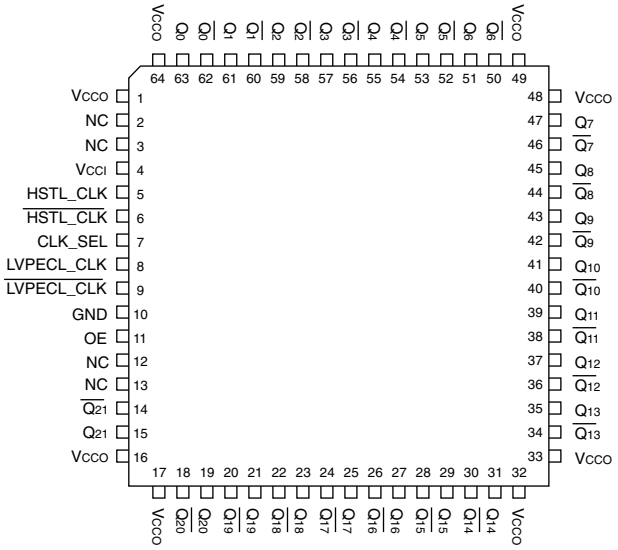
Rev.: E Amendment: /1
Issue Date: December 2002

PIN CONFIGURATION



64-Pin EPAD-TQFP

PIN NAMES

Pin	Function
HSTL_CLK, /HSTL_CLK	Differential HSTL Inputs
LVPECL_CLK, /LVPECL_CLK	Differential LVPECL Inputs
CLK_SEL	Input CLK Select (LVTTL)
OE	Output Enable (LVTTL)
Q_0-Q_{21}, /Q_0-/Q_{21}	Differential HSTL Outputs
GND	Ground
V_{CCI}	V_{CC} Core
V_{CCO}	V_{CC} Output

TRUTH TABLE

OE[1]	CLK_SEL	Q_0-Q_{21}	/Q_0-/Q_{21}
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

NOTE:

1. The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

SIGNAL GROUPS

Level	Direction	Signal
HSTL	Input	HSTL_CLK, /HSTL_CLK
HSTL	Output	Q_0-Q_{21}, /Q_0-/Q_{21}
LVPECL	Input	LVPECL_CLK, /LVPECL_CLK
LVCMOS/LVTTL	Input	CLK_SEL, OE

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CCI}, V_{CCO}	V_{CC} Pin Potential to Ground Pin	–0.5 to +4.0	V
V_{IN}	Input Voltage	–0.5 to V_{CCI}	V
I_{OUT}	DC Output Current (Output HIGH)	–50	mA
T_{store}	Storage Temperature	–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient) With Die attach soldered to GND: –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	 23 18 15	 °C/W °C/W °C/W
	With Die attach NOT soldered to GND: –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	44 36 30	°C/W °C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	4.3	°C/W

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCI}	V_{CC} Core	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}	V_{CC} Output	1.6	1.8	2.0	1.6	1.8	2.0	1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core	—	115	140	—	115	140	—	115	140	mA

HSTL

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage[1]	1.0	—	1.2	1.0	—	1.2	1.0	—	1.2	V
V_{OL}	Output LOW Voltage[1]	0.2	—	0.4	0.2	—	0.4	0.2	—	0.4	V
V_{IH}	Input HIGH Voltage	V_X +0.1	—	1.6	V_X +0.1	—	1.6	V_X +0.1	—	1.6	V
V_{IL}	Input LOW Voltage	–0.3	—	V_X –0.1	–0.3	—	V_X –0.1	–0.3	—	V_X –0.1	V
V_X	Input Crossover Voltage	0.68	—	0.9	0.68	—	0.9	0.68	—	0.9	V
I_{IH}	Input HIGH Current	+20	—	–350	+20	—	–350	+20	—	–350	µA
I_{IL}	Input LOW Current	—	—	–500	—	—	–500	—	—	–500	µA

NOTE:

1. Outputs loaded with 50Ω to ground.

LVPECL

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	Input HIGH Voltage	V_{CCI} – 1.165	V_{CCI} – 0.880	V_{CCI} – 1.165	V_{CCI} – 0.880	V_{CCI} – 1.165	V_{CCI} – 0.880	V
V_{IL}	Input LOW Voltage	V_{CCI} – 1.810	V_{CCI} – 1.475	V_{CCI} – 1.810	V_{CCI} – 1.475	V_{CCI} – 1.810	V_{CCI} – 1.475	V
I_{IH}	Input HIGH Current	—	+150	—	+150	—	+150	µA
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA

LVCMOS/LVTTL

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current	+20	—	–250	+20	—	–250	+20	—	–250	µA
I_{IL}	Input LOW Current	—	—	–600	—	—	–600	—	—	–600	µA

AC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay[2]	—	1.0	—	—	1.0	—	—	1.0	—	ns
t_{SKEW}	Within-Device Skew[3]	—	—	50	—	—	50	—	—	50	ps
t_{SKPP}	Part-to-Part Skew[4]	—	—	200	—	—	200	—	—	200	ps
V_{PP}	Minimum Input Swing[5] LVPECL_CLK	600	—	—	600	—	—	600	—	—	mV
V_{CMR}	Common Mode Range[6] LVPECL_CLK	–1.5	—	–0.4	–1.5	—	–0.4	–1.5	—	–0.4	V
t_S	OE Set-Up Time[7]	1.0	—	—	1.0	—	—	1.0	—	—	ns
t_H	OE Hold Time	0.5	—	—	0.5	—	—	0.5	—	—	ns
t_r tf	Output Rise/Fall Time (20% – 80%)	300	—	700	300	—	700	300	—	700	ps

NOTES:

1. Outputs loaded with 50Ω to ground. Airflow ≥ 300lfpm.
2. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
4. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
5. The V_{PP}(min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min.). The lower end of the CMR range varies 1:1 with V_{CCI}. The V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.
7. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89824LHC	H64-1	Extended Commercial

WAVEFORMS

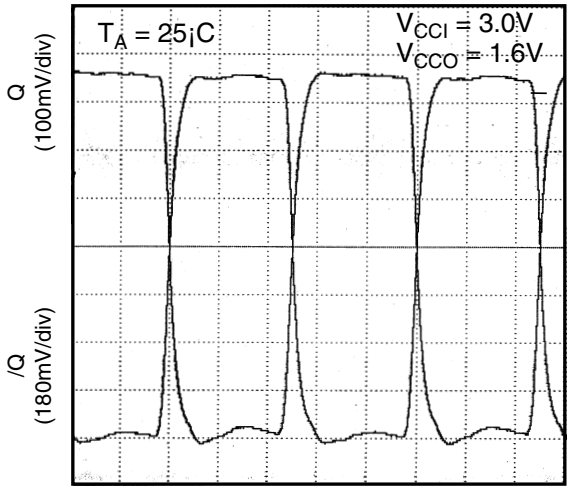


Figure 1. 100MHz Output Waveform

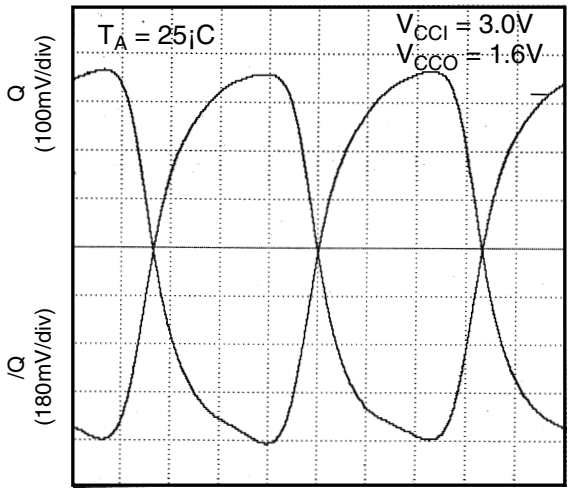
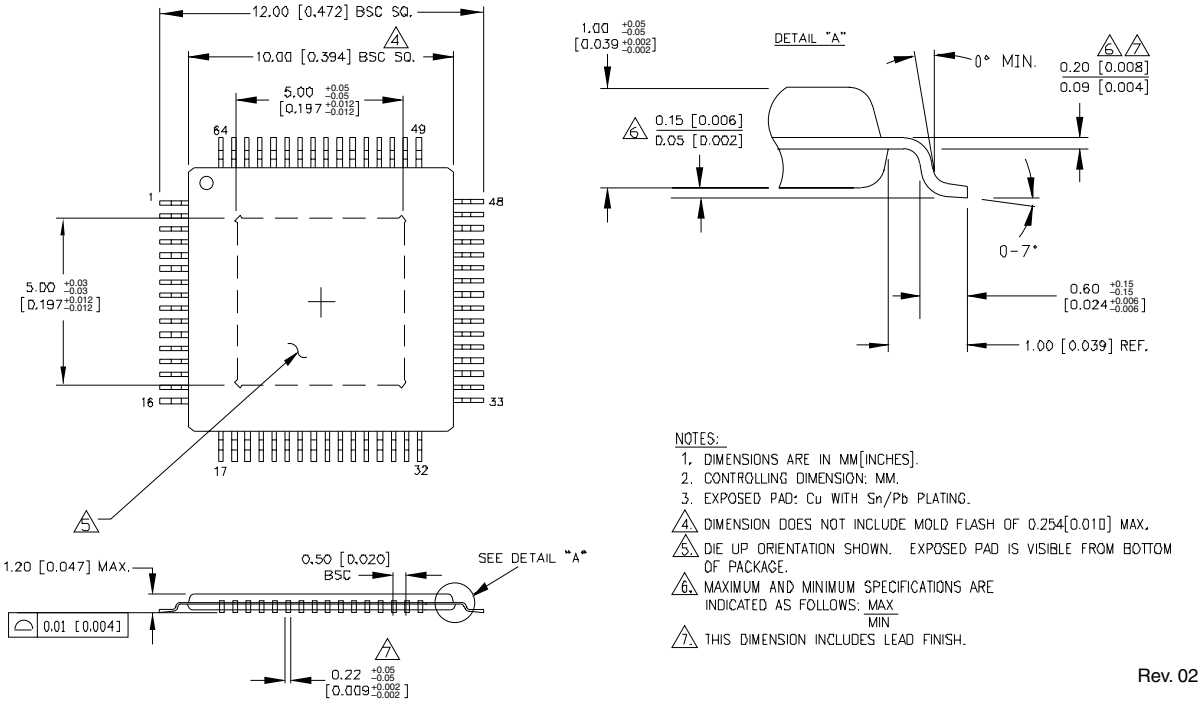


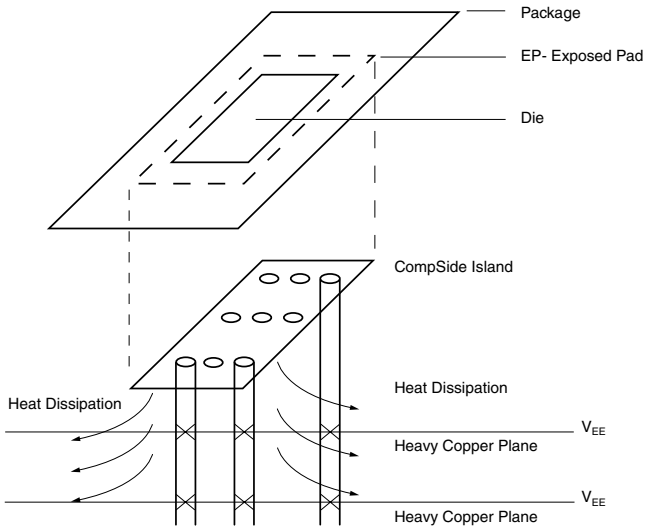
Figure 2. 300MHz Output Waveform

64 LEAD EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are 100% baked and dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

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