

FEATURES

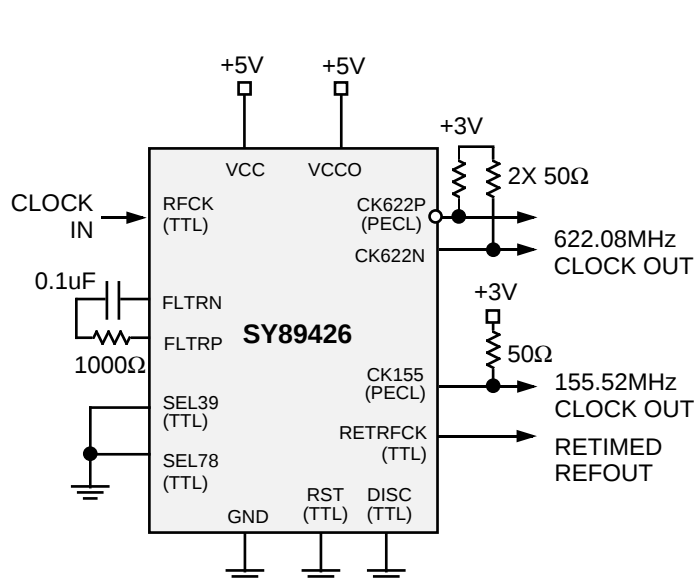
- Single chip source for 622.08MHz and 155.52MHz clocks
- 622.08MHz output is differential PECL, 155.52MHz output is single-ended PECL
- TTL/CMOS compatible inputs and reference output
- SONET compliant jitter performance ($\leq 0.01\text{UI}$)
- Choice of three reference frequencies
- Only 395mW (typ)
- Complies with Bellcore, CCITT and ANSI standards
- Single +5 volt power supply
- Fully compatible with industry standard 10KH I/O levels
- Available in 28-pin PLCC package

DESCRIPTION

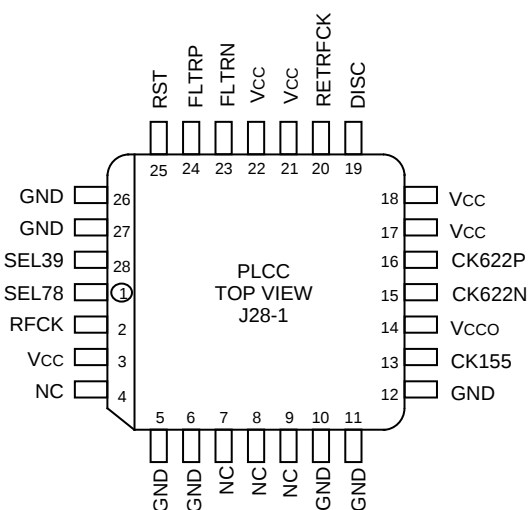
Micrel-Synergy's SY89426 Multi-Output Phase Locked Loop (PLL) is a SONET compliant clock generator providing 622.08MHz, 155.52MHz and retimed reference clock outputs. The PLL produces low jitter OC-12/STS-12 and OC-3/STS-3 rate clocks from an input reference clock of 38.88, 51.84, or 77.76MHz. Additionally, the input reference clock is retimed and provided as a TTL/CMOS compatible output, which may be disabled to minimize switching noise. The SY89426 operates from a single +5 volt supply, and requires only a simple series RC loop filter.

Coupling Micrel-Synergy's advanced PLL technology with our proprietary ASSET™ bipolar process has produced a clock generator IC which exceeds applicable Bellcore and ANSI specifications, while setting a new standard for performance and flexibility.

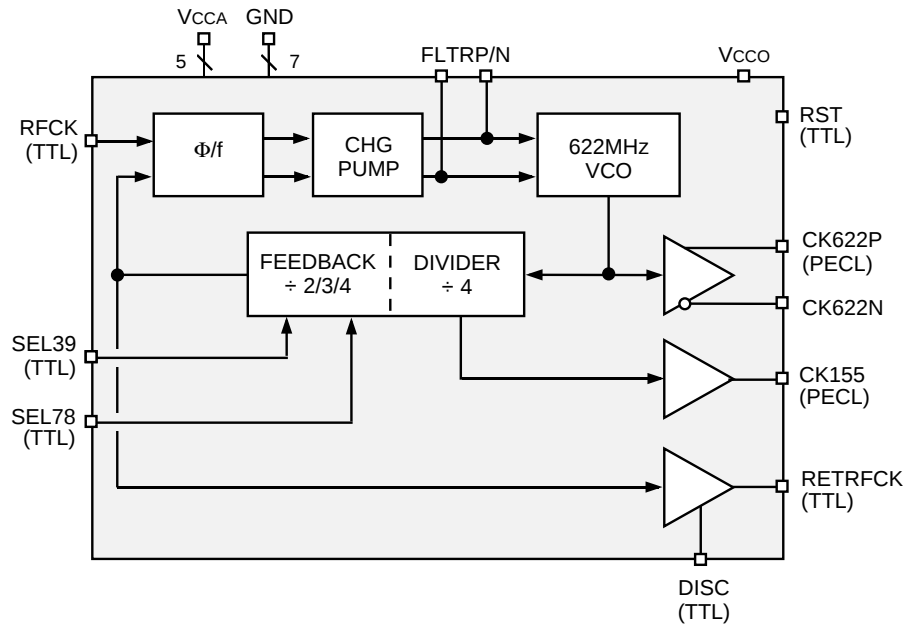
TYPICAL APPLICATION



PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

INPUTS**RFCK [Reference Clock] TTL**

Reference clock IN. (38.88, 51.84 or 77.76MHz).

SEL39 [38.88MHz Select] TTL

Logic HIGH on this pin denotes a 38.88MHz input reference clock. Tie to logic LOW if input is not 38.88MHz.

SEL78 [77.76MHz Select] TTL

Logic HIGH on this pin denotes a 77.76MHz input reference clock. Tie to logic LOW if input is not 77.76MHz.

RST [Reset] TTL

Tie to logic LOW for normal operation; logic HIGH forces reset of internal Phase Detector & feedback dividers.

FLTRP, FLTRN [Loop Filter, Pos & Neg] Analog

Connect a series RC loop filter between these pins. The suggested RC values are 500Ω and 0.1μF, as shown in the Typical Application.

DISC [Disable Clock] TTL

Logic HIGH on this pin disables the Retimed Reference Clock output (RETRFCK); if this output is not required, it is recommended that it be disabled to reduce switching noise. A logic LOW enables the output.

OUTPUTS

CK622P, CK622N [622 Clock Output] Differential PECL. 622.08MHz output clock from PLL B.

CK155 [155 Clock Out] Single-ended PECL. 155.52MHz output clock.

RETRFCK [Retimed Reference Clock Out] TTL

An output clock with the same frequency as the input Reference Clock (RFCK) and a 45-55% duty cycle. This output is derived by dividing the 622.08MHz output by the appropriate factor (e.g., divide by 16 for a 38.88MHz in/out reference; divide by 12 for 51.84MHz in; or divide by 8 for 77.76MHz in).

POWER & GROUND

VCC +5V for internal circuits.

VCCO +5V for PECL outputs.

GND Ground (0 volts).

REFERENCE FREQUENCY SELECTION⁽¹⁾

SEL39	SEL78	f _{RFCK}
0	0	51.84
0	1	77.76
1	0	38.88
1	1	77.76

NOTE:

1. Airflow greater than 500lfpm is maintained.

ABSOLUTE MAXIMUM RATINGS^{(1), (2)}

Symbol	Parameter	Rating	Unit
V _{CC}	Power Supply	0 to +7	V
V _I	Input Voltage	0 to V _{CC}	V
I _{OUT}	Output Current –Continuous –Surge	50 100	mA
T _A	Operating Temperature Range	–40 to +85	°C
T _{store}	Storage Temperature Range	–65 to +150	°C

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Airflow greater than 500lfpm is maintained.

PECL DC ELECTRICAL CHARACTERISTIC^{(1), (2)}

V_{CC} = V_{CCO} = +5V ± 5%; GND = 0V; T_A = –40°C to 85°C

Symbol	Parameter	T _A = –40°C		T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} -1130	V _{CC} -840	V _{CC} -1070	V _{CC} -790	V _{CC} -1030	V _{CC} -760	V _{CC} -960	V _{CC} -670	mV
V _{OL}	Output LOW Voltage	V _{CC} -2000	V _{CC} -1600	V _{CC} -2000	V _{CC} -1580	V _{CC} -2000	V _{CC} -1580	V _{CC} -2000	V _{CC} -1545	mV
V _{IH}	Input HIGH Voltage ⁽¹⁾	V _{CC} -1230	V _{CC} -890	V _{CC} -1170	V _{CC} -840	V _{CC} -1130	V _{CC} -810	V _{CC} -1060	V _{CC} -720	mV
V _{IL}	Input LOW Voltage ⁽¹⁾	V _{CC} -1950	V _{CC} -1500	V _{CC} -1950	V _{CC} -1480	V _{CC} -1950	V _{CC} -1480	V _{CC} -1950	V _{CC} -1445	mV
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	μA

NOTES:

1. Forcing one input at a time. Apply V_{IH} (Max) or V_{IL} (Min) to all other inputs.
2. Airflow greater than 500lfpm is maintained.

TTL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = V_{CCO} = +5V ± 5%; GND = 0V; T_A = –40°C to 85°C

Symbol	Parameter	Min.	Max.	Unit	Condition
V _{OH}	Output HIGH Voltage	2.4	—	V	I _{OH} = –2mA
V _{OL}	Output LOW Voltage	—	0.5	V	I _{OL} = 4mA
I _{OS}	Output Short Circuit Current	–150	–60	mA	V _{OUT} = 0
V _{IH}	Input HIGH Voltage	2.0	—	V	—
V _{IL}	Input LOW Voltage	—	0.8	V	—

NOTE:

1. Airflow greater than 500lfpm is maintained.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{CC} = V_{CCO} = +5V ± 5%; GND = 0V; T_A = -40°C to 85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{EE}	Internal Operating Current	—	79	120	mA	
I _{OUT}	Termination Output Current	—	11	—	mA	50Ω to V _{CC} -2, 50% duty cycle

NOTE:

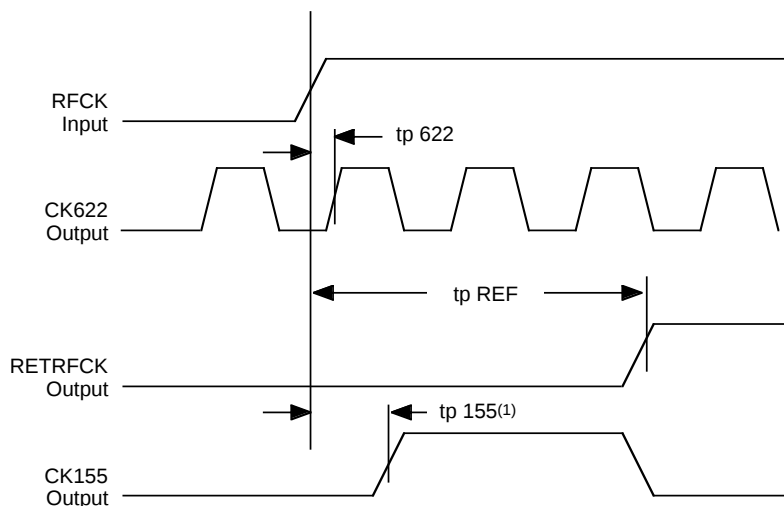
1. Airflow greater than 500lfpm is maintained.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{CC} = V_{CCO} = +5V ± 5%; GND = 0V; T_A = -40°C to 85°C

Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency	622.08 ±1%			MHz	Nominal
Reference Clock (RFCK) Frequency Tolerance	—	±20	—	ppm	77.76MHz
	—	±20	—	ppm	51.84MHz
	—	±10	—	ppm	38.88MHz
Reference Clock (RFCK) Input Duty Cycle	45	—	55	% of UI	
Reference Clock (RETRFCK) Output Duty Cycle	40	—	60	% of UI	15pF load
Acquisition Lock Time	—	—	15	μsec	
TTL Output Rise/Fall Time	—	—	2	ns	10% to 90% of amplitude, 15pF load
PECL Output Rise/Fall Time	—	—	500	ps	10% to 90%, 50Ω load, 5pF cap
CK622 Output Duty Cycle	45	—	55	% of UI	
CK155 Output Duty Cycle	45	—	55	% of UI	
t _{RST} – RST pulse width	1	—	—	μsec	
tp ₆₂₂ Static Phase Offset of CK622	190	400	600	ps	
tp ₁₅₅ Static Phase Offset of CK155	-250	-400	-750	ps	
tp _{REF} Static Phase Offset of RETRFCK	—	+3.5	—	ns	

NOTE:

1. Airflow greater than 500lfpm is maintained.

TIMING WAVEFORM**NOTE:**

1. Does not apply to 52MHz reference

JITTER GENERATION

Jitter Generation Definition

Bellcore TR-NWT-000499 (Issue 4), section 7.3.3 "Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter."

Jitter Generation Requirement

Bellcore TA-NWT-000253 (Issue 2), section 5.6.5.2 "For Category II interfaces, jitter generation shall not exceed 0.01 UI rms. For OC-N and STSX-N interfaces, a high-pass measurement filter with a 12kHz cutoff frequency shall be used." The low-pass cutoff frequency of the measurement filter shall be higher than 5MHz.

The characteristic of the measurement filter is shown below.

SONET OC-12 Category II Jitter Generation Measurement Filter Characteristics

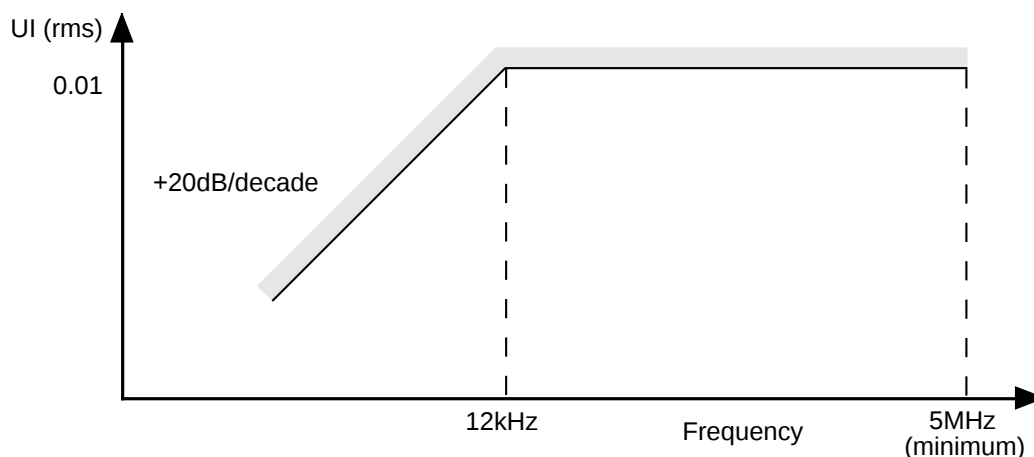
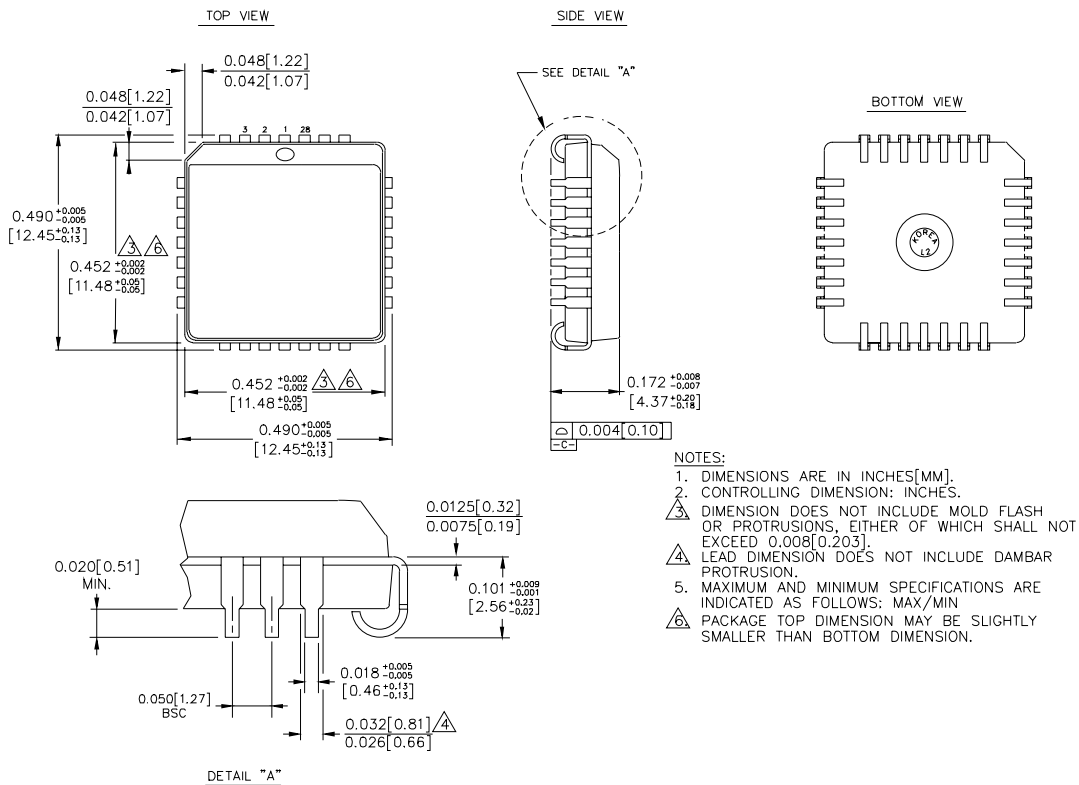


Figure 1

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89426JC	J28-1	Commercial
SY89426JCTR	J28-1	Commercial
SY89426JI	J28-1	Industrial
SY89426JITR	J28-1	Industrial

28 LEAD PLCC (J28-1)

Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USATEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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