5V/3.3V DUAL HIGH-PERFORMANCE PHASE LOCKED LOOP

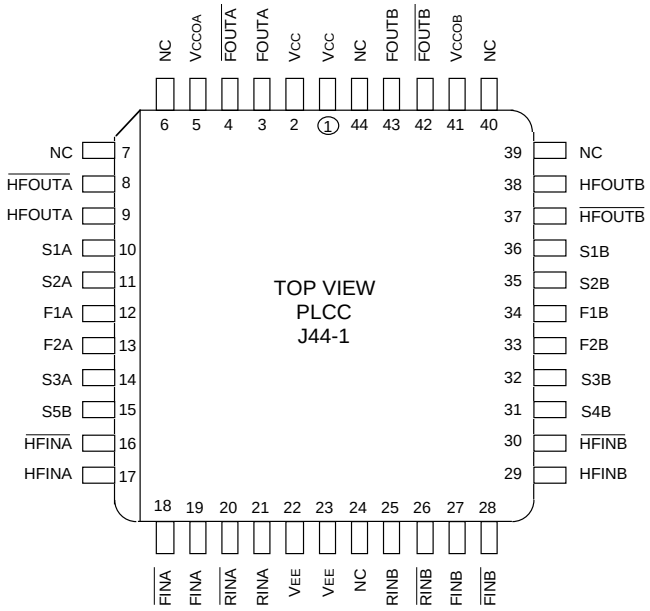
FEATURES

- 3.3V and 5V power supply options
- 1.12GHz maximum VCO frequency
- 30MHz to 560MHz reference input operating frequency
- External 2.0GHz VCO capability
- Frequency doubler mode
- Low jitter differential design
- PECL differential outputs
- External loop filter optimizes performance/cost
- Available in 44-pin PLCC package

APPLICATIONS

- Workstations
- Advanced communications
- High-performance computing

PIN CONFIGURATION



DESCRIPTION

The SY89423V device consists of two identical, low jitter, digital Phase Locked Loops based on Micrel-Synergy's differential PLL technology. Each PLL is capable of operating in the 30MHz to 560MHz reference input frequency range, and is independent of the other, and is configurable separately. The PLLs can be configured to be matched in all regards, or can be configured so that PLLB is used as a frequency doubler, while PLLA is used to regenerate the undoubled frequency. Each PLL is capable of operating up to 2000MHz with the HFIN input and an external VCO.

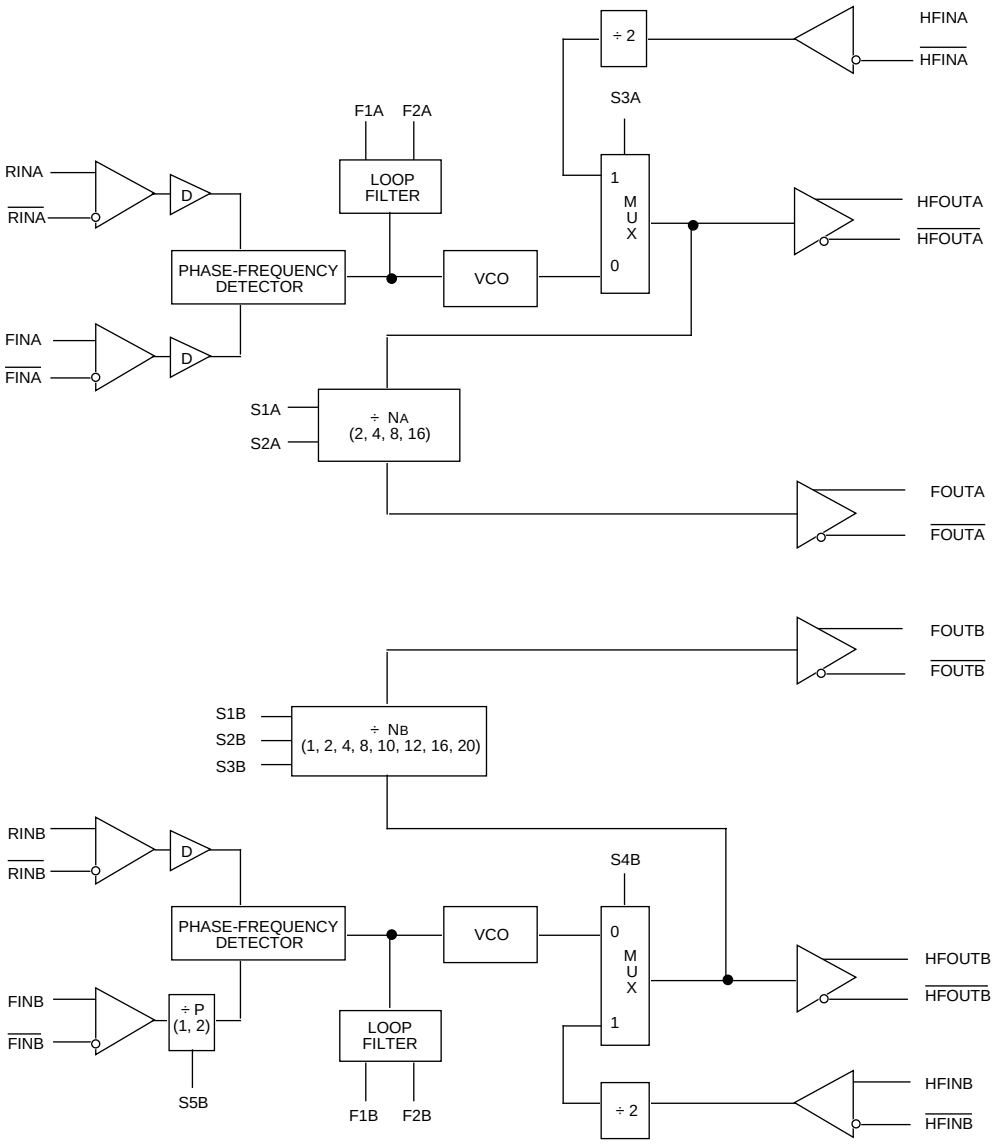
Two reference inputs (RINX and $\overline{\text{RINX}}$), two feedback inputs (FINX and $\overline{\text{FINX}}$), two high frequency inputs (HFINX and $\overline{\text{HFINX}}$), two filter pins (F1X and F2X), two normal outputs (FOUTX and $\overline{\text{FOUTX}}$), and two high frequency outputs (HFOUTX and $\overline{\text{HFOUTX}}$) are provided for each of the two PLLs. The reference, feedback, and high frequency inputs can be used as either differential or single-ended inputs. External reference voltage generators are required for single-ended drive.

Feedback for the loops is realized by connecting FOUTX, $\overline{\text{FOUTX}}$ to FINX, $\overline{\text{FINX}}$ by means of external circuitry. This allows the user the flexibility of inserting additional circuitry off-chip in the feedback paths, such as an additional divider. Pulldown resistors are required for the FOUTX and $\overline{\text{FOUTX}}$ pins, and for the HFOUTX and $\overline{\text{HFOUTX}}$ pins.

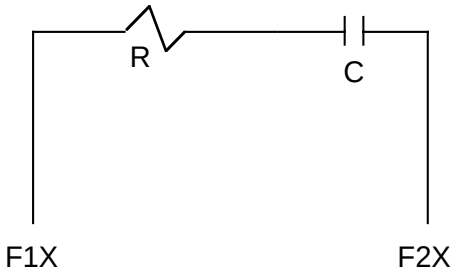
Use of a phase-frequency detector in each PLL results in excellent locking and tracking characteristics. Error correction voltages are generated by the detector if either phase or frequency deviations occur. The VCO in each PLL has a frequency range covering more than a 2:1 ratio from 480MHz to 1120MHz.

Select pins S1A, S2A, S1B, S2B, and S3B are used to program the N dividers for optimum VCO operation, in other words with the VCO operating in the center of its range. When both S3B and S5B are low, PLLB is identical to PLLA. When S5B is high, the 2X frequency multiplication option is enabled. Select pins S3A and S4B enable the HF inputs for PLLA and PLLB respectively, which allows the use of an external VCO in either PLL. All the select pins are TTL inputs.

BLOCK DIAGRAM



LOOP FILTER COMPONENT SELECTION



C = 1.0µF ±10% (X7R dielectric)

R = 560Ω ±10%

PIN NAMES

Pin	Function	I/O
F1A	Filter Pin 1A	I/O
F2A	Filter Pin 2A	I/O
RINA	Inverted Reference Input A	I
$\overline{\text{RINA}}$	Reference Input A	I
FINA	Feedback Input A	I
$\overline{\text{FINA}}$	Inverted Feedback Input A	I
HFINA	High Frequency Input A	I
$\overline{\text{HFINA}}$	Inverted High Frequency Input A	I
FOUTA	Frequency Output A	O
$\overline{\text{FOUTA}}$	Inverted Frequency Output A	O
HFOUTA	High Frequency Output A	O
$\overline{\text{HFOUTA}}$	Inverted High Frequency Output A	O
F1B	Filter Pin 1B	I/O
F2B	Filter Pin 2B	I/O
RINB	Reference Input B	I
$\overline{\text{RINB}}$	Inverted Reference Input B	I
FINB	Feedback Input B	I
$\overline{\text{FINB}}$	Inverted Feedback Input B	I
HFINB	High Frequency Input B	I
$\overline{\text{HFINB}}$	Inverted High Frequency Input B	I
FOUTB	Frequency Output B	O
$\overline{\text{FOUTB}}$	Inverted Frequency Output B	O
HFOUTB	High Frequency Output B	O
$\overline{\text{HFOUTB}}$	Inverted Frequency Output B	O
V_{CC}	V_{CC}	—
V_{CCOA}	Output V_{CC}	—
V_{CCOB}	Output V_{CC}	—
V_{EE}	V_{EE} (0V)	—
S1A	Select Input 1A (TTL)	I
S2A	Select Input 2A (TTL)	I
S3A	Select Input 3A (TTL)	I
S1B	Select Input 1B (TTL)	I
S2B	Select Input 2B (TTL)	I
S3B	Select Input 3B (TTL)	I
S4B	Select Input 4B (TTL)	I
S5B	Select Input 5B (TTL)	I

PIN DESCRIPTION

RINA, $\overline{\text{RINA}}$, RINB, $\overline{\text{RINB}}$

Reference frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

FINA, $\overline{\text{FINA}}$, FINB, $\overline{\text{FINB}}$

Feedback frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

HFINA, $\overline{\text{HFINA}}$, HFINB, $\overline{\text{HFINB}}$

High frequency feedback inputs. Differential drive is recommended.

F1A, F2A, F1B, F2B

These pins are connection points for the loop filters, which are to be provided off-chip. F1X is the high impedance side, F2X is the reference side. The loop filter should be a first order, low pass with a DC block. The difference voltage on these pins will be a DC level, which is controlled by the loop feedback and determined by the required VCO frequency.

FOUTA, $\overline{\text{FOUTA}}$, FOUTB, $\overline{\text{FOUTB}}$

Frequency outputs for the loops. These are differential, positive referenced, emitter-follower signals and must be terminated off-chip. Termination in 50 ohms is recommended.

HFOUTA, $\overline{\text{HFOUTA}}$, HFOUTB, $\overline{\text{HFOUTB}}$

High frequency outputs. These are differential, positive referenced, emitter-follower signals and must be terminated off-chip. Termination in 50 ohms is recommended.

S1A, S2A, S3A, S1B, S2B, S3B, S4B, S5B

These inputs are used to select the configuration for PLLA and PLLB. See the Frequency Selection Table for details of the logic.

V_{CC}

This is the positive supply for the chip. It should be decoupled and present a low impedance in order to assure low-jitter operation.

V_{CCOA}, V_{CCOB}

These are the positive supplies for the output buffers. They are constrained to be equal to or less than the value of V_{CC}.

V_{EE}

This pin is the negative supply for the chip and is normally connected to ground (0V).

FREQUENCY SELECTION TABLE

PLLA

S3A	S2A	S1A	NA	FOUTA (MHz)	HFOUTA (MHz)
0	0	0	2	240 – 560	480 – 1120
0	0	1	4	120 – 280	480 – 1120
0	1	0	8	60 – 140	480 – 1120
0	1	1	16	30 – 70	480 – 1120
1	0	0	2	HFINA divide by 4	HFINA divide by 2
1	0	1	4	HFINA divide by 8	HFINA divide by 2
1	1	0	8	HFINA divide by 16	HFINA divide by 2
1	1	1	16	HFINA divide by 32	HFINA divide by 2

PLLB

S4B	S3B	S2B	S1B	NB	FOUTB (MHz)	HFOUTB (MHz)
0	0	0	0	2	240 – 560	480 – 1120
0	0	0	1	4	120 – 280	480 – 1120
0	0	1	0	8	60 – 140	480 – 1120
0	0	1	1	16	30 – 70	480 – 1120
0	1	0	0	1	480 – 1120	480 – 1120
0	1	0	1	10	48 – 112	480 – 1120
0	1	1	0	12	40 – 93.3	480 – 1120
0	1	1	1	20	24 – 56	480 – 1120
1	0	0	0	2	HFINB divide by 4	HFINB divide by 2
1	0	0	1	4	HFINB divide by 8	HFINB divide by 2
1	0	1	0	8	HFINB divide by 16	HFINB divide by 2
1	0	1	1	16	HFINB divide by 32	HFINB divide by 2
1	1	0	0	1	HFINB divide by 2	HFINB divide by 2
1	1	0	1	10	HFINB divide by 20	HFINB divide by 2
1	1	1	0	12	HFINB divide by 24	HFINB divide by 2
1	1	1	1	20	HFINB divide by 40	HFINB divide by 2

S5B	Divide-by-P	Maximum Feedback Frequency (MHz)
0	P = 1	560
1	P = 2	1120

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_I	TTL Input Voltage[2]	–0.5 to 6.0	V
I_I	TTL Input Current[2]	–30 to +5.0	mA
I_{OUT}	ECL Output Current –Continuous –Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature[3]	0 to +85	°C

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.
3. All DC and AC electrical characteristics are specified over the operating temperature range.

5V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	4.75	—	5.25	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	200	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	56	mA	PECL outputs are open

3.3V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.135	—	3.465	V	$V_{CC} = V_{CCO}$
I_{CC}	Power Supply Current (V_{CC})	—	—	200	mA	
I_{CCO}	Power Supply Current (V_{CCO})	—	—	56	mA	PECL outputs are open

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V$ or $5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	$V_{CC} – 1.025$	—	$V_{CC} – 0.780$	V	
V_{OL}	Output LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.520$	V	
V_{IH}	Input HIGH Voltage	$V_{CC} – 1.165$	—	$V_{CC} – 0.780$	V	
V_{IL}	Input LOW Voltage	$V_{CC} – 1.810$	—	$V_{CC} – 1.475$	V	

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCOA} = V_{CCOB}$ = 3.3V or 5.0V ±5%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
I_{IH}	Input HIGH Current	—	—	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$
I_{IL}	Input LOW Current	—	—	–0.3	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	–1.2	V	$I_{IN} = –12mA$

AC ELECTRICAL CHARACTERISTICS

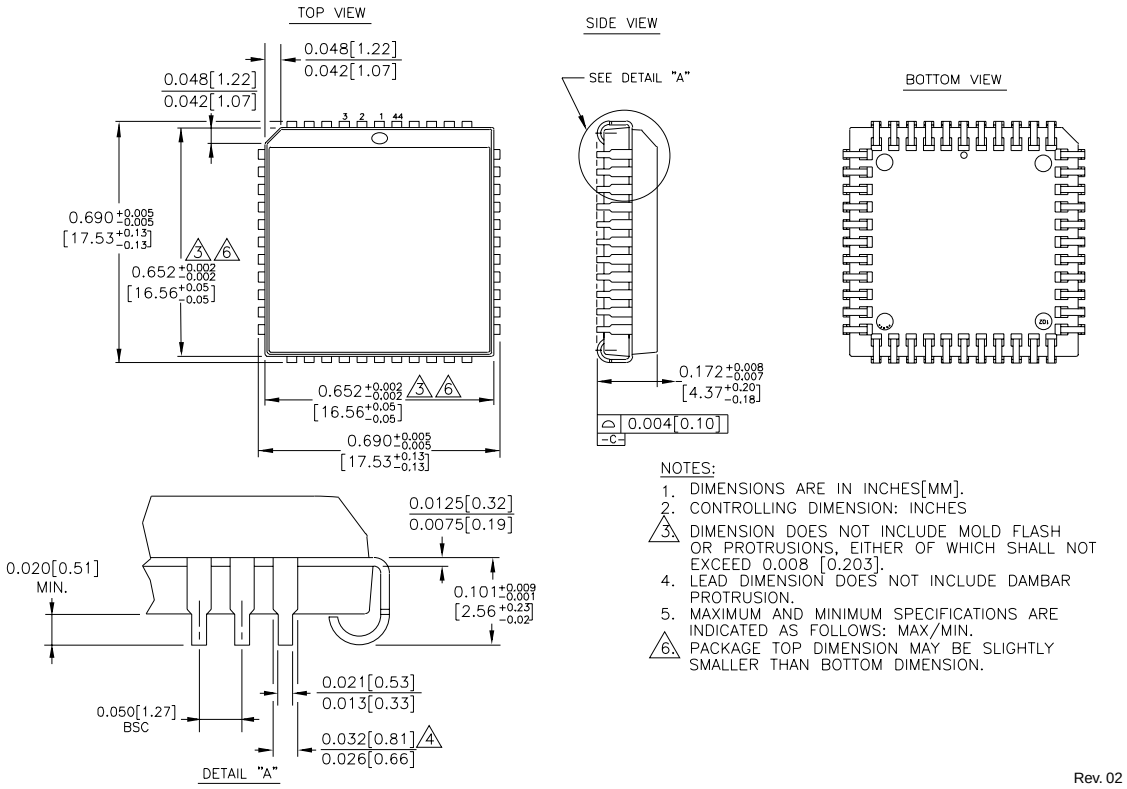
$V_{CC} = V_{CCOA} = V_{CCOB}$ = 3.3V or 5.0V ±5%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ΔT	Output Period Jitter	—	10	15	ps rms	
P_{PW}	Output Duty Cycle	45	50	55	%	
tr tf	Output Rise/Fall Time (20% to 80%)	— —	300 300	550 550	ps	—
RINA, B	Reference Frequency Inputs	—	—	560	MHz	
FINA, B FINB	Feedback Frequency Inputs Feedback Frequency Input	— —	— —	560 1120	MHz MHz	S5B = 0 S5B = 1
HFINA, B	High Frequency Inputs	—	—	2000	MHz	
HFOUTA, B	High Frequency Outputs	—	—	1120	MHz	
FOUTA	Frequency Outputs PLLA	—	—	560	MHz	
FOUTB	Frequency Outputs PLLB	—	—	1120	MHz	

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89423VJC	J44-1	Commercial
SY89423VJCTR	J44-1	Commercial

44 LEAD PLCC (J44-1)



MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.micrel.com