



# 3.3V/5V, 4GHz PECL/ECL ÷ 4 CLOCK GENERATOR

Precision Edge™  
SY89313V

## FEATURES

- Guaranteed AC performance over temperature and voltage
  - > 4GHz  $f_{MAX}$  input frequency
  - < 240ps  $t_r/t_f$
  - < 500ps  $T_{PD}$
- 3.3V and 5V power supply operation
- 100k ECL/PECL compatible I/O
- Wide operating temperature range: -40°C to +85°C
- Available in ultra-small 8-pin MLF™ (2mm x 2mm) package



Precision Edge™

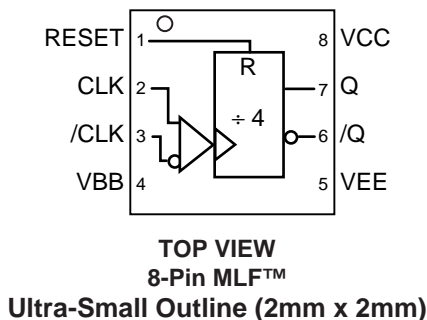
## DESCRIPTION

The SY89313V is a differential ECL/PECL integrated ÷4 divider clock generator. It is functionally equivalent to the SY100EP33V but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint.

The  $V_{BB}$  pin, an internally generated voltage supply, is available for this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also re-bias AC-coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01μF capacitor and limit current sourcing or sinking to 0.5mA. When not used,  $V_{BB}$  should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will be in a random state; the reset allows for the synchronous use of multiple SY89313V's in a system.

## PIN CONFIGURATION/BLOCK DIAGRAM



## TRUTH TABLE (Note 1)

CLK	/CLK	RESET	Q	/Q
X	X	Z	L	H
		L	F	F

Note 1. = LOW-to-HIGH transition  
 = HIGH-to-LOW transition  
 F = Divide by 4 function

**ORDERING INFORMATION****Ordering Information**

Part Number	Package Type	Operating Range	Package Marking
SY89313VMITR*	MLF-8	Industrial	313

\*Tape and Reel

**PIN DESCRIPTION**

Pin Number	Pin Name	Type	Pin Function
2, 3	CLK, /CLK	100k ECL/PECL Input	Differential PECL/ECL Input: Internal 75k $\Omega$ pull-down resistor. If left open, pin defaults LOW. See <i>"Input Interface Applications"</i> section for single-ended inputs.
7, 6	Q, /Q	100k Output	Differential PECL/ECL Output: Output CLK input divided by 4. See <i>"Output Interface Applications"</i> section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1 $\mu$ F//0.01 $\mu$ F low ESR capacitors.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and Exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Reference Voltage: VCC–1.4V. Used as reference voltage for single-ended input or AC-coupling to the CLK, /CLK inputs. Max sink/source is $\pm 0.5$ mA. See <i>"Input Interface Applications"</i> section.
1	Reset	100EP Input	Single-ended Input: PECL/ECL Asynchronous reset.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	–0.5V to +6.0V
Input Voltage ( $V_{IN}$ )	–0.5V to $V_{CC}$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Current ( $V_{BB}$ )	
Source or sink current on $V_{BB}$ , <b>Note 3</b>	$\pm 1.5$ mA
Lead Temperature (soldering, 10 sec.)	+220°C
Storage Temperature ( $T_S$ )	–65°C to +150°C

**Operating Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	3.0V to 3.6V
	4.5V to 5.5V
Ambient Temperature ( $T_A$ )	–40°C to +85°C
Package Thermal Resistance ( <b>Note 4</b> )	
MLF ( $\theta_{JA}$ )	
Still-Air	93°C/W
500lfpm	~87°C/W
MLF ( $\Psi_{JB}$ )	
Junction-to-Board	60°C/W

**PECL/ECL (100K) DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +3.3V \pm 10\%$  or  $+5V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -3.3V \pm 10\%$  or  $-5V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{EE}$	Power Supply Current	Max $V_{CC}$ , No Load	—	30	40	mA
$V_{OH}$	Output HIGH Voltage		$V_{CC} - 1.145$	—	$V_{CC} - 0.895$	V
$V_{OL}$	Output LOW Voltage		$V_{CC} - 1.945$	—	$V_{CC} - 1.695$	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 1.225$	—	$V_{CC} - 0.88$	V
$V_{IL}$	Input LOW Voltage		$V_{CC} - 1.945$	—	$V_{CC} - 1.625$	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range	<b>Note 5</b>	$V_{EE} + 2.0$	—	$V_{CC}$	V
$V_{BB}$	Bias Voltage		$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V
$I_{IH}$	Input HIGH Current		—	—	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current CLK, RESET		0.5	—	—	$\mu\text{A}$
	Input LOW Current /CLK		–150	—	—	$\mu\text{A}$

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Due to the limited drive capability use for input of the same package only.

**Note 4.** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

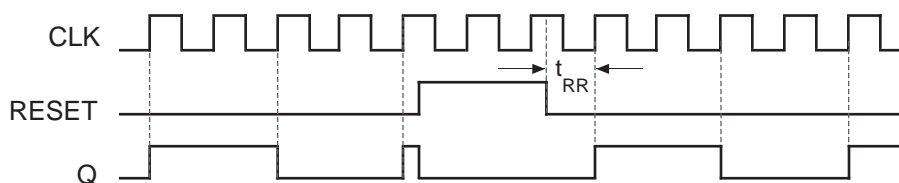
**Note 5.**  $V_{IHCMR}$  (min) varies 1:1 with  $V_{EE}$ , (max) varies 1:1 with  $V_{CC}$ .

**AC ELECTRICAL CHARACTERISTICS (Note 6)**

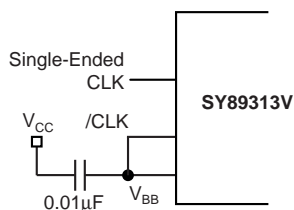
$V_{CC} = +3.3V \pm 10\%$  or  $+5V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -3.3V \pm 10\%$  or  $-5V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Input Frequency		4	—	—	GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output CLK → Q (SY10EP33V) RESET → Q (SY100EP33V) RESET → Q		300 300 310	380 420 420	460 500 500	ps
$t_{RR}$	Set/Reset Recovery		200	100	—	ps
$t_{PW}$	Minimum Pulse Width RESET		550	200	—	ps
$t_{JITTER}$	Cycle-to-Cycle RMS Jitter		—	—	1	ps(rms)
$V_{PP}$	Input Voltage Swing (Differential)		150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% to 80%) Q, /Q		90	180	240	ps

**Note 6.** Measured using a 750mV source, 50% duty cycle clock source. All loading with  $50\Omega$  to  $V_{CC} - 2.0V$ .

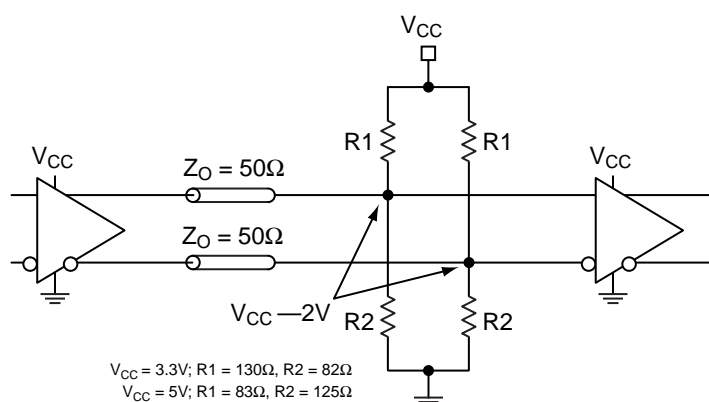
**TIMING DIAGRAM**

## INPUT INTERFACE APPLICATIONS

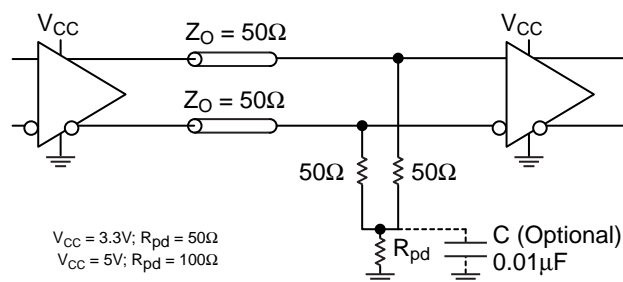


**Figure 1. Single-Ended LVPECL Input  
(Terminating Unused Input)**

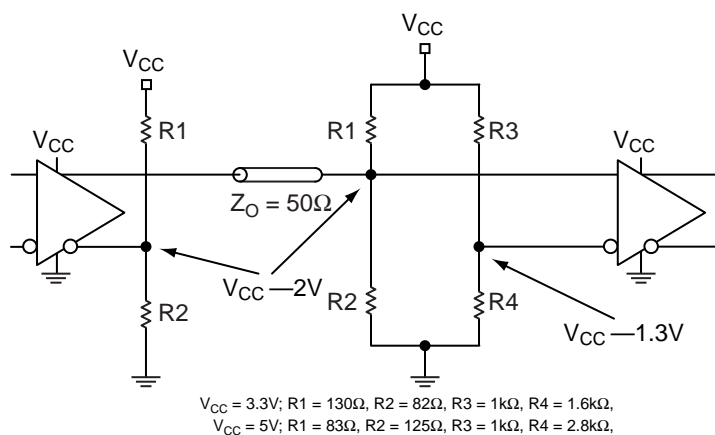
## LVPECL OUTPUT INTERFACE APPLICATIONS



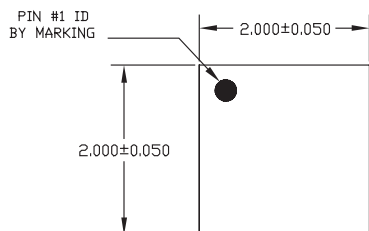
**Figure 2a. Parallel Thevenin-Equivalent  
Termination**



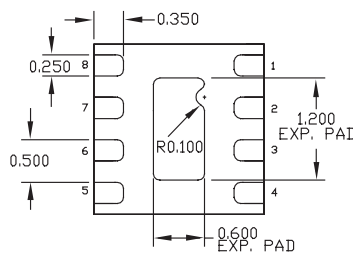
**Figure 2b. Three Resistor  
"Y Termination"**



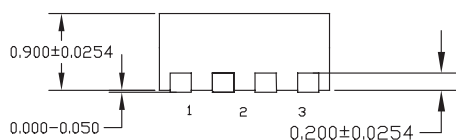
**Figure 2c. Terminating Unused I/O**

**8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)**

TOP VIEW

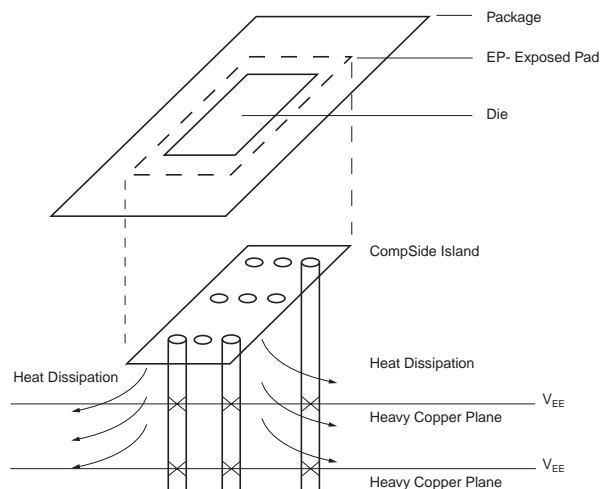


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**PCB Thermal Consideration for 8-Pin MLF™ Package****Package Notes:**

**Note 1.** Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.

**Note 2.** Exposed pads must be soldered to plane equivalent to device  $V_{EE}$  pin's potential for proper thermal management.

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