



5V/3.3V 2.5Gbps VARIABLE OUTPUT SWING PECL/ECL DIFFERENTIAL RECEIVER

Precision Edge™
SY89307V

FEATURES

- 3.3V and 5V power supply options
- >2.5Gbps maximum throughput
- Fast output transitions <160ps t_r / t_f
- 100k compatible PECL/ECL I/O
- Functionally equivalent to SY88927V and SY100EP16VS
- Variable output swing from 100mV to 700mV
- Guaranteed operation over -40°C to $+85^{\circ}\text{C}$ temperature range
- Available in ultra-small 8-pin MLF™ (2mm x 2mm) package

APPLICATIONS

- Multimode optical transceiver
- VCSEL driver
- Backplane receiver



Precision Edge™

DESCRIPTION

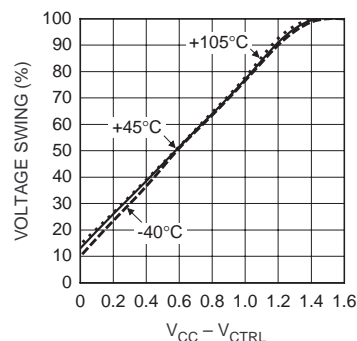
The SY89307V is a differential receiver with a variable output swing. It is functionally equivalent to the SY100EP16VS but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint. Like the EP16VS its variable output swing makes it ideal for use as a VCSEL laser driver.

The operational range of the SY89307V control input is from V_{BB} (maximum output swing) to V_{CC} (minimum output swing). The output swing can be controlled by a variable resistor between the V_{BB} pin and V_{CC} with the wiper driving V_{CTRL} .

The SY89307V provides a V_{BB} output for either single-ended use or as a DC bias for AC-coupling to the device. The V_{BB} pin should be used only as a bias for this device as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to V_{CC} via a $0.01\mu\text{F}$ capacitor.

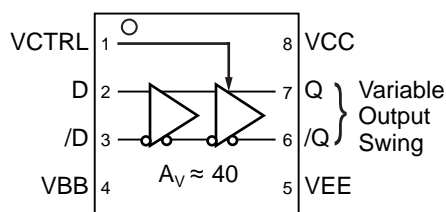
Under open input conditions the Q output will be LOW.

TYPICAL VOLTAGE OUTPUT SWING



Typical Voltage Output Swing
 $V_{CC} = 3.3\text{V or } 5\text{V}$

PACKAGE/ORDERING INFORMATION



TOP VIEW

8-Pin MLF™

Ultra-Small Outline (2mm x 2mm)

Ordering Information

| Part Number | Package Type | Operating Range | Package Marking |
|---------------|--------------|-----------------|-----------------|
| SY89307VMITR* | MLF-8 | Industrial | P16S |

*Tape and Reel

PIN DESCRIPTION

| Pin Number | Pin Name | Type | Pin Function |
|------------|------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2, 3 | D, /D | 100k ECL Input | Differential PECL/ECL Inputs: If inputs are left open, Q output will default to LOW. See <i>"Input Interface Applications"</i> section for single-ended inputs. |
| 7, 6 | Q, /Q | 100k PECL/ECL Output | Differential Outputs: Variable swing PECL/ECL output pair defaults to LOW if D inputs left open. See <i>"Application Implementation"</i> section for recommendations on terminations. |
| 8 | VCC | Positive Power Supply | Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors. |
| 5 | VEE, Exposed Pad | Negative Power Supply | Negative Power Supply: V _{EE} and Exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground. |
| 4 | VBB | Reference Voltage Output | Bias Voltage: V _{CC} -1.3V. Used as reference voltage when AC-coupling to the D, /D inputs. Bypass with 0.01μF capacitor to V _{CC} . |
| 1 | VCTRL | Control Voltage | Voltage Input: Variable voltage input to control output swings. |

Absolute Maximum Ratings(Note 1)

| | |
|----------------------------------------------------|-------------------|
| Supply Voltage (V_{CC}) | –0.5V to +6.0V |
| Input Voltage (V_{IN}) | –0.5V to V_{CC} |
| LVPECL Output Current (I_{OUT}) | |
| Continuous | 50mA |
| Surge | 100mA |
| Input Current | |
| Source or sink current on D, /D | ±50mA |
| Current (V_{BB}) | |
| Source or sink current on V_{BB} , Note 3 | ±1.5mA |
| Lead Temperature (soldering, 10 sec.) | +220°C |
| Storage Temperature (T_S) | –65°C to +150°C |

Operating Ratings(Note 2)

| | |
|-----------------------------------------------|----------------|
| Supply Voltage ($ V_{CC}-V_{EE} $) | 3.0V to 3.6V |
| | 4.5V to 5.5V |
| Ambient Temperature (T_A) | –40°C to +85°C |
| Package Thermal Resistance, (Note 4) | |
| MLF™ (θ_{JA}) | |
| Still-Air | 93°C/W |
| 500lfpm | 87°C/W |
| MLF™ (Ψ_{JB}) | |
| Junction-to-Board | 56°C/W |

PECL/ECL (100K) DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $R_L = 50\Omega$ to $V_{CC} - 2V$ unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|----------------------|------------------------|------------------|-----|------------------|-------|
| I_{EE} | Power Supply Current | Max V_{CC} , no load | — | — | 51 | mA |
| V_{OH} | Output HIGH Voltage | | $V_{CC} - 1.085$ | — | $V_{CC} - 0.88$ | V |
| V_{OL} | Output LOW Voltage | $V_{CTRL} = V_{BB}$ | $V_{CC} - 1.90$ | — | $V_{CC} - 1.650$ | V |
| | Output LOW Voltage | $V_{CTRL} = V_{CC}$ | $V_{CC} - 1.125$ | — | $V_{CC} - 0.975$ | V |
| V_{IH} | Input HIGH Voltage | | $V_{CC} - 1.165$ | — | $V_{CC} - 0.88$ | V |
| V_{IL} | Input LOW Voltage | | $V_{CC} - 1.810$ | — | $V_{CC} - 1.475$ | V |
| V_{BB} | Bias Voltage | | $V_{CC} - 1.38$ | — | $V_{CC} - 1.26$ | V |
| I_{IH} | Input HIGH Current | D, /D | — | — | 150 | μA |
| I_{IL} | Input LOW Current | | 0.5 | — | — | μA |
| | | $V_{CTRL} = V_{IH}$ | | | 80 | μA |

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$ unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|----------------------------------------|----------------------|----------------|----------|----------------|-------|
| f_{MAX} | Maximum Throughput | NRZ Data | 2.5 | — | — | Gbps |
| t_{pd} | Propagation Delay | D (Diff) D (SE) | 100 100 | — 250 | 300 400 | ps |
| V_{PP} | Minimum Input Swing | Note 5 | 150 | — | — | mV |
| V_{CMR} | Common Mode Range | Note 6 | $V_{CC} - 1.3$ | — | $V_{CC} - 0.4$ | V |
| t_r, t_f | Output Rise/Fall Times (20% to 80%) | Q, /Q; Note 7 | — | 95 | 160 | ps |

Note 5. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 when output has a full swing.

Note 6. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}(\text{min.})$ and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{EE} = -3.3V$ and $V_{CC} = 0V$. Note for PECL operation, the $V_{CMR}(\text{min.})$ will be fixed at $3.3V - |V_{CMR}(\text{min.})|$.

Note 7. Output at full swing.

INPUT INTERFACE APPLICATIONS

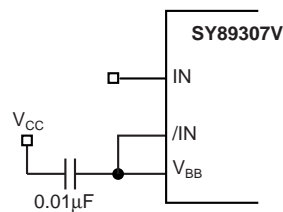


Figure 1. Single-Ended Input
(Terminating Unused Input)

APPLICATION IMPLEMENTATION

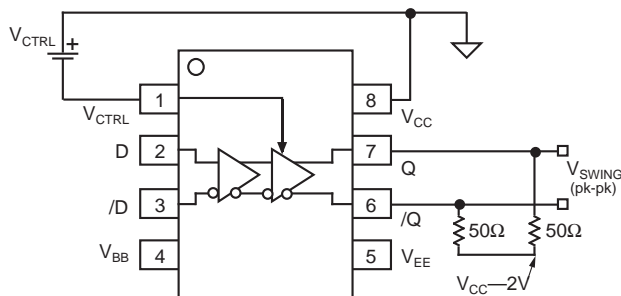


Figure 2. Voltage Source Implementation

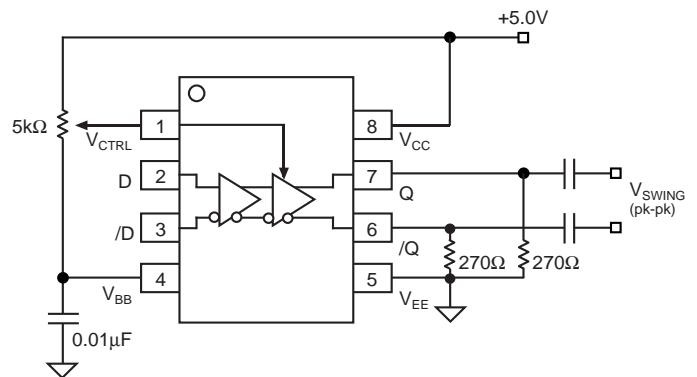
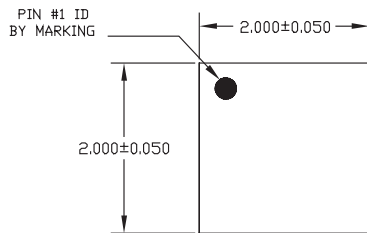
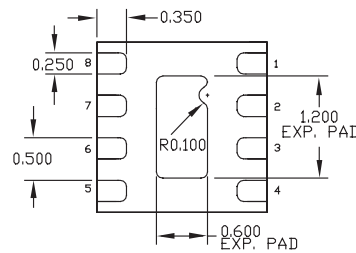


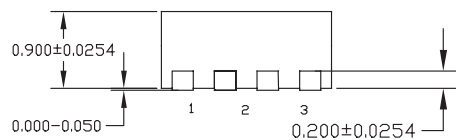
Figure 3. Alternative Implementation

8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)

TOP VIEW

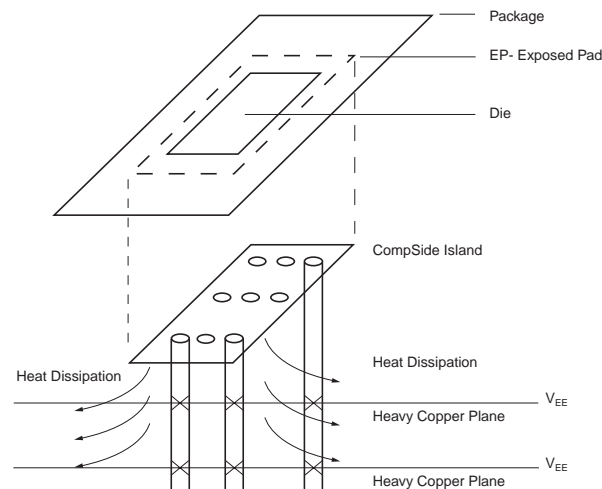


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**PCB Thermal Consideration for 8-Pin MLF™ Package****Package Notes:**

- Note 1.** Package meets Level 2 qualification.
- Note 2.** All parts are dry-packaged before shipment.
- Note 3.** Exposed pads must be soldered to a plane equivalent to device V_{EE} for proper thermal management.

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