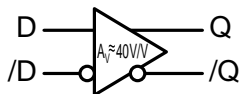


FEATURES

- $f_{MAX} > 2.5\text{GHz}$
- Inputs (D, /D) include $75\text{k}\Omega$ pull-down resistors
- SY89306V: 100k EP compatible
- SY89316V: 10k EP compatible
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$
- Available in an ultra-small 8-pin (2mm x 2mm) MLF™ package

BLOCK DIAGRAM



Precision Edge™

DESCRIPTION

The SY89306V and SY89316V are a high-speed buffer/receivers. The devices are functionally equivalent to the 10/100EP16 buffers, but feature a 70% smaller footprint.

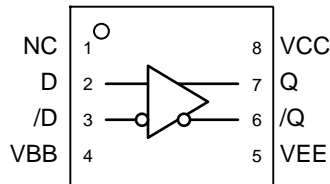
The SY89306/316V includes a V_{BB} reference for single-ended AC-coupling applications. Whenever used, the V_{BB} pin should be bypassed to ground via a $0.01\mu\text{F}$ capacitor. V_{BB} reference can only sink/source 0.5mA .

Under open input conditions (pulled to V_{EE}), internal input clamps will force the Q output LOW.

FUNCTIONAL CROSS REFERENCE

Micrel Part Number	Logic	Functional Cross
SY89306V	100kEP	100EP16V
SY89316V	10kEP	10EP16V

PACKAGE/ORDERING INFORMATION



8-Pin MLF™
Ultra-Small Outline

Ordering Information

Part Number	Package Type	PECL/ECL Logic	Operating Range	Package Marking
SY89306VMITR*	MLF-8	100KEP	Industrial	306
SY89316VMITR*	MLF-8	10KEP	Industrial	316

*Tape and Reel

PIN DESCRIPTION

SY89306V

Pin Number	Pin Name	Type	Pin Function
2, 3	D, /D	100k ECL Input	Differential PECL/ECL Input: The signal inputs include internal 75kΩ pull-down resistors. If inputs are left open, Q output will default to LOW. See <i>"Input Interface Applications"</i> section for single-ended inputs.
7, 6	Q, /Q	100k ECL Output	Differential PECL/ECL Output: Defaults to LOW if D inputs left open. See <i>"Output Interface Applications"</i> section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: V _{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V _{CC} -1.4V. Used as reference voltage when AC coupling to the D, /D inputs. Max sink/source is ±0.5mA.
1	NC		No connection.

SY89316V

Pin Number	Pin Name	Type	Pin Function
2, 3	D, /D	10k ECL Input	Differential PECL/ECL Input: The signal inputs include internal 75kΩ pull-down resistors. If inputs are left open, Q output will default to LOW. See <i>"Input Interface Applications"</i> section for single-ended inputs.
7, 6	Q, /Q	10k ECL Output	Differential PECL/ECL Output: Defaults to LOW if D inputs left open. See <i>"Output Interface Applications"</i> section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: V _{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V _{CC} -1.4V. Used as reference voltage when AC coupling to the D, /D inputs. Max sink/source is ±0.5mA.
1	NC		No connection.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{EE}) ($V_{CC} = 0V$)	-6.0V to 0V
Power Supply Voltage (V_{CC}) ($V_{EE} = 0V$)	+6.0V to 0V
Input Voltage (V_{IN})		
($V_{CC} = 0V$, V_{IN} not more negative than V_{EE})		-6.0V to 0V
($V_{EE} = 0V$, V_{IN} not more negative than V_{CC})		+6.0V to 0V
Output Current (I_{OUT})		
Continuous	50mA
Surge	100mA
V_{BB} Sink/Source Current (I_{BB})	$\pm 0.5mA$
Lead Temperature (soldering, 10 sec.)	220°C
Storage Temperature (T_S)	-65°C to +150°C

Operating Ratings(Note 2)

Power Supply Voltage ($ V_{CC}-V_{EE} $)	3.0V to 3.6V
	4.5V to 5.5V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance Note 3		
MLF™ (θ_{JA})		
Still-Air	93°C/W
500lfpm	87°C/W
MLF™ (ψ_{JB})	60°C/W

SY89306V (100K ECL) DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$ unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{EE}	Power Supply Current				48	mA
V_{OH}	Output HIGH Voltage	Note 4, 5	$V_{CC}-1.085$	—	$V_{CC}-0.880$	V
V_{OL}	Output LOW Voltage	Note 4, 5	$V_{CC}-1.830$	—	$V_{CC}-1.555$	V
V_{IH}	Input HIGH Voltage		$V_{CC}-1.165$	—	$V_{CC}-0.880$	V
V_{IL}	Input LOW Voltage		$V_{CC}-1.810$	—	$V_{CC}-1.475$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range	Note 6	$V_{EE}+2.0$	—	$V_{CC}-4.0$	V
V_{BB}	Bias Voltage		$V_{CC}-1.38$	—	$V_{CC}-1.26$	V
I_{IH}	Input HIGH Current		—	—	150	μA
I_{IL}	Input LOW Current		0.5	—	—	μA

SY89316V (10K ECL) DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$ unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{EE}	Power Supply Current				48	mA
V_{OH}	Output HIGH Voltage	Note 4, 5	$V_{CC}-1.08$	—	$V_{CC}-0.72$	V
V_{OL}	Output LOW Voltage	Note 4, 5	$V_{CC}-1.95$	—	$V_{CC}-1.595$	V
V_{IH}	Input HIGH Voltage		$V_{CC}-1.23$	—	$V_{CC}-0.72$	V
V_{IL}	Input LOW Voltage		$V_{CC}-1.95$	—	$V_{CC}-1.445$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range	Note 6	$V_{EE}+2.0$	—	$V_{CC}-4.0$	V
V_{BB}	Bias Voltage		$V_{CC}-1.43$	—	$V_{CC}-1.19$	V
I_{IH}	Input HIGH Current		—	—	150	μA
I_{IL}	Input LOW Current		0.5	—	—	μA

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $R_L = 50\Omega$ to $V_{CC} - 2V$;
 $T_A = -40^\circ C$ to $+85^\circ C$; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Input Frequency	Note 7	2.5			GHz
t_{PLH} t_{PHL}	Propagation Delay (Differential)	D to Q, /Q; Note 8	100		300	ps
t_{SKEW}	Duty-Cycle Skew	Note 9		8	30	ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)	Q, /Q	60	110	180	ps

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Package Thermal Resistance values assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Note 4. Output loaded with 50Ω to $V_{CC} - 2V$.

Note 5. $V_{IN} = V_{IL}(\text{min})$ or $V_{IH}(\text{max})$

Note 6. V_{IHCMR} (Min) varies 1:1 with V_{EE} , (max) varies 1:1 with V_{CC} .

Note 7. f_{MAX} guaranteed for functionality only, $V_{OUT} \geq 400mV$. V_{OL} and V_{OH} levels are guaranteed at DC only.

Note 8. $V_{IN} = 800mV$.

Note 9. Duty-cycle skew is the difference between the t_{PLH} and t_{PHL} propagation delay.

INPUT INTERFACE APPLICATIONS

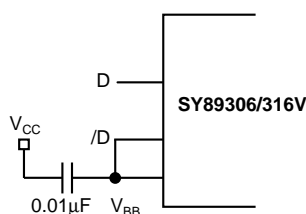


Figure 1. Single-Ended LVPECL Input
(Terminating Unused Input)

LVPECL OUTPUT INTERFACE APPLICATIONS

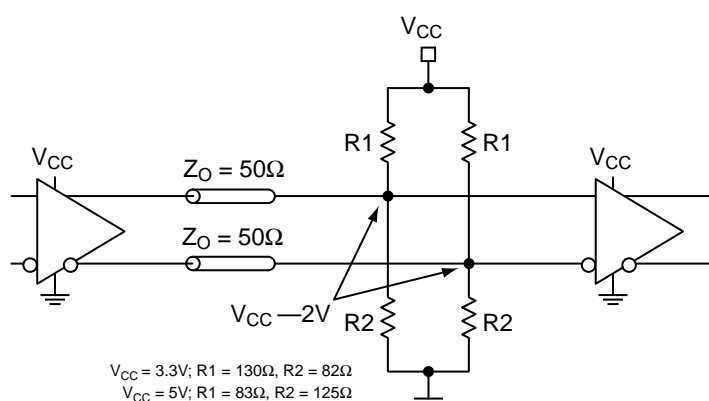


Figure 2a. Parallel Thevenin-Equivalent
Termination

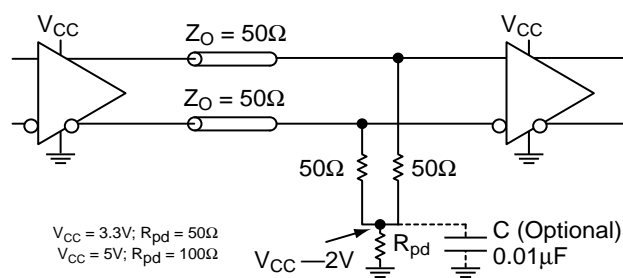


Figure 2b. Three Resistor
"Y Termination"

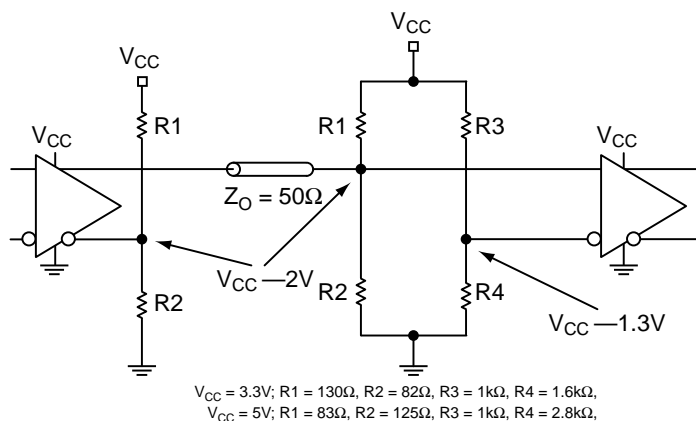
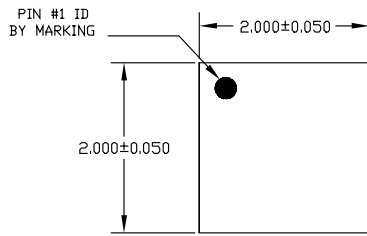


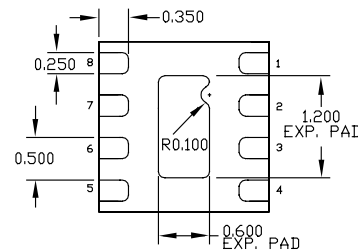
Figure 2c. Terminating Unused I/O

RELATED PRODUCT AND SUPPORT DOCUMENTATION

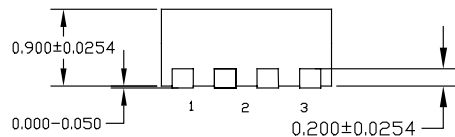
Part Number	Function	Data Sheet Link
SY89206/216V	3.3V/5V 1GHz Differential PECL/ECL Receiver/Buffer	www.micrel.com/product-info/products/sy89206-216v.shtml
SY89223L	3.3V Dual Differential LVPECL-to-LVTTL Translator	www.micrel.com/product-info/products/sy89223l.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)

TOP VIEW

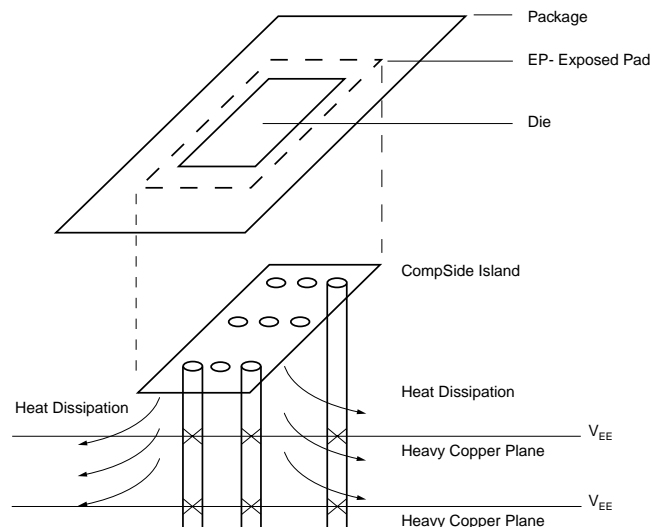


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**PCB Thermal Consideration for 8-Pin MLF™ Package****Package Notes:**

- Note 1.** Package meets Level 2 Moisture Sensitivity Classification and is shipped in Dry-pack form.
- Note 2.** Exposed pads must be soldered to the most negative supply plane, equivalent to V_{EE} , for proper thermal management.

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