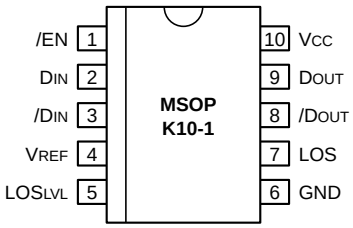
2.5Gbps HIGH-SPEED LIMITING POST AMPLIFIER

FEATURES

- Up to 2.5Gbps operation
- Low noise
- Chatter-Free LOS generation
- Open Collector TTL LOS output
- TTL /EN Input
- Differential PECL inputs for data
- Single power supply
- Designed for use with SY88922 and SY88904 or SY88905
- Available in a tiny 10-pin (3mm) MSOP

PIN CONFIGURATION



DESCRIPTION

The SY88923 limiting post amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 2.5Gbps. Signals as small as 5mVp-p can be amplified to drive devices with PECL inputs. The SY88923 generates a chatter-free Loss of Signal (LOS) open collector TTL output.

The SY88923 incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the /EN input of the device to maintain stability under loss of signal condition. Using LOSLVL pin, the sensitivity of the level detection can be adjusted. The LOSLVL voltage can be set by connecting a resistor divider between VCC and VREF. Figure 3 and Figure 4 show the relationship between input level sensitivity and the voltage set on LOSLVL. Figure 5 shows the relationship between input level sensitivity and resistor divider ratio.

The LOS output is a TTL open collector output that requires a pull-up resistor for proper operation, Figure 1.

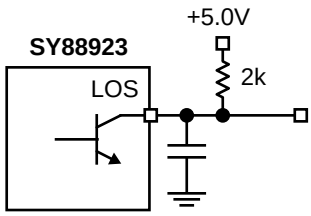
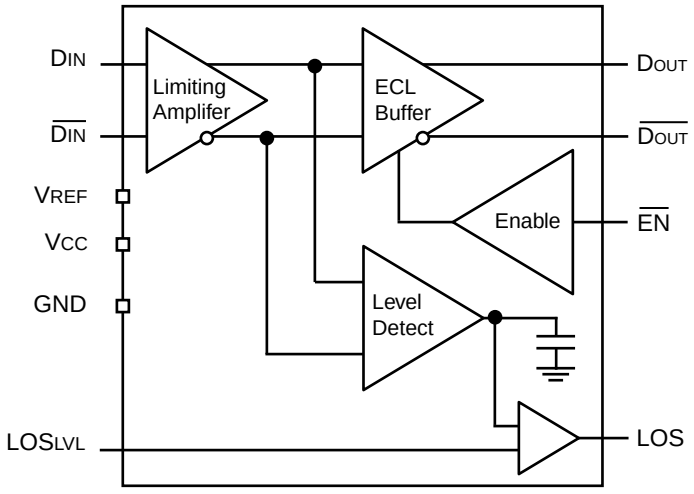


Figure 1. LOS Output with Desired Rise Time

APPLICATIONS

- 1.25Gbps Gigabit Ethernet
- 531Mbps and 1062Mbps Fibre Channel
- 622Mbps SONET
- Gigabit interface converter
- 2.5Gbps SDH/SONET

BLOCK DIAGRAM



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PIN NAMES

Pin	Type	Function
DIN	Data Input	Data Input
/DIN	Data Input	Inverting Data Input
LOS LVL	Input	LOS Limit Set
/EN	TTL Input	Output Enable (Active Low)
LOS	TTL Output (Open Collector)	Loss of Signal Indicator (Active High)
GND	Ground	Ground
/DOUT	PECL Output	Inverting Data Output
DOUT	PECL Output	Data Output
VCC	Power Supply	Positive Power Supply
VREF	Output	Reference Voltage Output for LOS Level Set (see Fig. 3)

GENERAL DESCRIPTION

General

The SY88923 is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optics link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The SY88923 limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The /EN pin allows the user to disable the output signal without removing the input signal.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VCC	Power Supply Voltage	0 to +7.0	V
DIN, /DIN	Input Voltage	0 to VCC	V
DOUT, /DOUT	Output Voltage (with 50Ω load)	VCC –2.5, VCC +0.3	V
TA	Operating Temperature Range	–40 to +85	°C
Tstore	Storage Temperature Range	–55 to +125	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±10%, R_{LOAD} = 50Ω to V_{CC}-2V, T_A = –40°C to +85°C

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{CC}	Power Supply Current(1)	—	35	—	35	—	21	35	—	35	mA
I_{IL}	/EN Input LOW Current	–0.3(8)	—	–0.3(8)	—	–0.3(8)	—	—	–0.3(8)	—	mA
I_{IH}	/EN Input HIGH Current	— —	20(5) 100(6)	— —	20(5) 100(6)	— —	— —	20(5) 100(6)	— —	20(5) 100(6)	µA
V_{CMR}	Common Mode Range	GND +2.0	V_{CC} –1.0	GND +2.0	V_{CC} –1.0	GND +2.0	—	V_{CC} –1.0	GND +2.0	V_{CC} –1.0	V
V_{offset}	Differential Output Offset	—	±100	—	±100	—	—	±100	—	±100	mV
LOS_{LVL}	LOS_{LVL} Level(2)	V_{REF}	V_{CC}	V_{REF}	V_{CC}	V_{REF}	—	V_{CC}	V_{REF}	V_{CC}	V
V_{OL}	LOS Output Low Level(3)	—	0.5	—	0.5	—	—	0.5	—	0.5	V
I_{OH}	LOS Output Leakage(4)	—	250	—	250	—	—	250	—	250	uA
V_{OH}	D_{OUT} and /D_{OUT} HIGH Output	V_{CC}–1085	V_{CC}–880	V_{CC}–1025	V_{CC}–880	V_{CC}–1025	V_{CC}–955	V_{CC}–880	V_{CC}–1025	V_{CC}–880	mV
V_{OL}	D_{OUT} and /D_{OUT} LOW Output	V_{CC}–1830	V_{CC}–1555	V_{CC}–1810	V_{CC}–1620	V_{CC}–1810	V_{CC}–1705	V_{CC}–1620	V_{CC}–1810	V_{CC}–1620	mV
V_{REF}	Reference Supply(7)	V_{CC}–2.625	V_{CC}–2.325	V_{CC}–2.625	V_{CC}–2.325	V_{CC}–2.625	V_{CC}–2.475	V_{CC}–2.325	V_{CC}–2.625	V_{CC}–2.325	V
V_{IH}	/EN Input HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V
V_{IL}	/EN Input LOW Voltage	—	0.8	—	0.8	—	—	0.8	—	0.8	V

NOTES:

1. No output load.
2. 2^{23}-1 pattern.
3. I_{OL} = + 2mA.
4. V_{OH} = 5.5V.
5. V_{IN} = 2.7.
6. V_{IN} =V_{CC}.
7. I_{REF} must be limited within –0.8mA (source) and 0.4mA (sink).
8. V_{IN} = 0.5V.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±10%, R_{LOAD} = 50Ω to V_{CC} - 2V, T_A = –40°C to +85°C

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
PSRR	Power Supply(1) Rejection Ratio	—	—	—	—	—	35	—	—	—	dB	Input referred, 55MHz
V_{ID}	Input Voltage Range	5	1800	5	1800	5	—	1800	5	1800	mVp-p	
t_r, t_f	Output Rise/Fall Time	— —	175 —	— —	175 —	— —	— t_{rin},t_{fin}	175 —	— —	175 —	ps	V_{ID} > 100mVp-p V_{ID} < 100mVp-p
V_{OD}	Differential Output Voltage Swing(2)	— —	— —	— —	— —	— —	600 200	— —	— —	— —	mV mV	V_{ID} = 15mVp-p V_{ID} = 5mVp-p
t_{OFFL}	LOS Release Time(3) Minimum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs	
t_{OFFH}	LOS Release Time(4) Maximum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs	
t_{ONL}	LOS Assert Time(3)	—	0.5	—	0.5	—	0.2	0.5	—	0.5	µs	
V_{SR}	LOS Sensitivity Range	5	50	5	50	5	—	50	5	50	mVp-p	2^{23}-1 pattern
HYS	LOS Hysteresis	2	8	2	8	2	4.6	8	2	8	dB	

NOTES:

1. Input referred noise = RMS output noise/low frequency gain.
2. Input is a 622MHz square wave.
3. Input is a 200MHz square wave, tr < 300ps, 8mVp-p.
4. Input is a 200MHz square wave, tr < 300ps, 1.8Vp-p.

DESIGN PROCEDURE

Output Termination

The SY88923 outputs must be terminated with a 50Ω load to VCC – 2V (or thevenin equivalent).

Layout and PCB Design

Since the SY88923 is a high-frequency component, performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via power supply.

The SY88923 ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

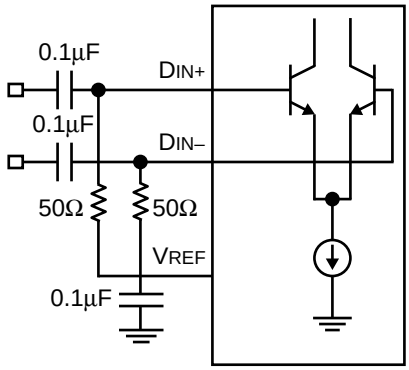
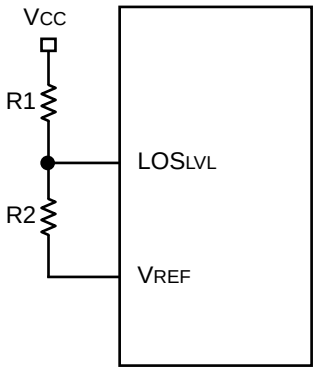


Figure 2. Differential Input Configuration



NOTE:
Resistor Divider = R2/ (R1 + R2)
R1 + R2 ≥ 5kΩ

Figure 3. LOSLVL Circut

PERFORMANCE CURVE

LOS Assert and Deassert Levels vs LOSLVL

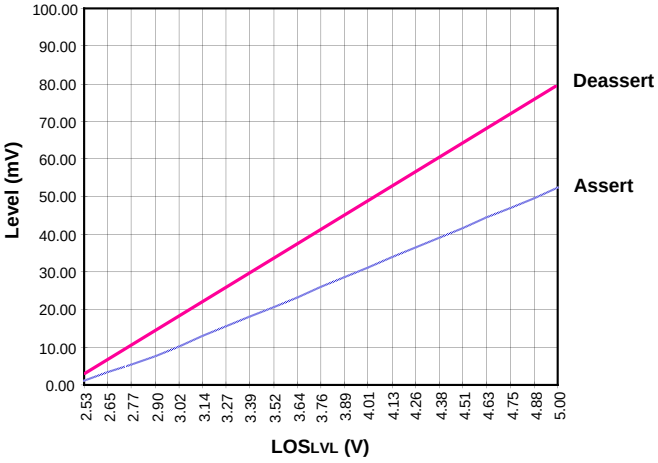


Figure 4. 2^{23}-1 Pattern

LOS Assert and Deassert Levels vs Resistor Divide

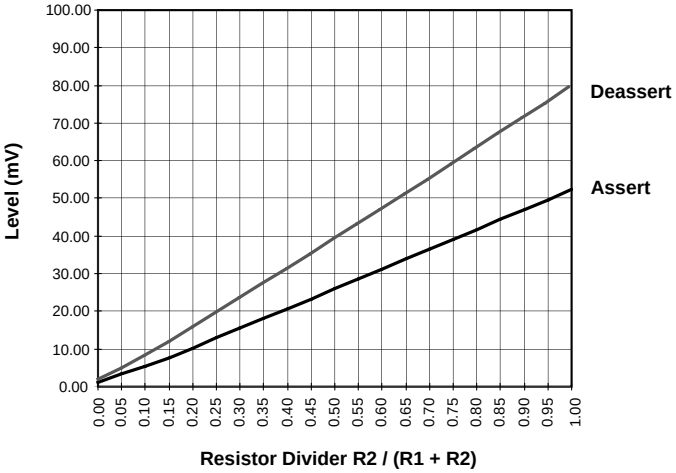
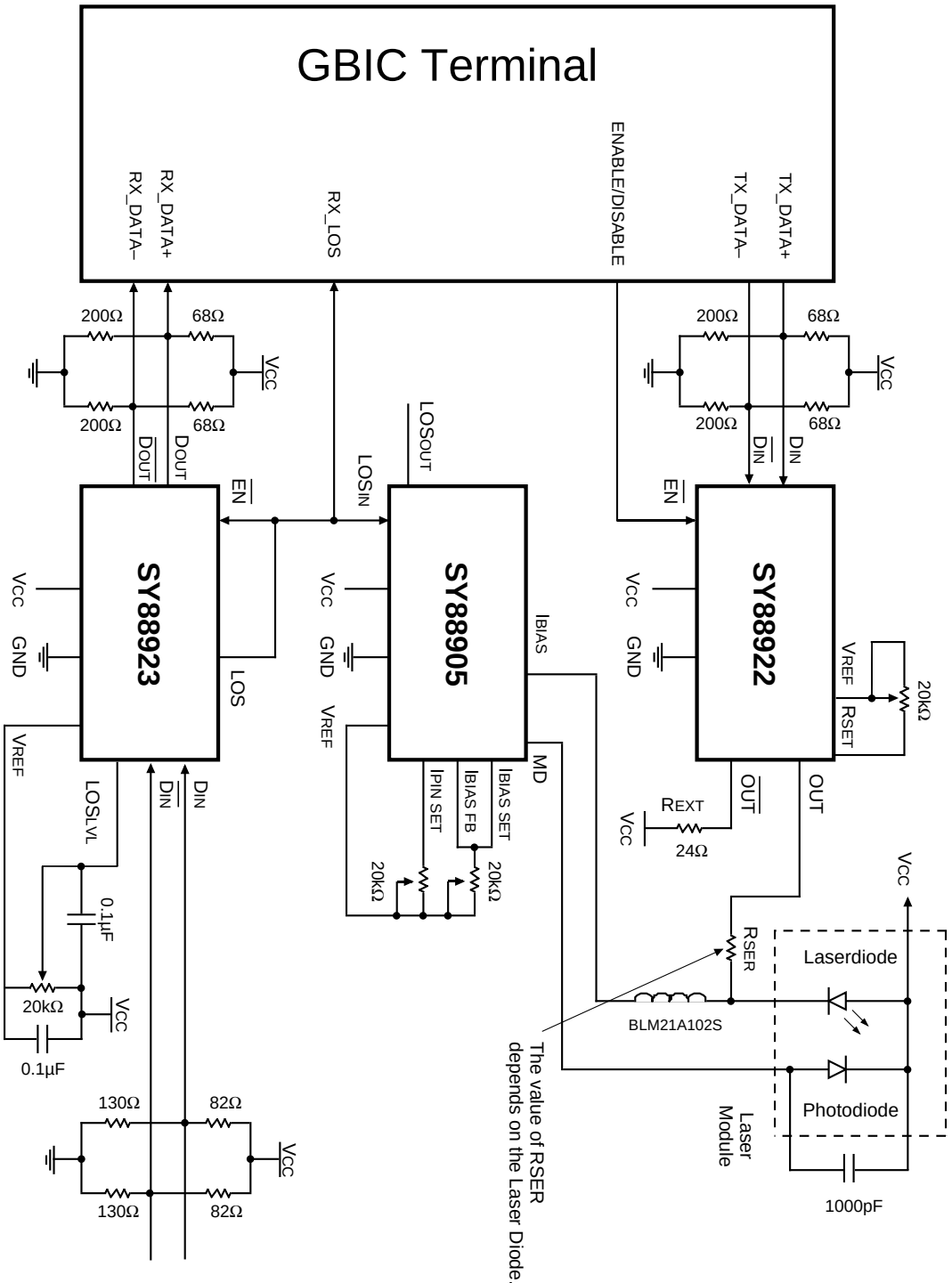


Figure 5. 2^{23}-1 Pattern

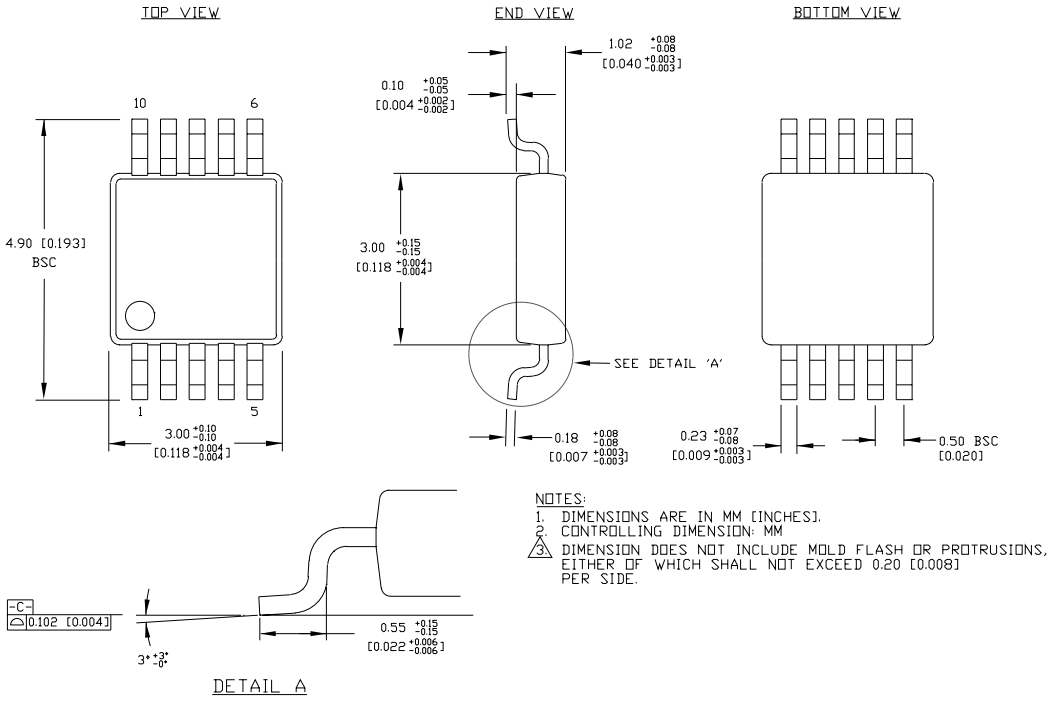
APPLICATION EXAMPLE FOR 3-CHIP SET SOLUTION



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY88923KC	K10-1	Commercial

10 LEAD MSOP (K10-1)



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